Error sources on the transmit path of a sync message

Dragan Obradovic, Siemens AG
Günter Steindl, Siemens AG

Initial statements

“Time-stamping error“
due to “timestamp granularity“ – transmit and receive timestamp are „too late“ and never too early

“Dynamic timestamp error“
Due to “MAC/PHY latency variation“

“IEEE 802.3 Clause 90“
This includes the optimizations from IEEE 802.3cx

“Cable asymmetry“
Standard Ethernet cables do allow for 40ns/100m asymmetry
<compensation not feasable>

“Digital control“
Hardware to adding an additional or skipping the intended tick every user defined interval of ticks.

“Rate of change of fractional frequency offset for the oscillator“
ClockSource/ClockMaster := 3 ppm/s due to external tunning + 1 ppm/s due to environmental conditions
ClockTarget/ClockSlave := 1 ppm/s due to environmental conditions
LocalClock := 1 ppm/s due to environmental conditions

“Frequency range for the oscillators“
+/- 50 ppm for PTP end instances
+/- 25 ppm for Grandmaster

Time transmission path

ClockSource to ClockMaster

Time transmission path

ClockSource to ClockMaster

ClockSource very likely has its own oscilator, including the capability to digital control the rate of counting.

ClockMaster very likely has its own oscilator, including the capability to digital control the rate of counting.

Digital control: See page 2

Aligning a ClockMaster to the ClockSource, introduces and error.
Using PCIe PTM, in case of PCIe connecting in between, allows to reduce this error to +/- 100ns.

ClockMaster to MAC

Time transmission path

ClockMaster to MAC

Error:

Deviation of the Origin time in the Sync message from the ClockMaster time.

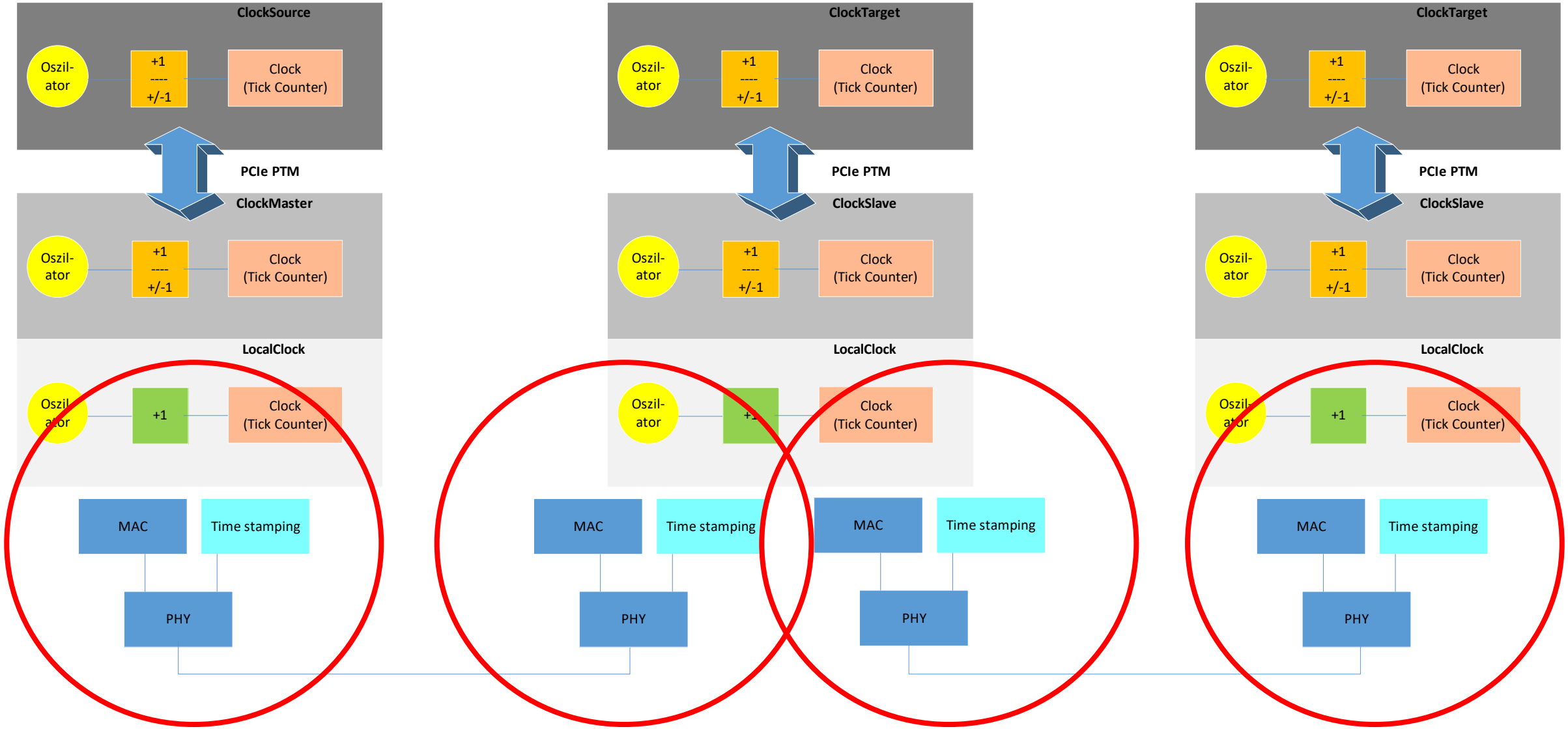
Rate deviation between the ClockMaster and the clock used for time stamping

How to avoid:

Limit the deviation between Origin time and the assumed time-stamped transmit time

MAC, PHY and time-stamping

Time transmission path



MAC, PHY and time-stamping

Error:

Latency variation of MAC and PHY after time-stamping

Time-stamping error due to resolution of the clock used for time stamping (e.g. 125MHz / 8ns)

Rate deviation between the ClockMaster and the clock used for time stamping

How to avoid:

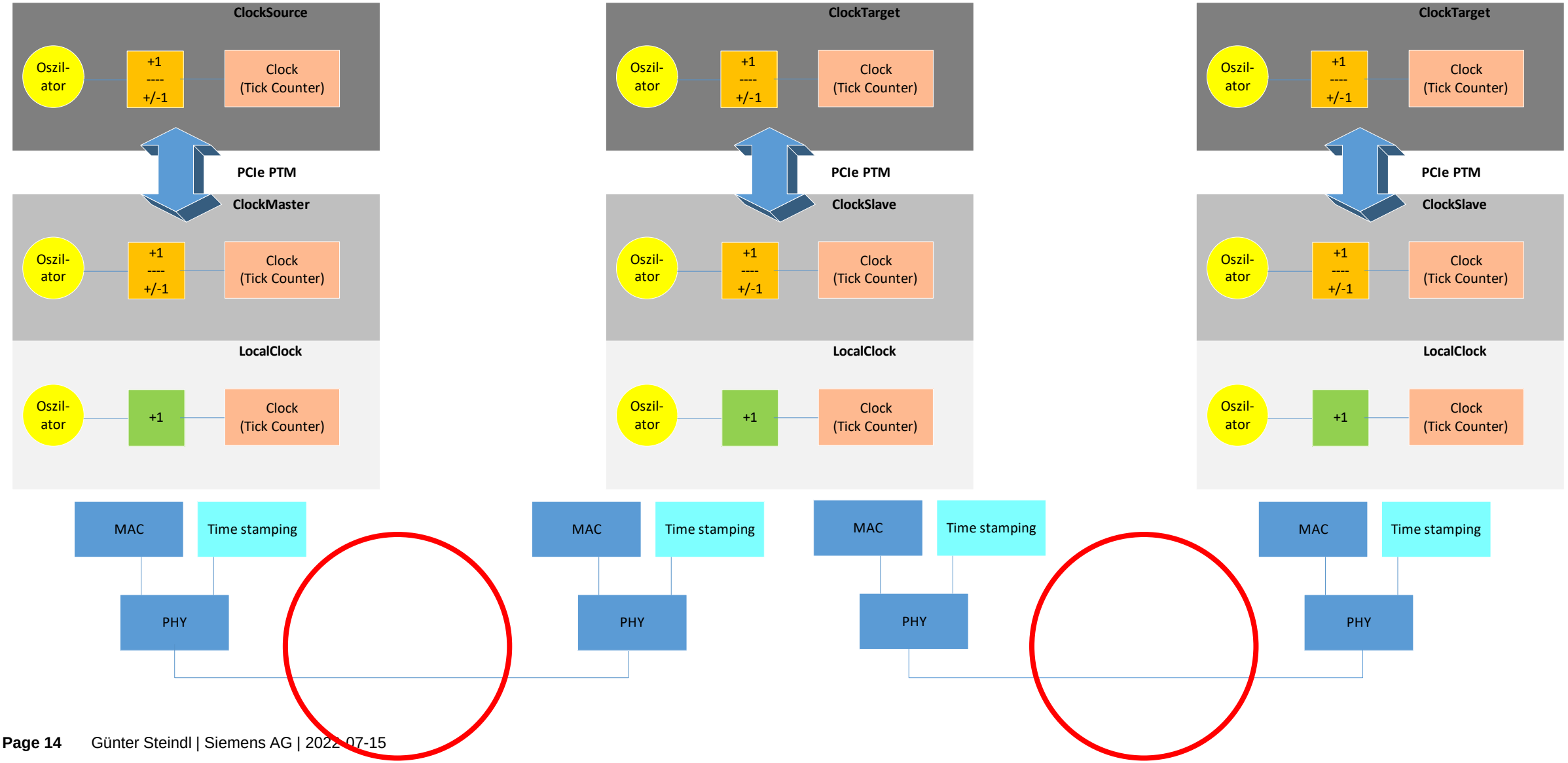
Use IEEE 802.3 Clause 90 concept for time-stamping
-> Additional limit the error for signaling

Use ClockMaster time for time-stamping
-> Avoid rate problems

Use 8ns or better 4ns for time-stamping
-> Reduce time-stamping error

Wire

Time transmission path



Wire

Error:

Asymmetry of the cable

Rate deviation between the clocks used for pdelay measurement

How to avoid:

Specify better cables
Align the clocks used for pdelay measurement

Note
If 802.3 Clause 90 is not used, thus, the latency variation of MAC + PHY after the time-stamping influences the pdelay measurement.

Measurement error increases with the value of latency variation.

MAC to ClockSlave

Time transmission path

MAC to ClockSlave

Error:

Rate deviation between the ClockSlave and the clock used for time stamping

How to avoid:

Limit the deviation between ClockSlave and the assumed time-stamped transmit time

ClockSlave

Time transmission path

ClockSlave

Error:

Offset between ClockMaster (Origin time + accumulated latency) due to rate difference between ClockSource and ClockSlave

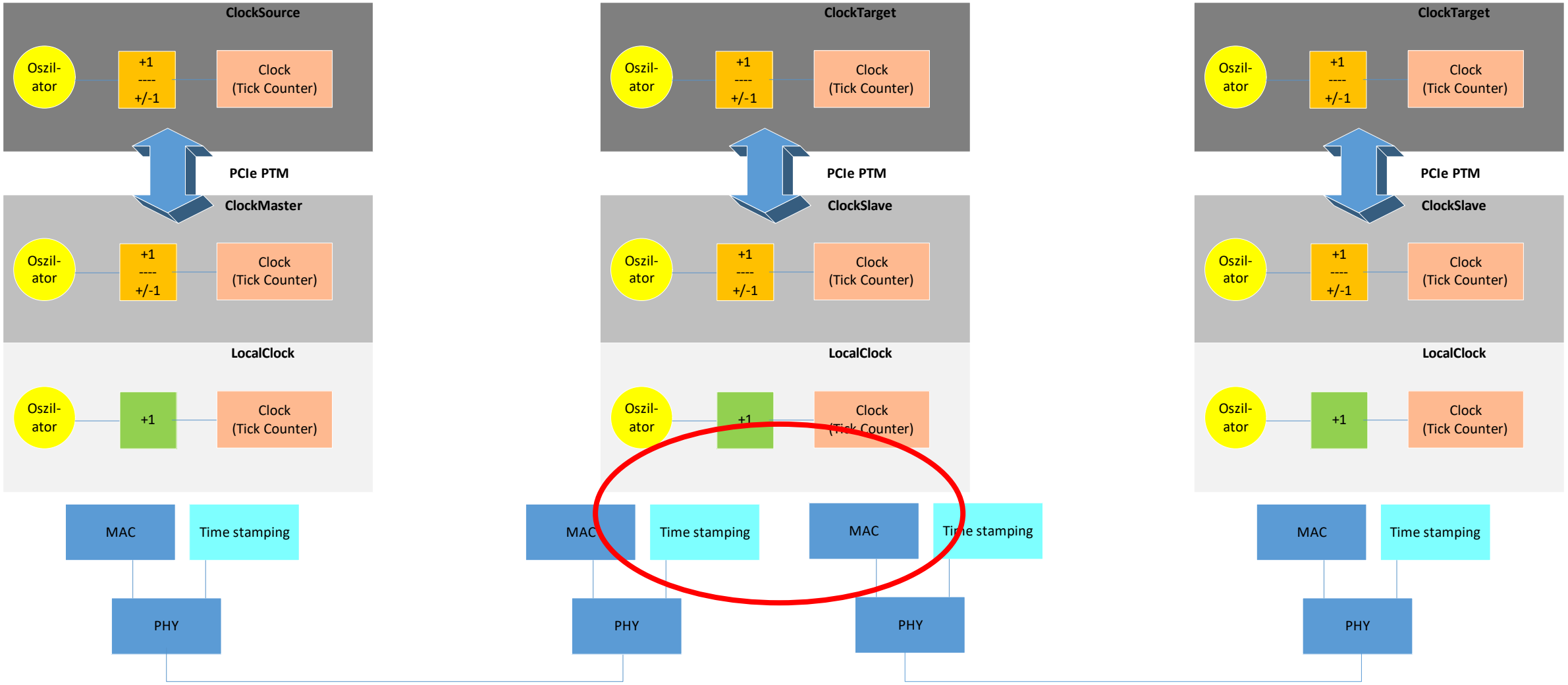
How to avoid:

Unavoidable under industrial working conditions

Compensate by
- measuring the offset between ClockMaster and ClockSlave with each received sync frame
- use the difference as input to a controller
- Control the ClockSlave time using digital control (see page 6)

Residence time

Time transmission path



Residence time

Error:

Rate deviation between the ClockMaster and the clock used for time stamping

Time-stamping error

How to avoid:

Unavoidable under industrial working conditions

Optimize (for Working Clock)
- by time-stamping (revceive and transmit) with ClockSlave (makes value added to accumulated latency a simple substraction + addition

Other timescales
- Rate compensation…

Optimizations for WorkingClock

Optimizations for WorkingClock

Enable hardware to

Time-stamp concurrently with LocalClock and WorkingClock ClockSlave; including 4ns time-stamps

Control WorkingClock ClockSlave by applying slide 20 offset control concepts; including digital control

Use WorkingClock ClockSlave time-stamps to calculate and update accumulated latency

Support IEEE802.3 Clause 90 time-stamping to reduce error introduced through latency variation

Limit wire parameters for asymmetry

NOTE
These optimization apply for WorkingClock; can be used for other timescales

Errors

Time transmission path

Errors - 1

(1)

ClockSource or ClockTarget
-> Own oscilator
-> Connection to ClockMaster or ClockSlave using PCIe PTM

Errors:
- Rate deviation between ClockSource or ClockTarget and ClockMaster or ClockSlave (e.g. x ppm/s)
- PCIe PTM introduced error (e.g. +/- 100ns)

Errors - 2

(2)

ClockMaster or ClockSlave
-> Own oscilator or (1) rate compensated clock
-> Connection to LocalClock

Errors:
- Rate deviation between ClockMaster or ClockSlave and LocalClock (e.g. x ppm/s)
- Error introduced by two independent clocks (e.g. xx ns)

Errors - 3

(3)

MAC, PHY and time-stamping

Errors:
Case 1: MAC time-stamping
-> Time-stamping error (e.g. 0..8ns)
-> MAC/PHY latency variation (e.g. xx ns)
-> Rate deviation to ClockMaster

Case 2: IEEE 802.3 Clause 90 time-stamping
-> Time-stamping error (e.g. 0..8ns)
-> Signal error (e.g. 0...xx ns)
-> Rate deviation to ClockMaster

Errors - 4

(4)

Wire
Lesser or greater dependent on the case

Errors:
Case 1: MAC time-stamping
-> Time-stamping error (e.g. 0..8ns)
-> MAC/PHY latency variation (e.g. xx ns)
-> Rate deviation to ClockMaster and between peers

Case 2: IEEE 802.3 Clause 90 time-stamping
-> Time-stamping error (e.g. 0..8ns)
-> Signal error (e.g. 0...xx ns)
-> Rate deviation to ClockMaster and between peers

Conclusion

This document is just a starting port showing that many entities contribute to the errors.

Todays solutions differ (in implementation) between WorkingClock and e.g. GlobalTime.