60802 Update on Time Sync

David McCall – Intel Corporation

Version 2

References – 1

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- David McCall “60802 Time Sync: Reducing dTE – Complexities & Tradeoffs – Ad Hoc Next Steps” https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-Errors-Complexity-Tradeoffs-Ad-Hoc-Next-Steps-0922-v02.pdf
- David “60802 Time Synchronisation – Monte Carlo Analysis: 100-hop Model, “Linear” Clock Drift, NRR Accumulation Overview & Details, Including Equations” https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Monte-Carlo-Multi-Hop-Overview-and-Details-0922-v02.pdf

References – 2

- Dragan Obradovic "ClockSlave PI Controller: Definition and Implementation“ https://www.ieee802.org/1/files/public/docs2022/60802-Obradovic-ClockSlave-1022-v02.pdf
- David McCall "60802 Time Sync Ad Hoc mNRRsmoothing Optimisation Results" https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-mNRRsmoothingN-Optimisation-Results-1122-v1.pdf

References – 3

- Max Turner "Alternative Sync/pDelay Processing" https://www.ieee802.org/1/files/public/docs2022/new-turner-alternateTimeStamping-1022-v01.pdf
- David McCall "60802 Time Sync Ad Hoc mNRRsmoothing Optimisation & Aligning pDelayResp & Sync" https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-mNRRsmoothingN-Optimisation-1022-v1.pdf

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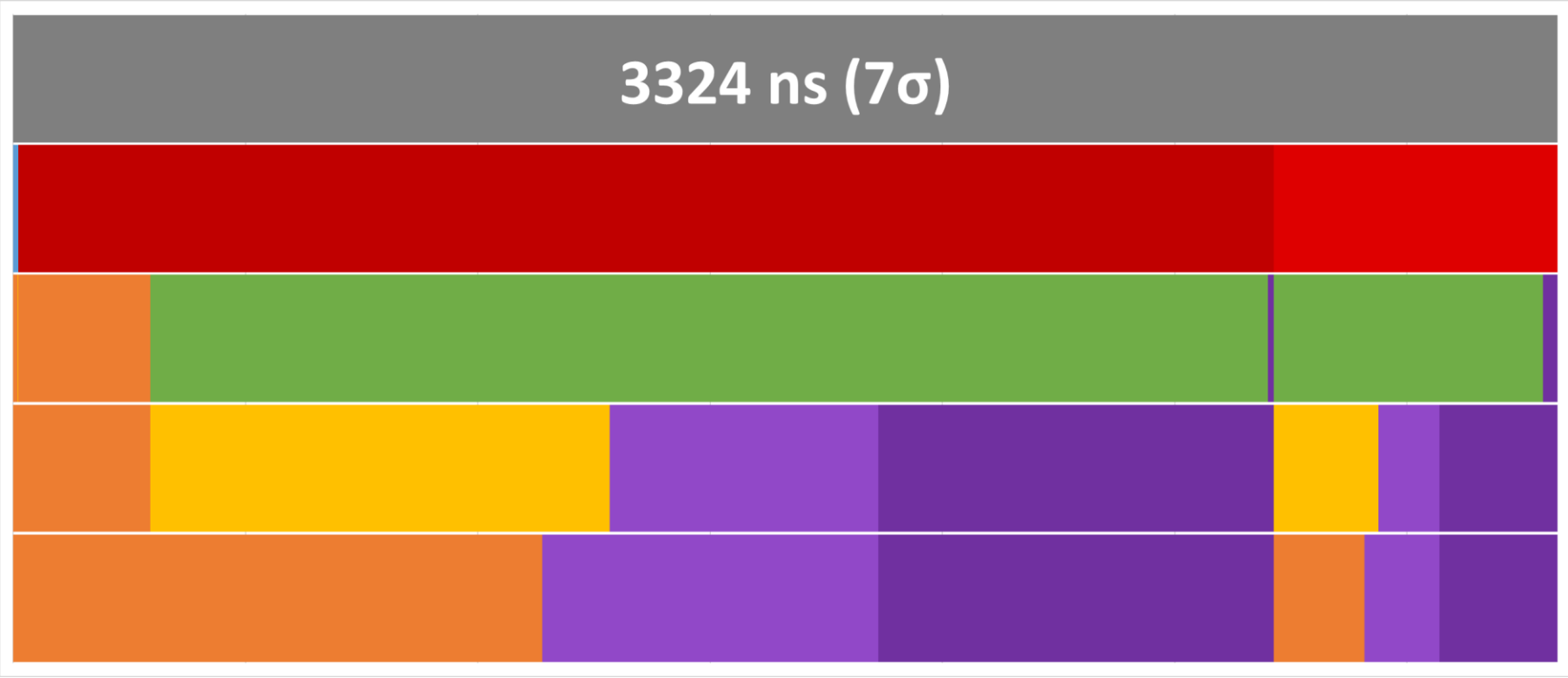
- Geoff Garner, "New Simulation Results for Time Error Performance for Transport over an IEC/IEEE 60802 Network Based on Updated Assumptions Revision 3" https://www.ieee802.org/1/files/public/docs2020/60802-garner-new-simulation-results-dte-updated-assumptions-60802-network-0920-v03.pdf
- Geoff Garner, "Further Simulation Results for Dynamic Time Error Performance for Transport over an IEC/IEEE 60802 Network Based on Updated Assumptions Revision 2" https://www.ieee802.org/1/files/public/docs2020/60802-garner-further-simulation-results-time-sync-transport-1120-v02.pdf
- Geoff Garner, "Effect of a Frequency Perturbation in a Chain of Syntonized Transparent Clocks" whitepaper https://www.ieee802.org/1/files/public/docs2007/as-garner-protocol-synton-chain-freq-offset-accum-0307.pdf
- Geoff Garner, "Effect of a Frequency Perturbation in a Chain of Syntonized Transparent Clocks" presentation https://www.ieee802.org/1/files/public/docs2007/as-garner-protocol-synton-chain-freq-offset-accum-vgs-0307.pdf

Content

- Baseline to “Pain-free”
- More Options (Varying Pain Levels)

Baseline to “Pain-free”

Baseline dTE Breakdown



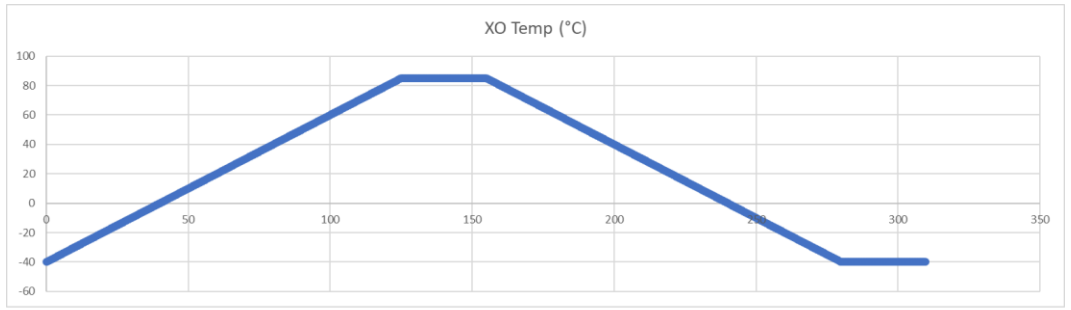
Baseline vs “Pain-free” – No Change

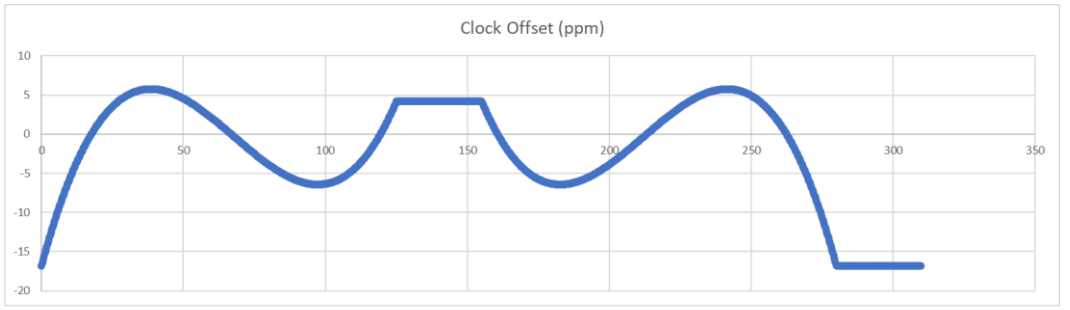
Parameter	Baseline	Pain-free
syncInterval	125ms Gamma distribution	
pDelayInterval	125ms Uniform distribution 90% - 130%	
Timestamp Granularity	8ns	
Dynamic Timestamp Error	±4ns	
meanLinkDelay Error Correction	95%	

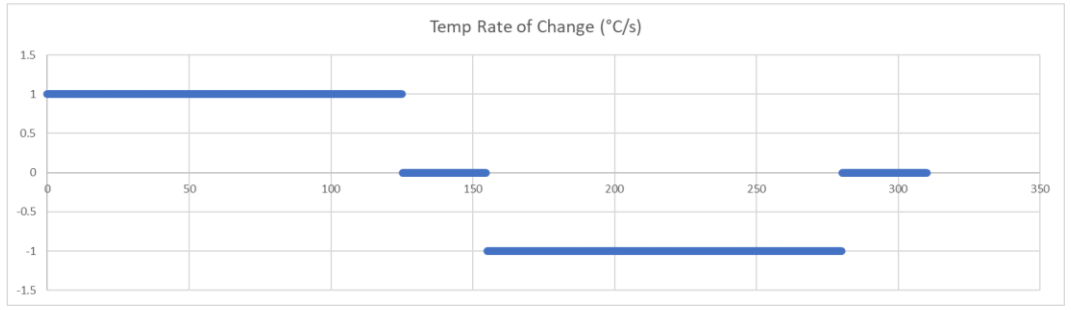
Baseline vs “Pain-free” – Differences

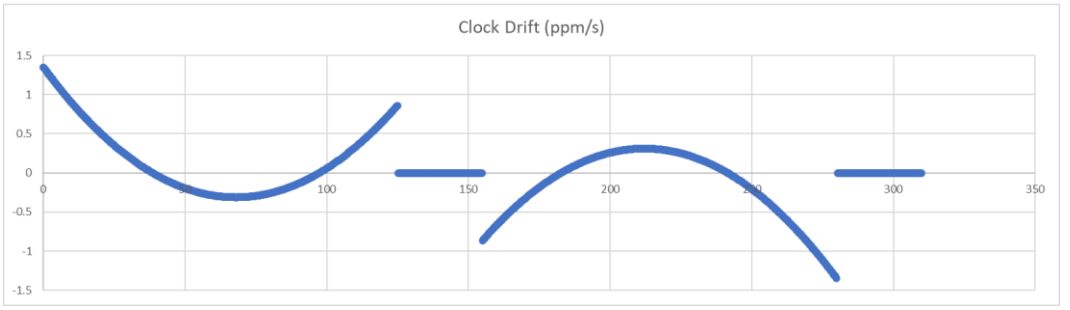
Parameter	Baseline	Pain-free
residenceTime	10ms Always 10ms, i.e. max limit	10ms Gaussian; mean 5ms; 6σ 5ms; min 1ms; max 10ms
pDelayTurnaroud	10ms Always 10ms, i.e. max limit	10ms Gaussian; mean 5ms; 6σ 5ms; min 1ms; max 10ms
mNRRsmoothingN	1	2
Temperature Ramp	Linear -40° to +85°C 1°C/s ; 30s Hold	Quarter-Sinusoidal -40° to +85°C 125s ramp up/down ; 30s hold

Clock Drift Example – Linear Temperature Ramp: 1°C/s ↕ (125s ↕)







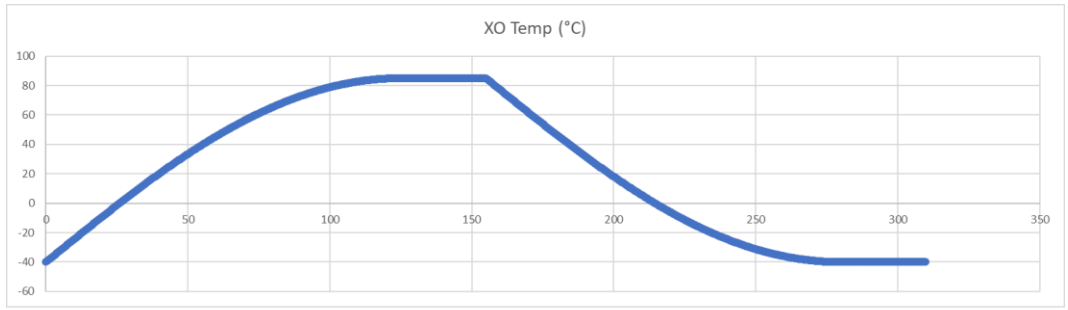


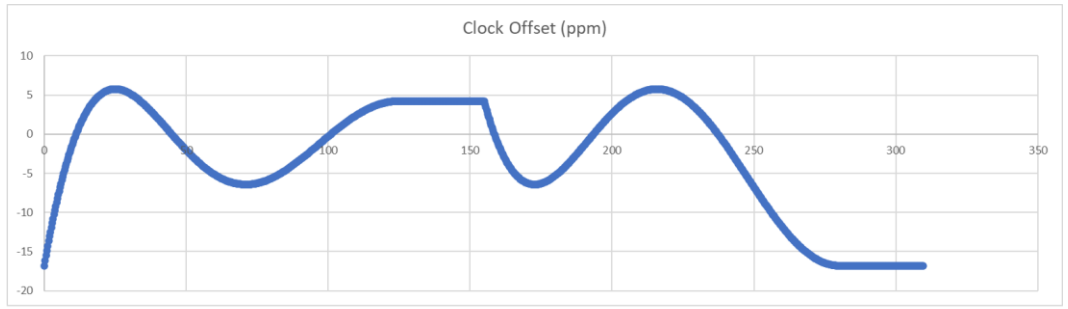
Inputs		
Temp Max	85	°C
Temp Min	-40	°C
Temp Ramp Rate	1	°C/s
Temp Hold	30	s

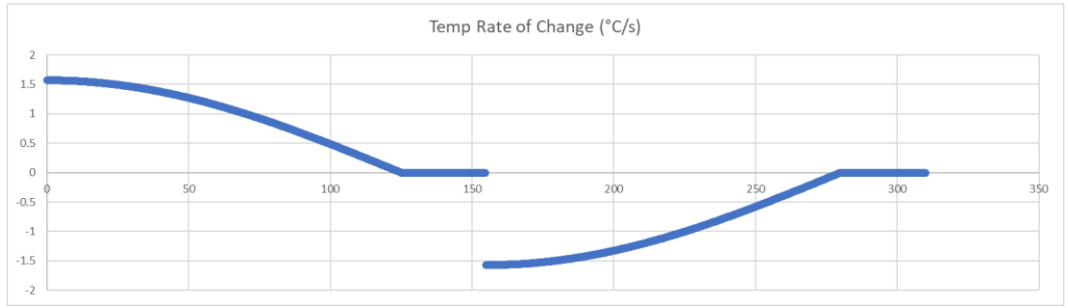
Temp Rate of Change		
MAX	1.00	°C/s
MIN	-1.00	°C/s

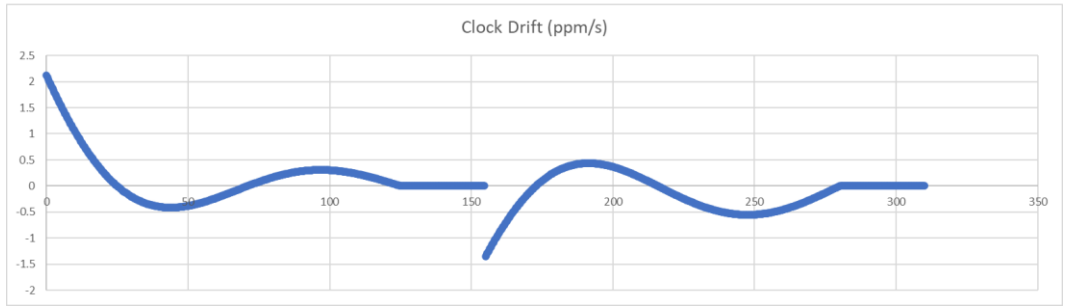
Clock Drift		
MAX	1.35	ppm/s
MIN	-1.35	ppm/s

Clock Drift Example – ¼-Sinusoidal Temperature Ramp: 125s ↕







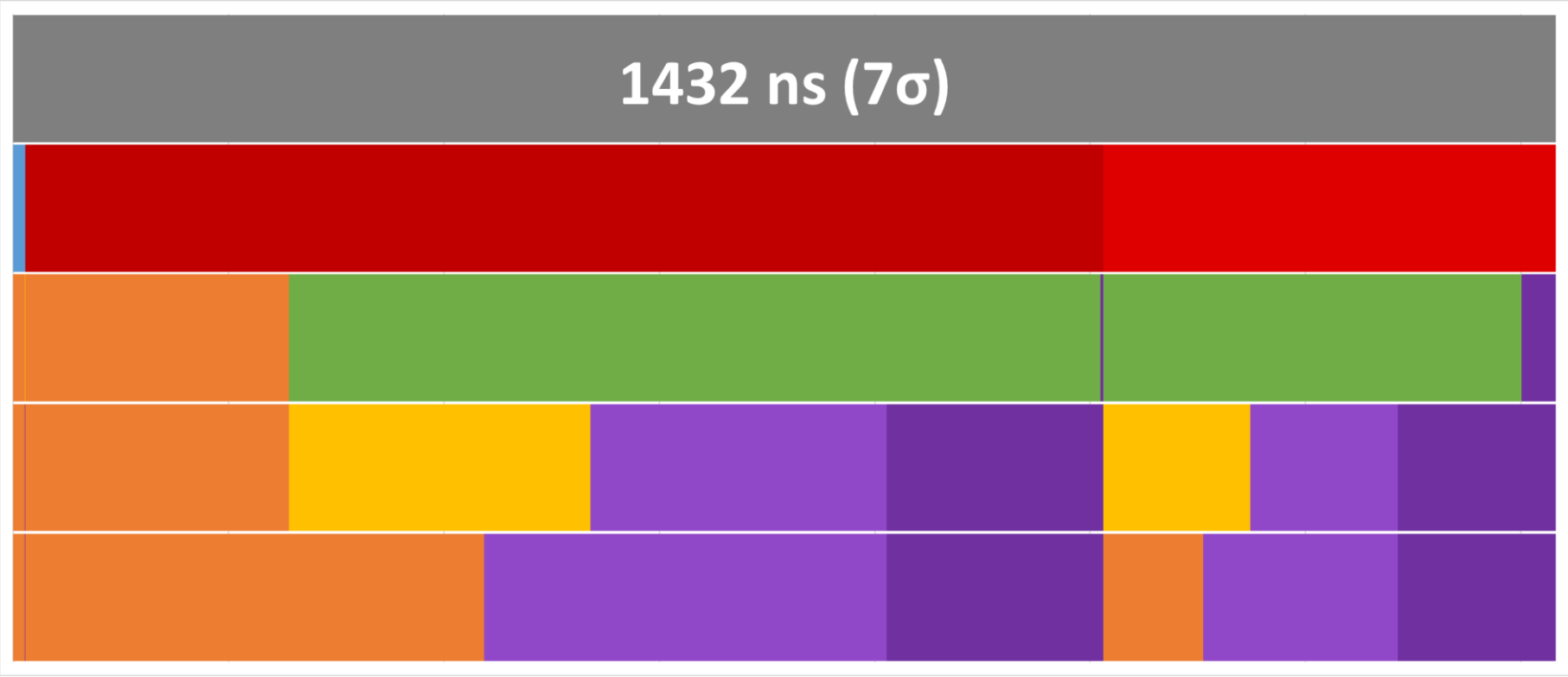


Inputs		
Temp Max	85	°C
Temp Min	-40	°C
Temp Ramp Period	125	s
Temp Hold	30	s

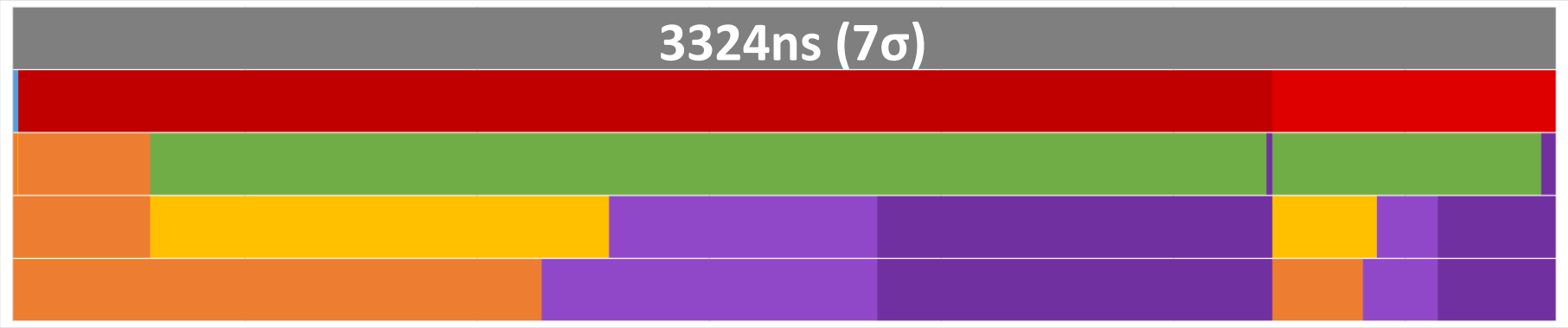
Temp Rate of Change		
MAX	1.57	°C/s
MIN	-1.57	°C/s

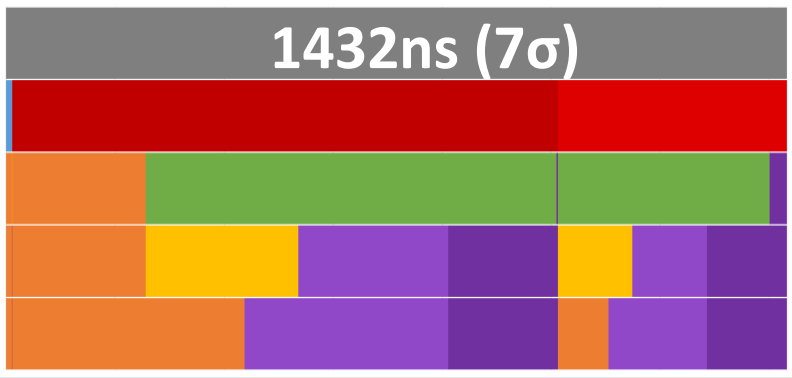
Clock Drift		
MAX	2.12	ppm/s
MIN	-1.35	ppm/s

“Pain-free” dTE Breakdown



Baseline vs. “Pain-free”





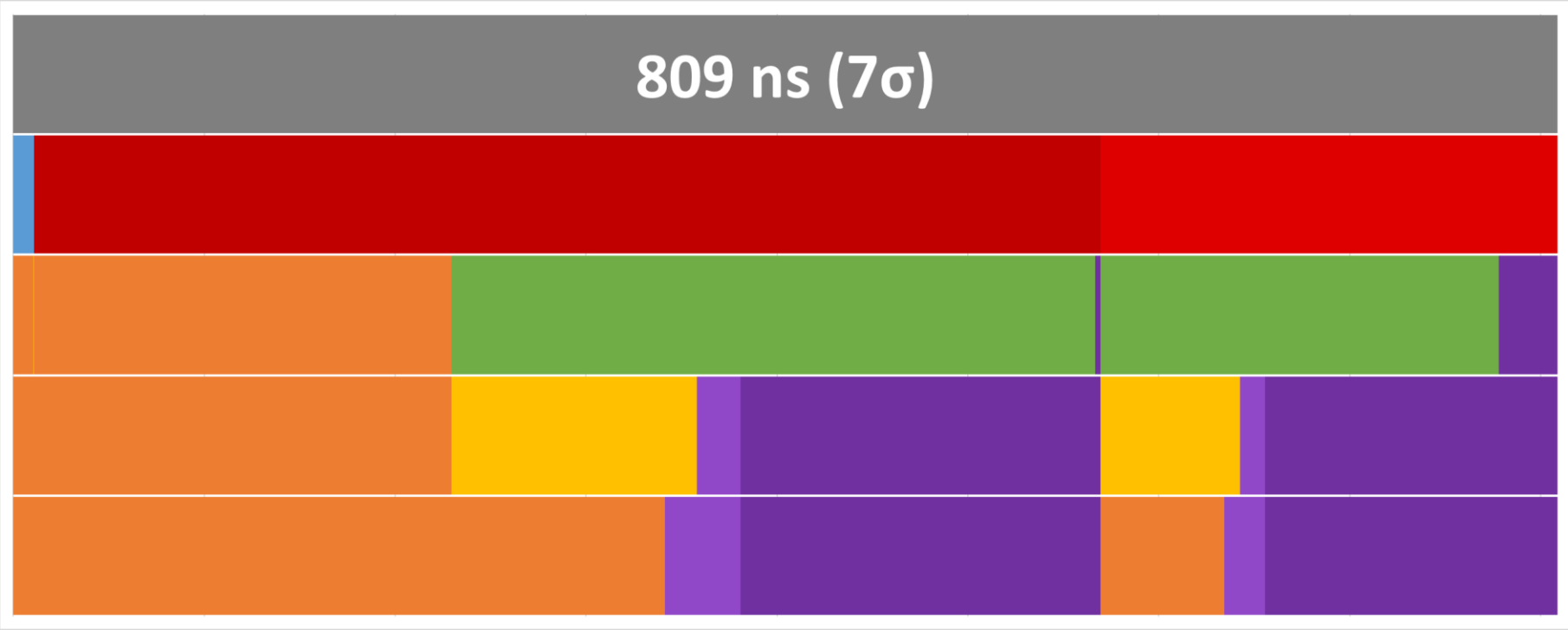
More Options

Varying Pain Levels

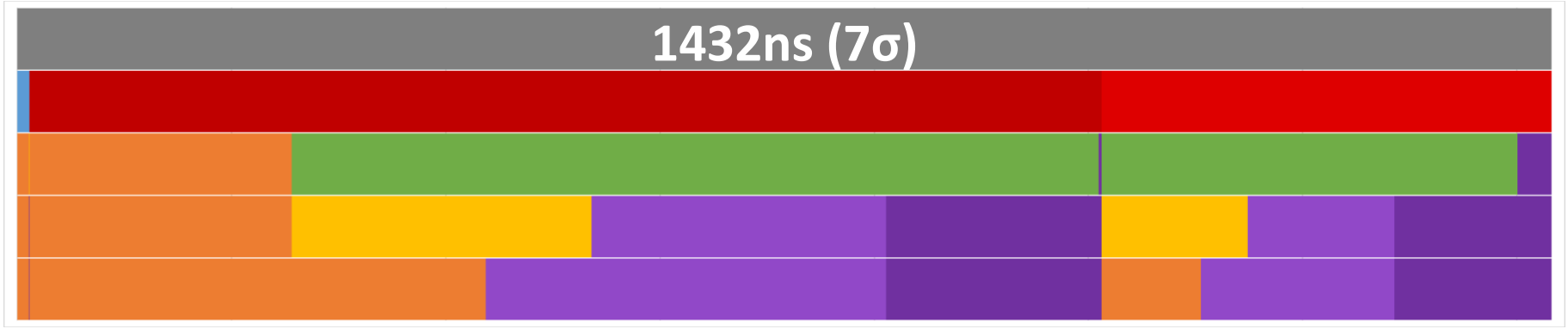
Baseline vs More Options

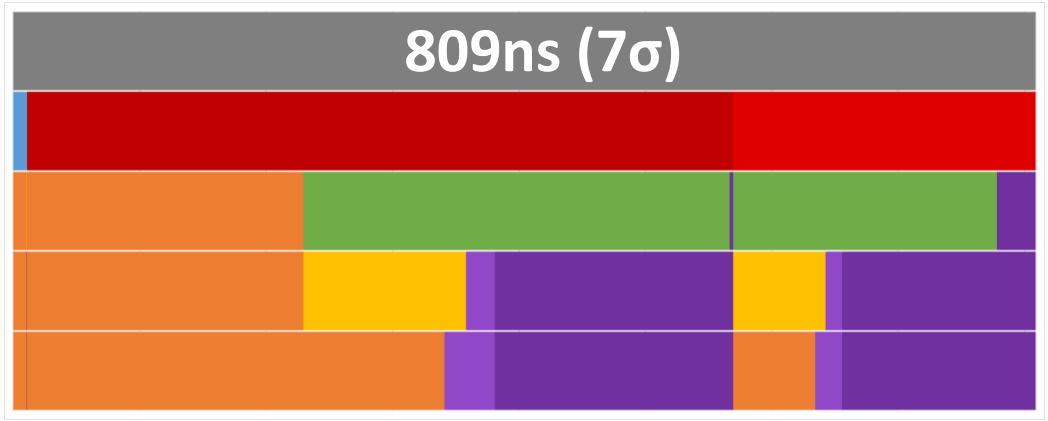
Parameter	Pain-free	More Options
pDelayInterval	125ms Uniform distribution 90% - 130%	125ms Uniform distribution 95% - 105%
NRR Drift Error Correction	0%	90%
mNRRsmoothingN	1	4

Other Options dTE Breakdown



“Pain-free” vs Other Options

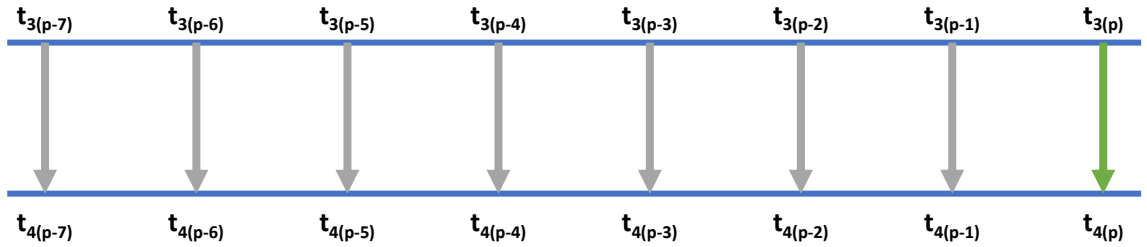




Even More Options

- Combination of mNRRsmoothingA and mNRRsmoothingN
  - Reduces effect of Timestamp error on mNRR
- Align pDelayResp with Sync
  - Reduces effect of NRR Clock Drift on mNRR
- Send TLV with t1out following Sync to allow downstream node to update mNRR just prior to Sync calculation
  - Reduces effect of NRR Clock Drift on mNRR
- RR Error Correction
- Calculate RR via Sync messaging (vs. accumulation of NRR)

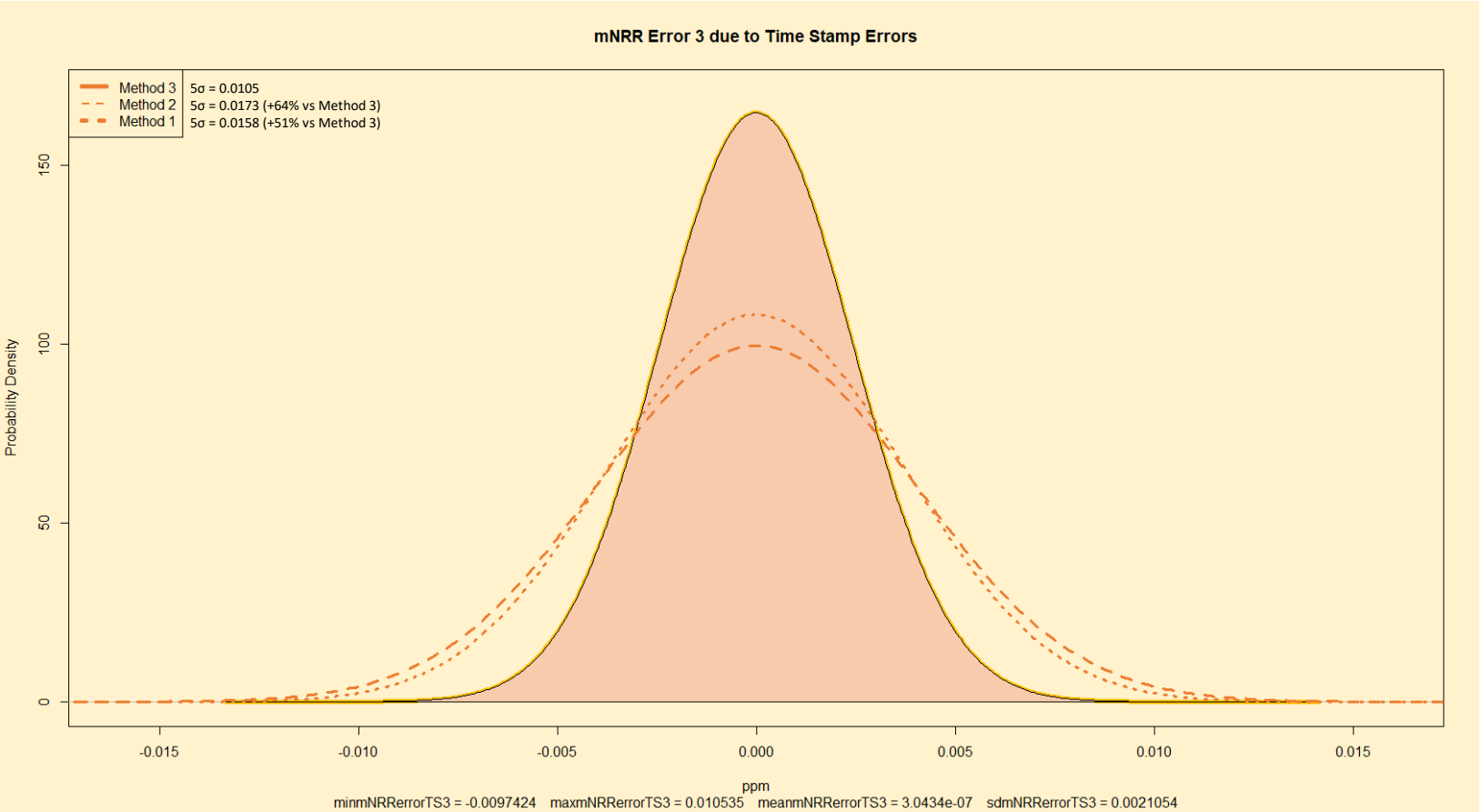
mNRRsmoothingN & mNRRsmoothingA – Examples



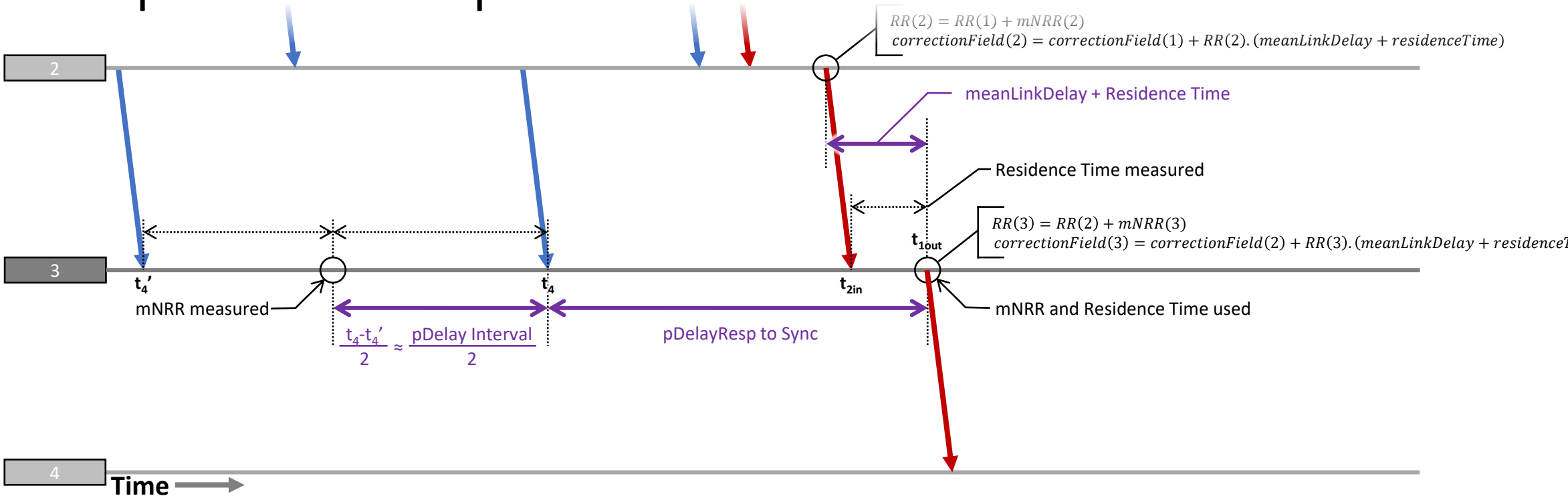
Method 1	mNRRsmoothingN = 1 mNRRsmoothingA = 1	p-1 — 1 — p
	mNRRsmoothingN = 4 mNRRsmoothingA = 1	p-4 — 4 — p
	mNRRsmoothingN = 7 mNRRsmoothingA = 1	p-7 — 7 — p
Method 2	mNRRsmoothingN = 1 mNRRsmoothingA = 4 Average of A, B, C & D	A: p-1 — 1 — p B: p-2 — 3 — p-1 C: p-3 — 5 — p-2 D: p-4 — 7 — p-3
Method 3	mNRRsmoothingN = 4 mNRRsmoothingA = 4 Average of A, B, C & D	A: p-4 — 4 — p B: p-5 — 6 — p-1 C: p-6 — 8 — p-2 D: p-7 — 10 — p-3

mNRRsmoothing Method Comparison

Input Errors		
Drift Type (Linear Temp Ramp)	2	
GM Clock Drift Max	+1.35	ppm/s
GM Clock Drift Min	-1.35	ppm/s
Fraction of GM nodes w/ Drift	80%	
non-GM Clock Drift Max	+1.35	ppm/s
non-GM Clock Drift Min	-1.35	ppm/s
Fraction of non-GM Nodes w/ Drift	80%	
Temp Max	+85.	°C
Temp Min	-40.	°C
Temp Ramp Rate	±1	°C/s
Temp Ramp Period	125	s
Temp Hold Period	30	s
GM Scaling Factor	100%	
non-GM Scaling Factor	100%	
Timestamp Granularity TX	±4	ns
Timestamp Granularity RX	±4	ns
Dynamic Time Stamp Error TX	±4	ns
Dynamic Time Stamp Error RX	±4	ns
Input Parameters		
pDelay Interval	31.25	ms
Sync Interval	125	ms
pDelay Turnaround Time	10	ms
residenceTime	10	ms
Input Correction Factors		
Mean Link Delay Averaging	0%	
NRR Drift Rate Correction	90%	
RR Drift Rate Error Correction	0%	
pDelayResp → Sync Type (Uniform)	1	
pDelayResp → Sync Max	100%	
pDelayResp → Sync Min	0%	
pDelayResp → Sync Target	10	ms
mNRR Smoothing N	15, 1, 8	
mNRR Smoothing A	1, 15, 8	
Configuration		
Hops	100	
Runs	100,000	



Clock Drift Error – Relevant Intervals
4 Hops – 3rd Hop



pDelayResp Sync

- Same errors in NRR and RR as 2nd Hop.
  - Error due to drift during NRR measurement. (**Node 3** to **Node 2**)
  - Error due to drift between measuring and using NRR. (**Node 3** to **Node 2**)
  - Error due to drift during Residence Time measurement. (**Node 3** to **GM**)
  - Error due to drift between RR(2) calculation, at Node 2, and use in calculating RR(3). (**Node 2** to **GM**)

Thank you!