

60802 Time Sync Contribution Normative Requirements & Informative Text

David McCall – Intel Corporation

Version 1

References

1. David McCall “60802 Update on Time Sync”
<https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Update-On-Time-Sync-Status-15-Nov-1122-v2.pdf>
2. David McCall “60802 Time Sync Contribution Discussion”
<https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-Contribution-Discussion-17-Nov-1122-v2.pdf>
3. David McCall “[60802 Time Sync Contribution Discussion – 2nd December 2022](#)”

Before We Start... ChatGPT

- Please tell me, in simple terms, what Time Sensitive Networking is.
- Time Sensitive Networking (TSN) is a set of networking technologies that are designed to provide deterministic, low-latency communication for real-time systems. TSN uses time synchronization and reservation protocols to ensure that time-critical data is delivered within a specified time window, allowing devices on a network to coordinate their actions and respond to events in a timely and predictable manner. This is particularly useful in industrial and other environments where precision and reliability are essential. TSN is being standardized by the Institute of Electrical and Electronics Engineers (IEEE) as a way to support a wide range of applications, including factory automation, traffic control, and power grid management.

Before We Start... ChatGPT

- What is IEEE 802.1AS?
- IEEE 802.1AS is a standard for time-sensitive networking (TSN) that specifies a protocol for precise time synchronization in local area networks (LANs). The standard defines a set of mechanisms for distributing time information over a network, allowing devices on the network to synchronize their clocks and align their actions with respect to time. This is important in many real-time applications, such as factory automation and traffic control, where precise timing is essential for correct operation. IEEE 802.1AS builds on the existing IEEE 1588 standard for network time synchronization, adding new features and capabilities that are specifically tailored to the needs of TSN.

Agenda

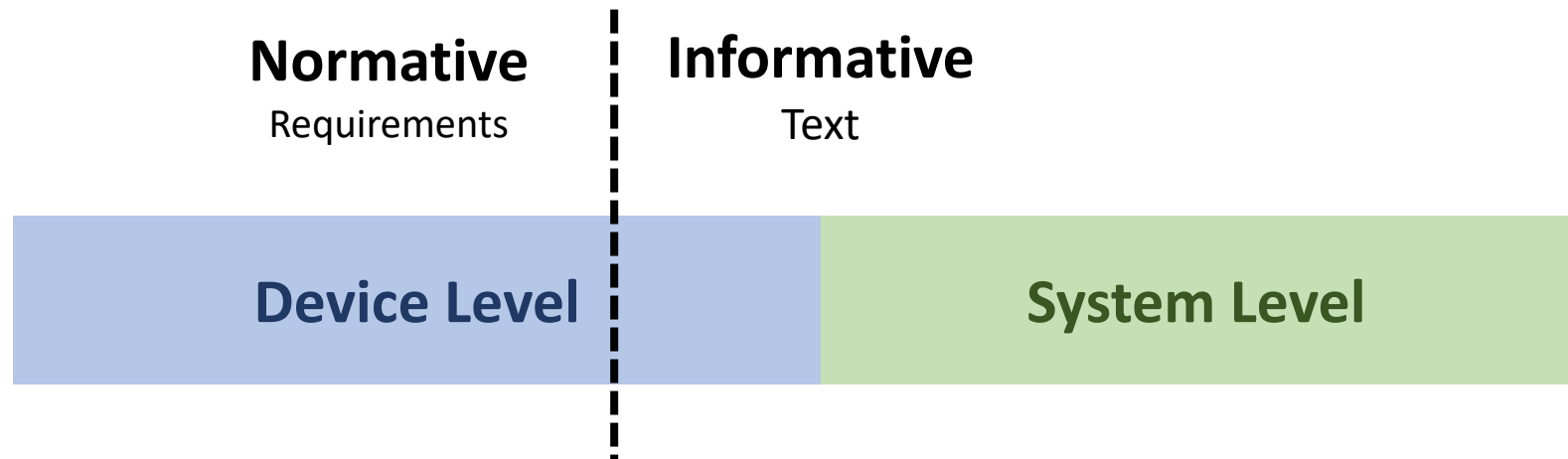
- Error Accumulation & Approach to Error Budget Management
- Normative Requirements
- Informative Text
- What Else?

Error Accumulation & Error Budget Management

Device-level requirements for system-level performance

Assumptions

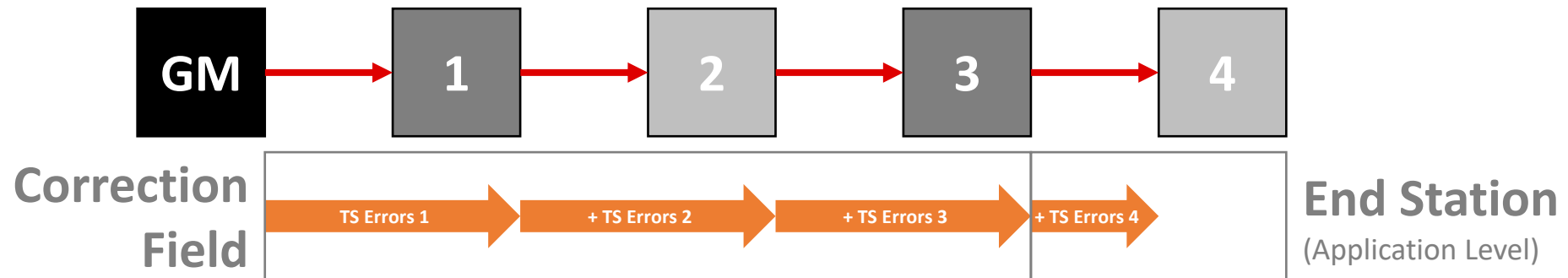
- All normative requirements are device-level
 - Single Bridge / End Station
- Any system-level content will be in the informative text
 - There may also be device-level content in the informative text



Propositions

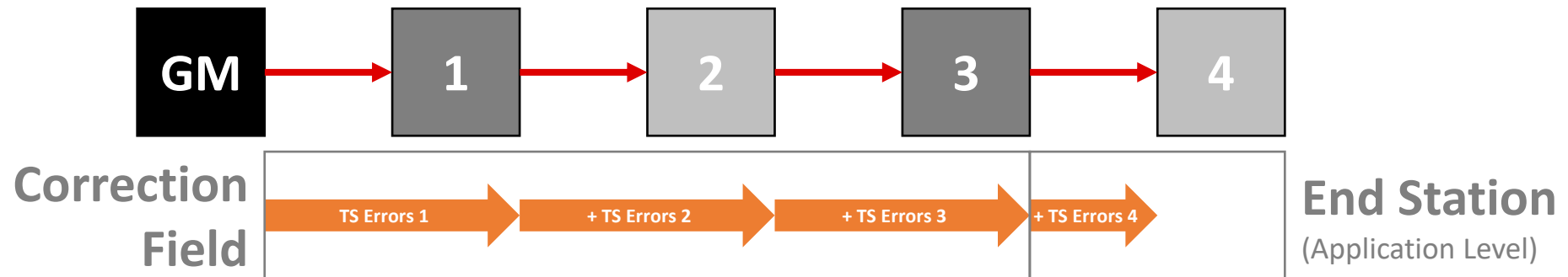
- The specification must include different normative requirements for error generation under different circumstances
 - No Clock Drift
 - NRR Clock Drift
 - RR Clock Drift
- For No Clock Drift, Correction Field offers the best measure
 - Timestamp Error
- For NRR & RR Clock Drift, Rate Ratio field offers the best measure
 - NRR: Clock Drift error when upstream node's (or local node's) Local Clock drifts
 - RR: Clock Drift error when GM's (or local node's) Local Clock drifts

Error Accumulation – Mix of Circumstances



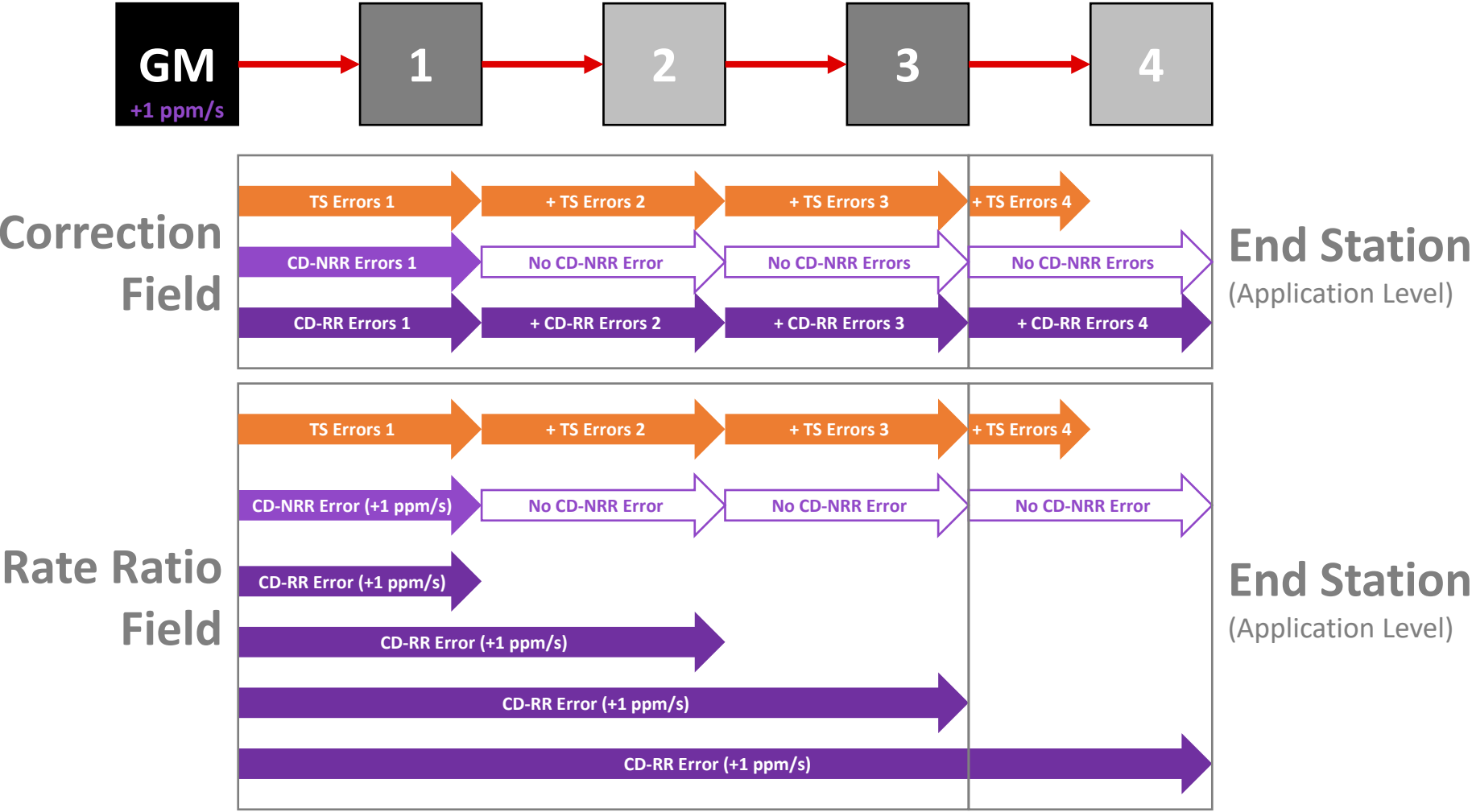
- System-level performance is based on devices experiencing different levels of Clock Drift. (Modelled via temperature curve.)
- Some devices won't experience much, if any.
 - If **every** device experienced zero clock drift, dTE would be entirely due to Timestamp Errors (combination of Time Stamp Granularity & Dynamic Time Stamp Error).

Error Accumulation – Mix of Circumstances

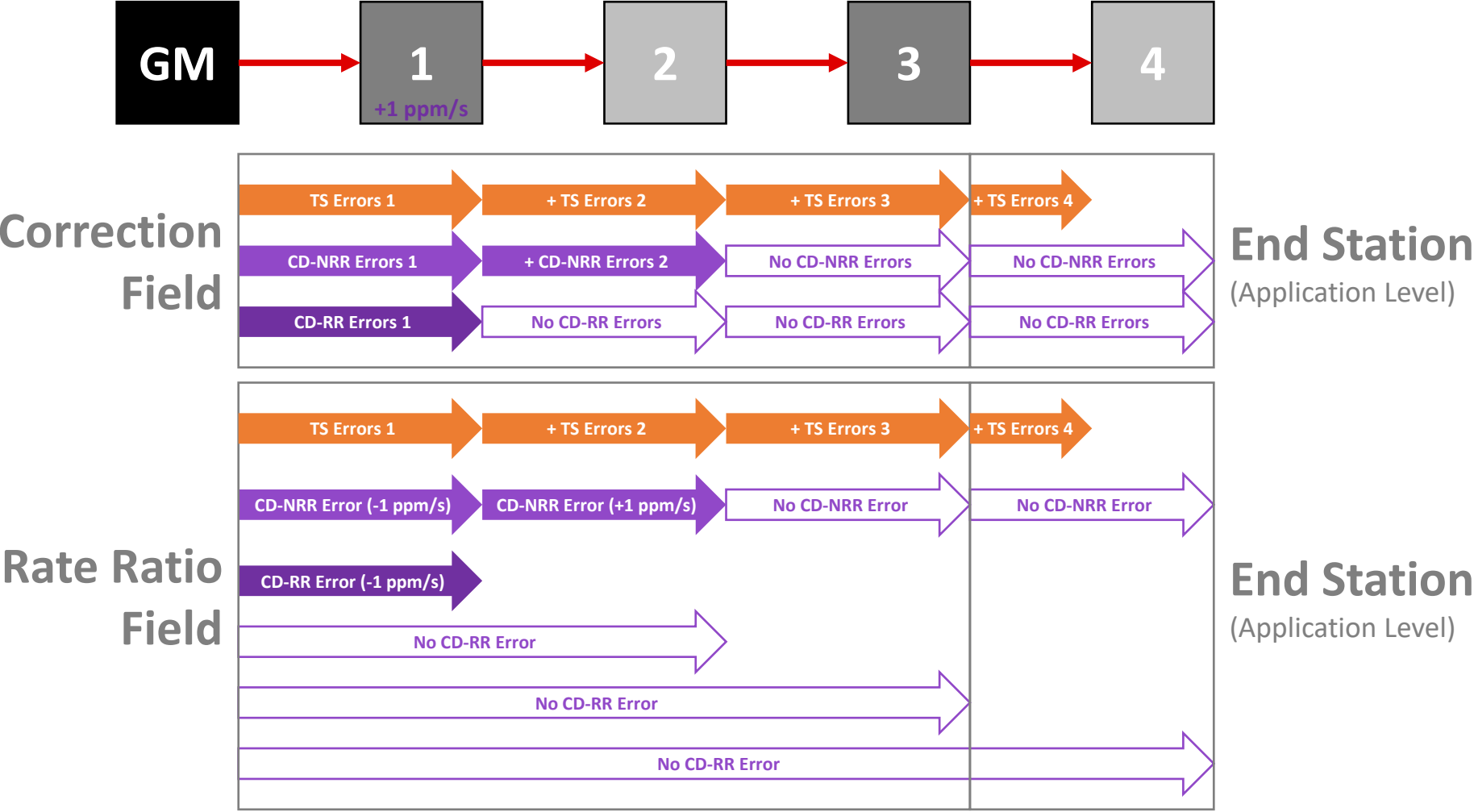


- Some devices' Local Clocks will drift.
 - Effect varies depending on which devices clock drifts.

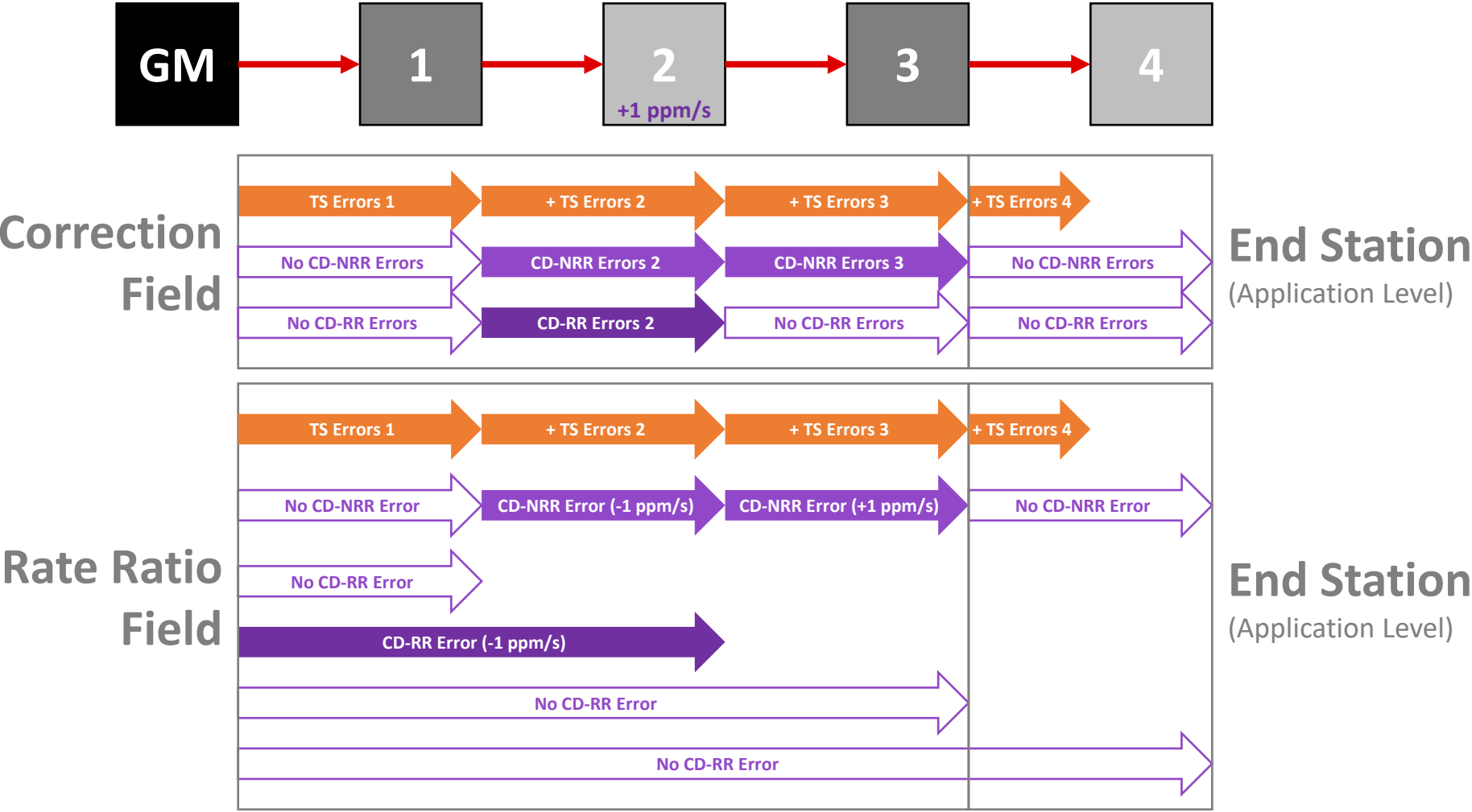
Error Accumulation – Mix of Circumstances



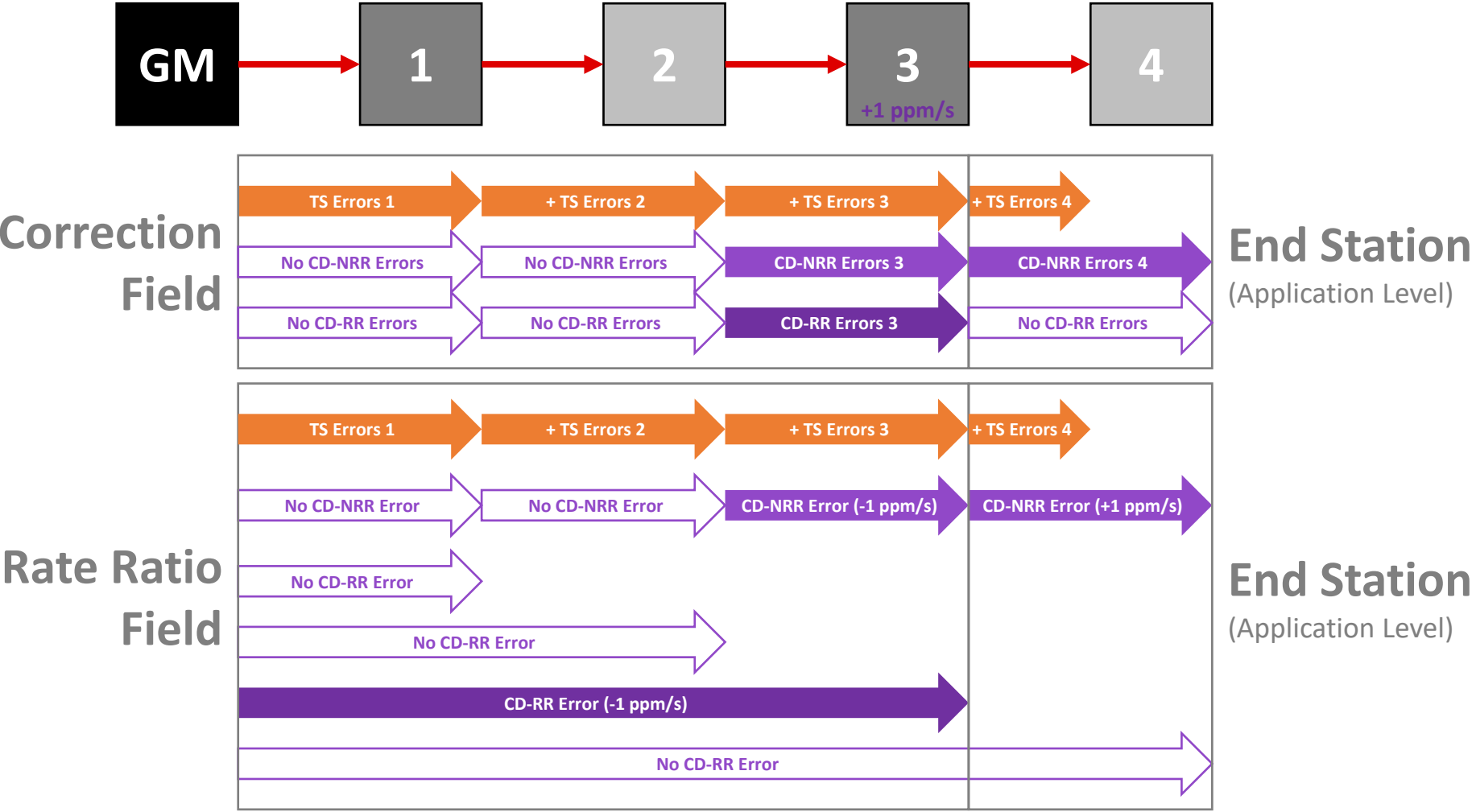
Error Accumulation – Mix of Circumstances



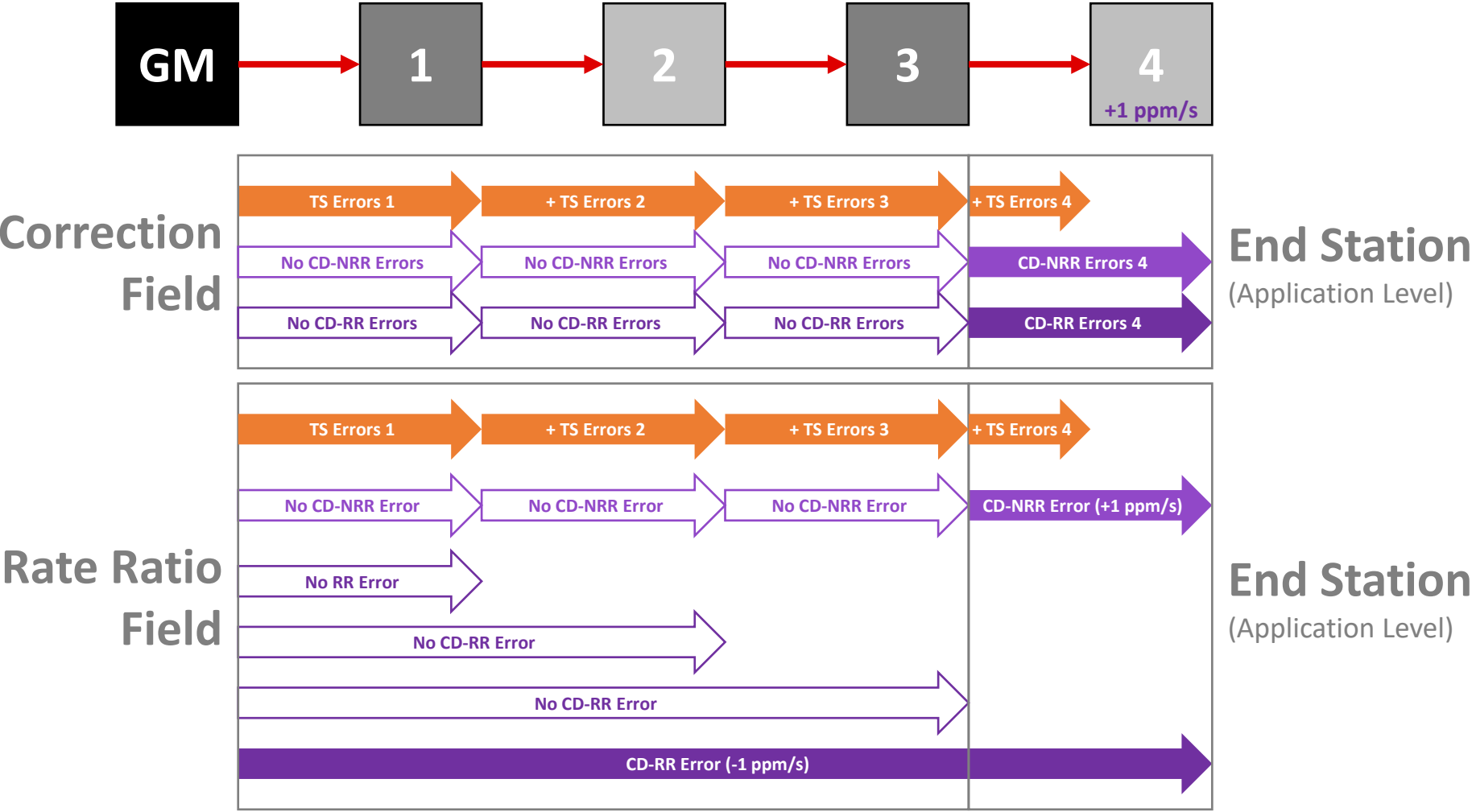
Error Accumulation – Mix of Circumstances



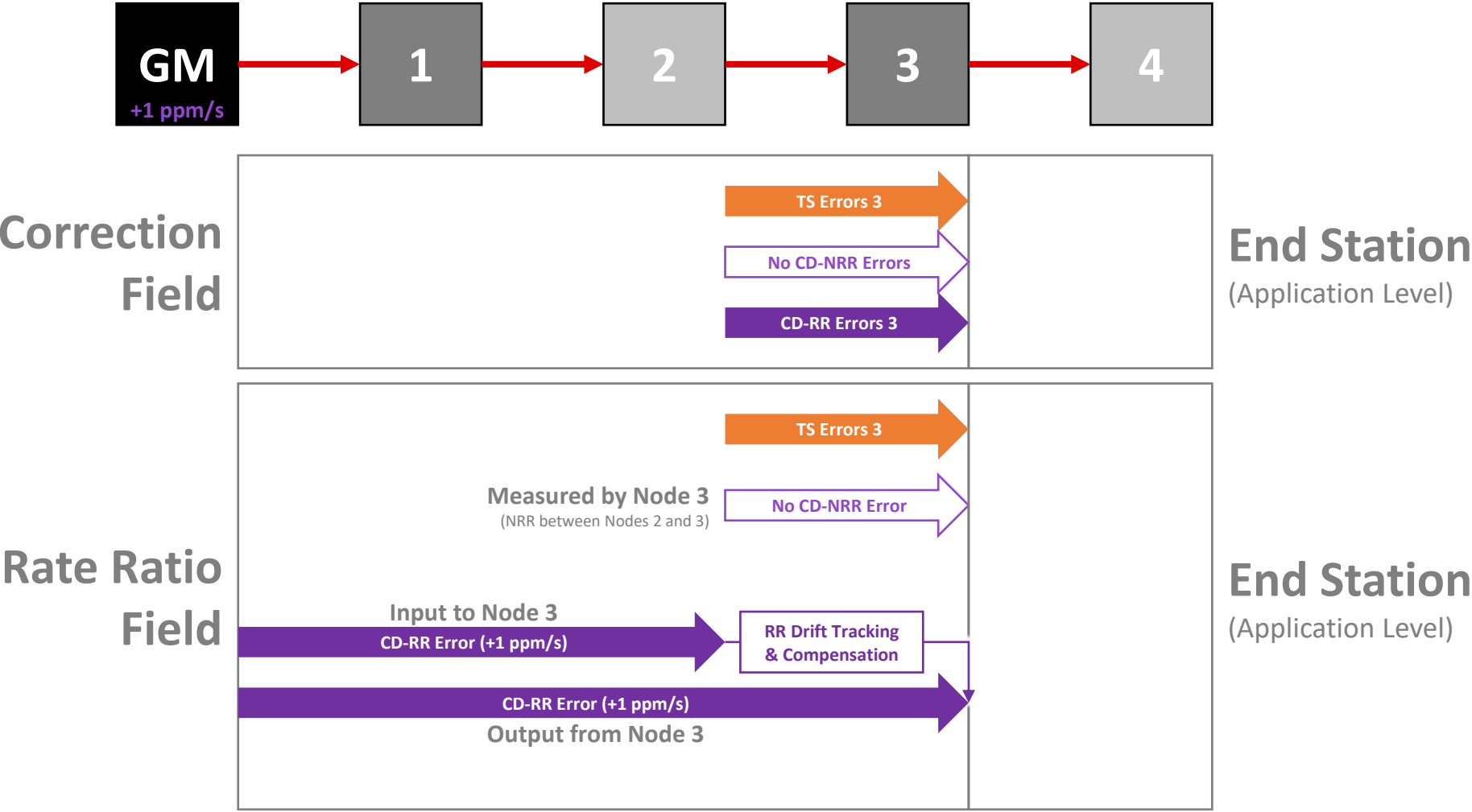
Error Accumulation – Mix of Circumstances



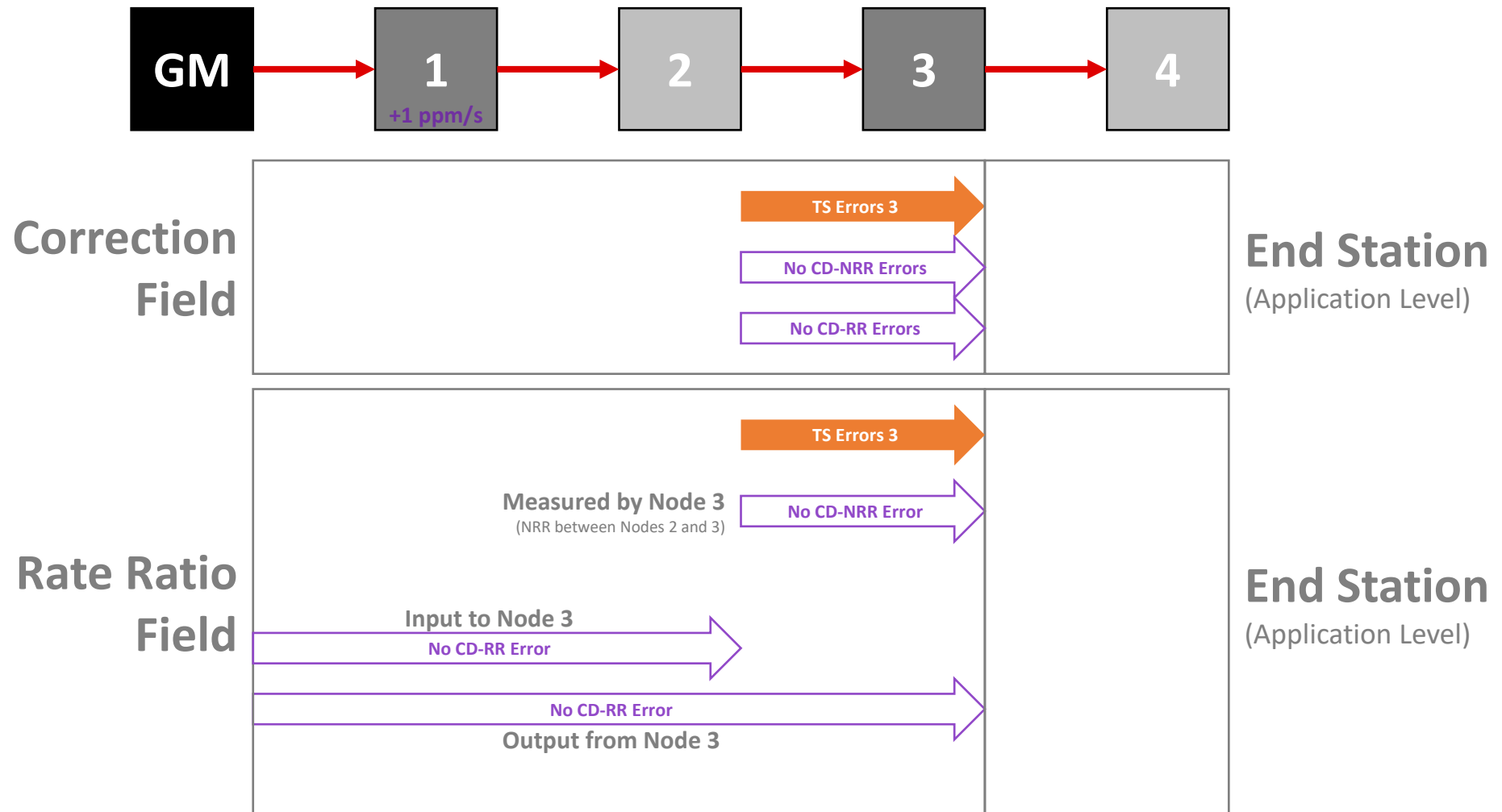
Error Accumulation – Mix of Circumstances



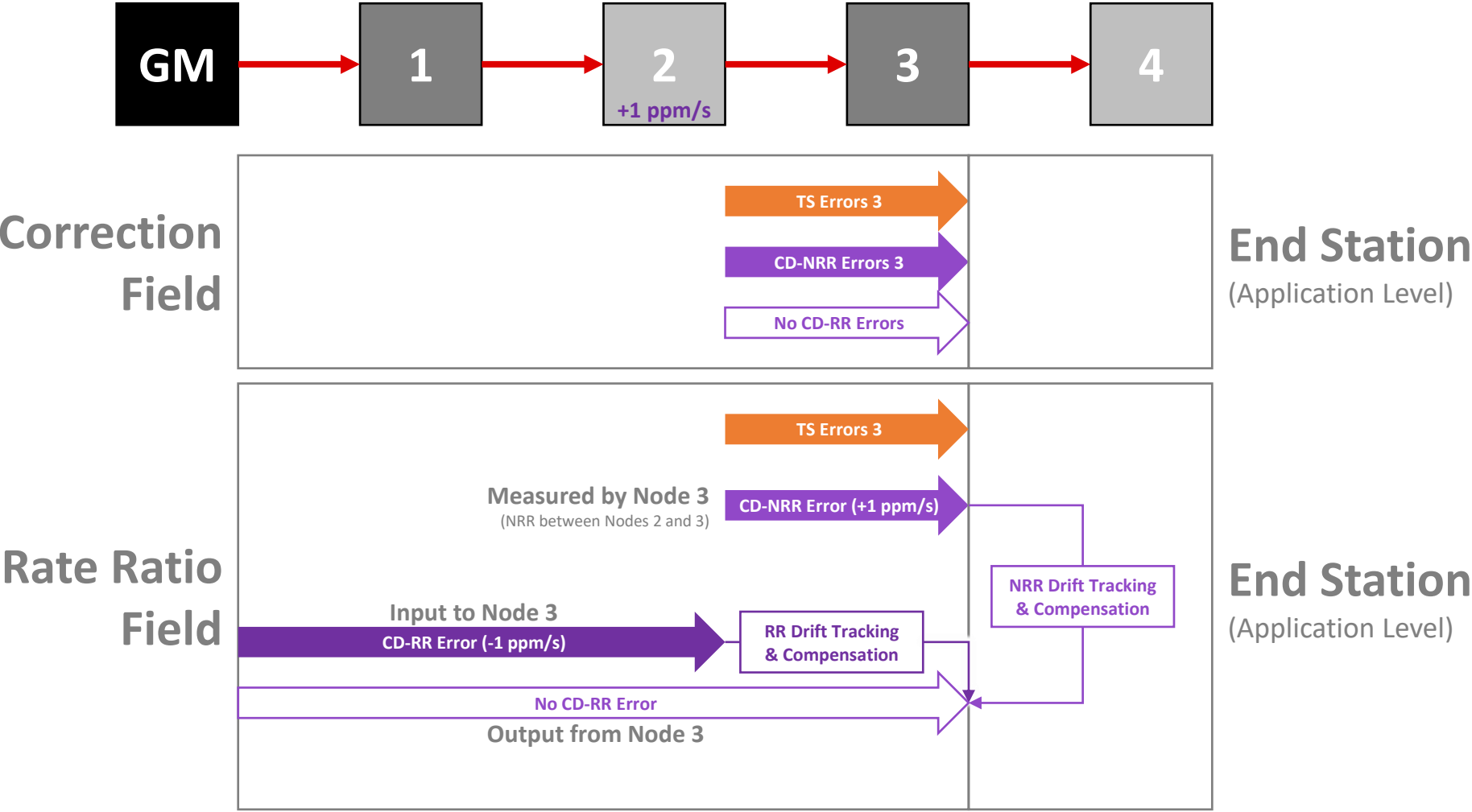
Error Accumulation – Node 3



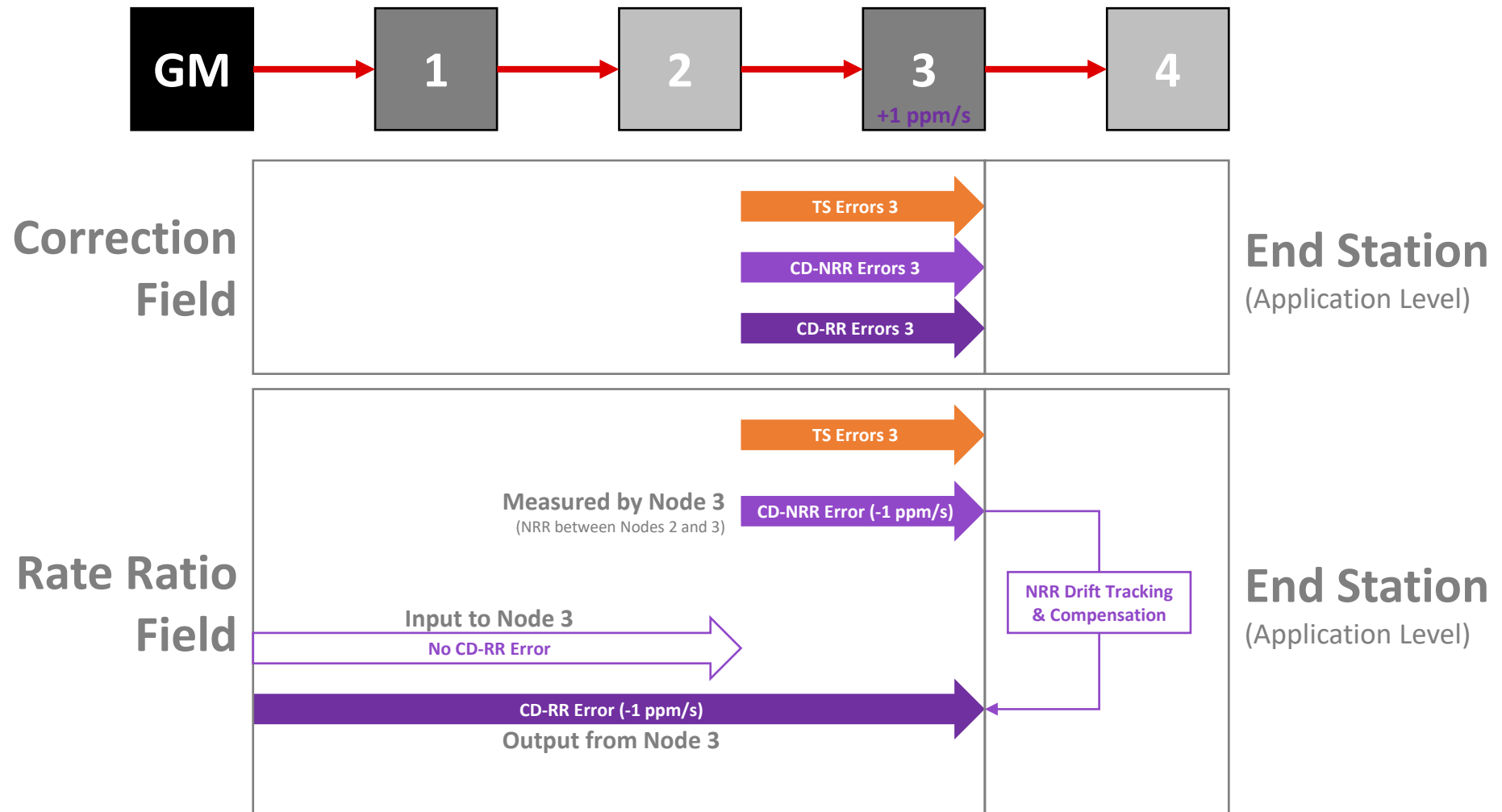
Error Accumulation – Node 3



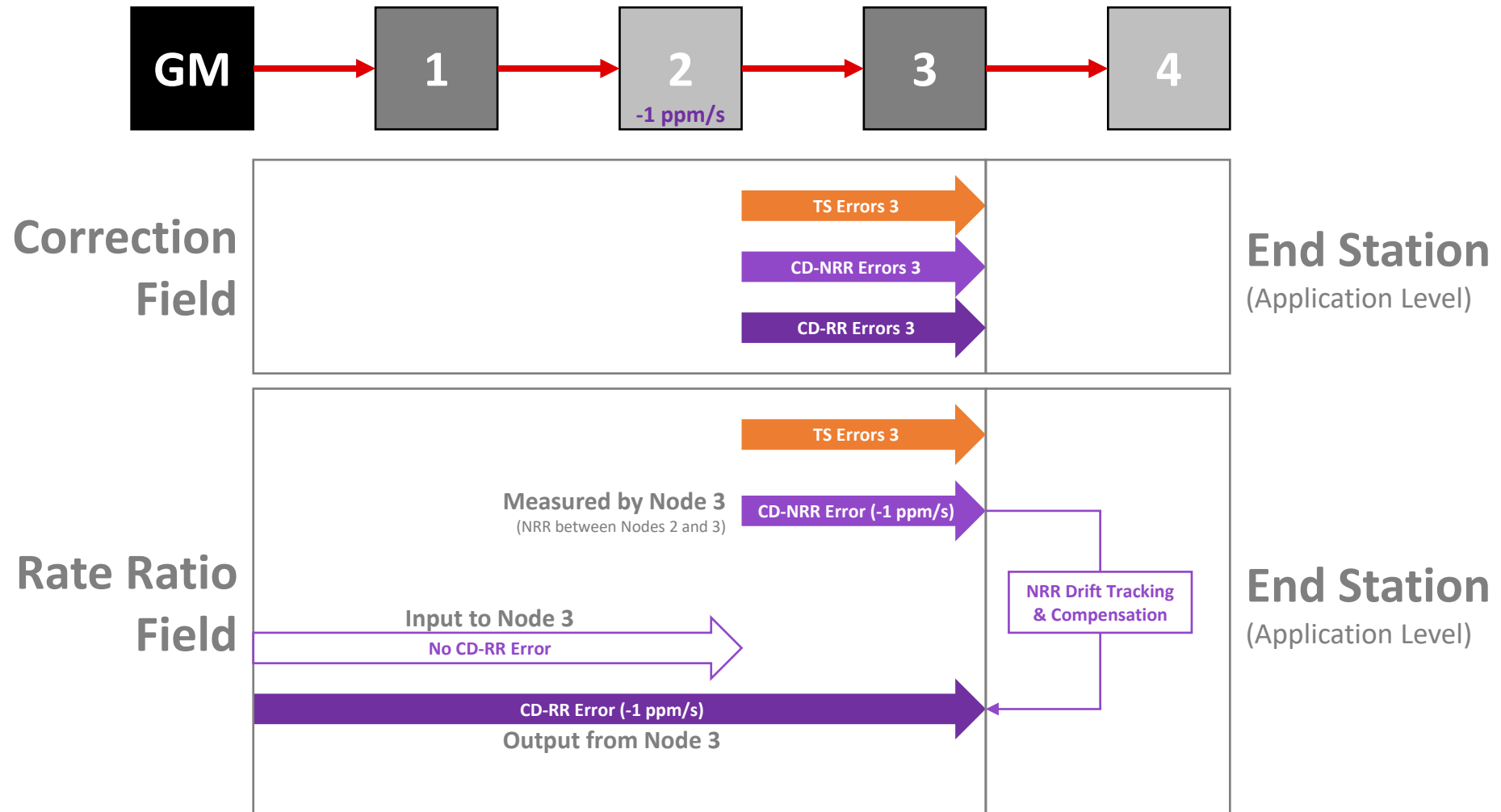
Error Accumulation – Node 3



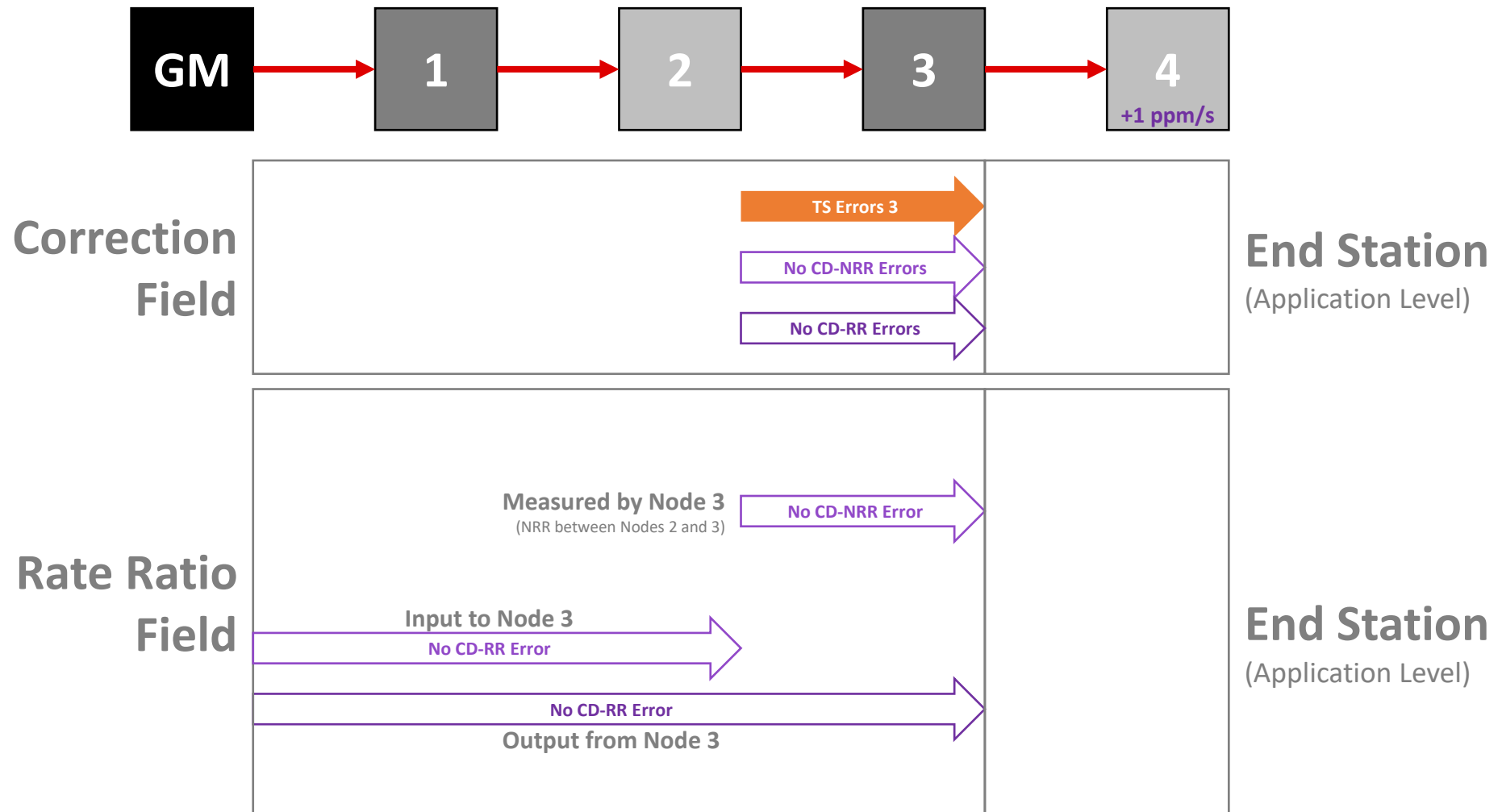
Error Accumulation – Node 3



Error Accumulation – Node 3



Error Accumulation – Node 3



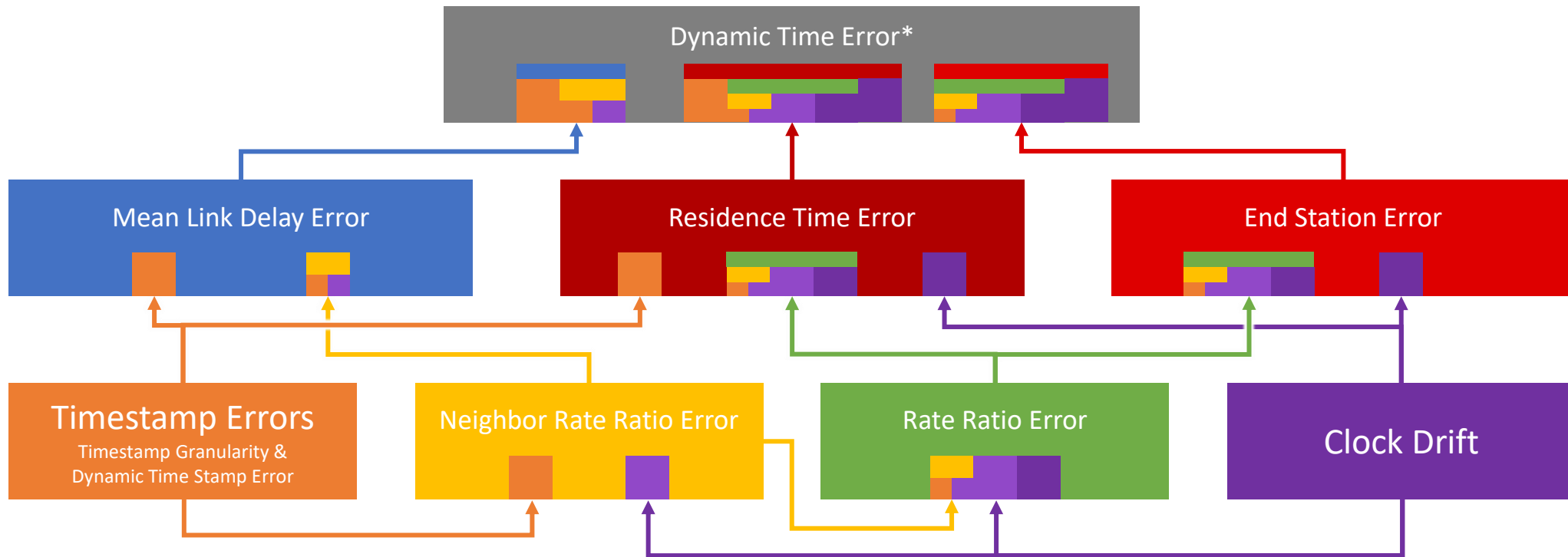
Summary for Individual Node

Input RR Field (ppm/s)	Upstream Node Clock (ppm/s)*	Output RR Field Error Affected By...	Output Correction Field Error Affected By...	Emulates
No Drift	No Drift	TS (Small)	TS (Large)	N/A
+X ppm/s	No Drift	TS (Small) CD-RR	TS (Large) CD-RR	GM Clock Drift (+X ppm/s)
No Drift	-X ppm/s	TS (Small) CD-NRR	TS (Large) CD-NRR	Local Clock Drift (+X ppm/s)
-X ppm/s	+X ppm/s	TS (Small) CD-RR CD-NRR	TS (Large) CD-RR CD-NRR	Upstream Node Clock Drift (+X ppm/s)

60802 Normative Requirements

- System design is for a low-cost, relatively unstable XO (vs. TCXO)
 - Assumes only a portion of temps changing and thus clocks drifting at any one time.
 - Assumes a lot of the Clock Drift error is eliminated via NRR node-to-node cancellation and algorithmic tracking and compensation.
- Can not have a single Time Sync error budget for a device
 - A device might use a TCXO and allocate the entire error budget to Timestamp Error...which is uncorrelated over time (isn't eliminated via NRR node-to-node cancellation) and can't be addressed via algorithmic tracking and compensation. A system of such devices will not meet system design goal.
- Therefore, need to have error budgets for...
 - No clock drift
 - Essentially measures Timestamp Error
 - GM clock drift
 - CD-RR; emulated by varying incoming RR field)
 - To measure effectiveness of RR drift error tracking and compensation
 - Local Clock Drift
 - CD-NRR; emulated by varying upstream node clock without varying incoming RR field)
 - To measure effectiveness of NRR drift error tracking and compensation
- No need for error budget for Upstream Node Clock Drift, as this is a combination of the other two.
- Better to measure latter two (GM & Local Clock) via RR field as this is closer to the errors of interest and limits the noise from Timestamp error

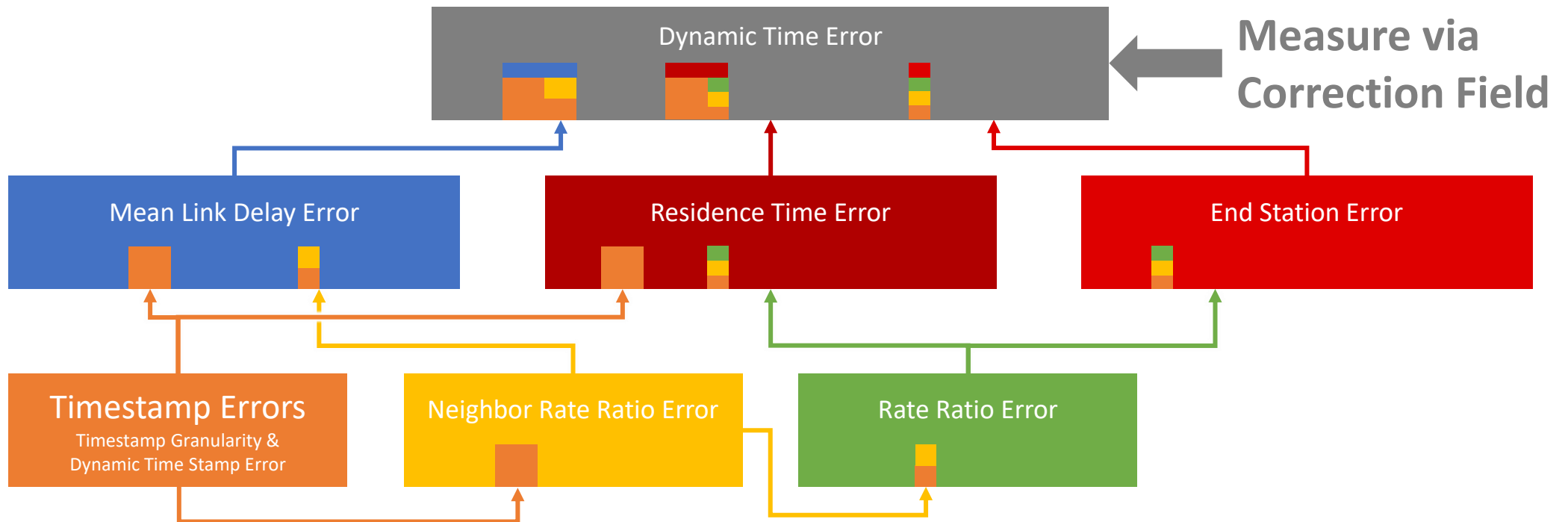
Dynamic Time Sync Error Accumulation



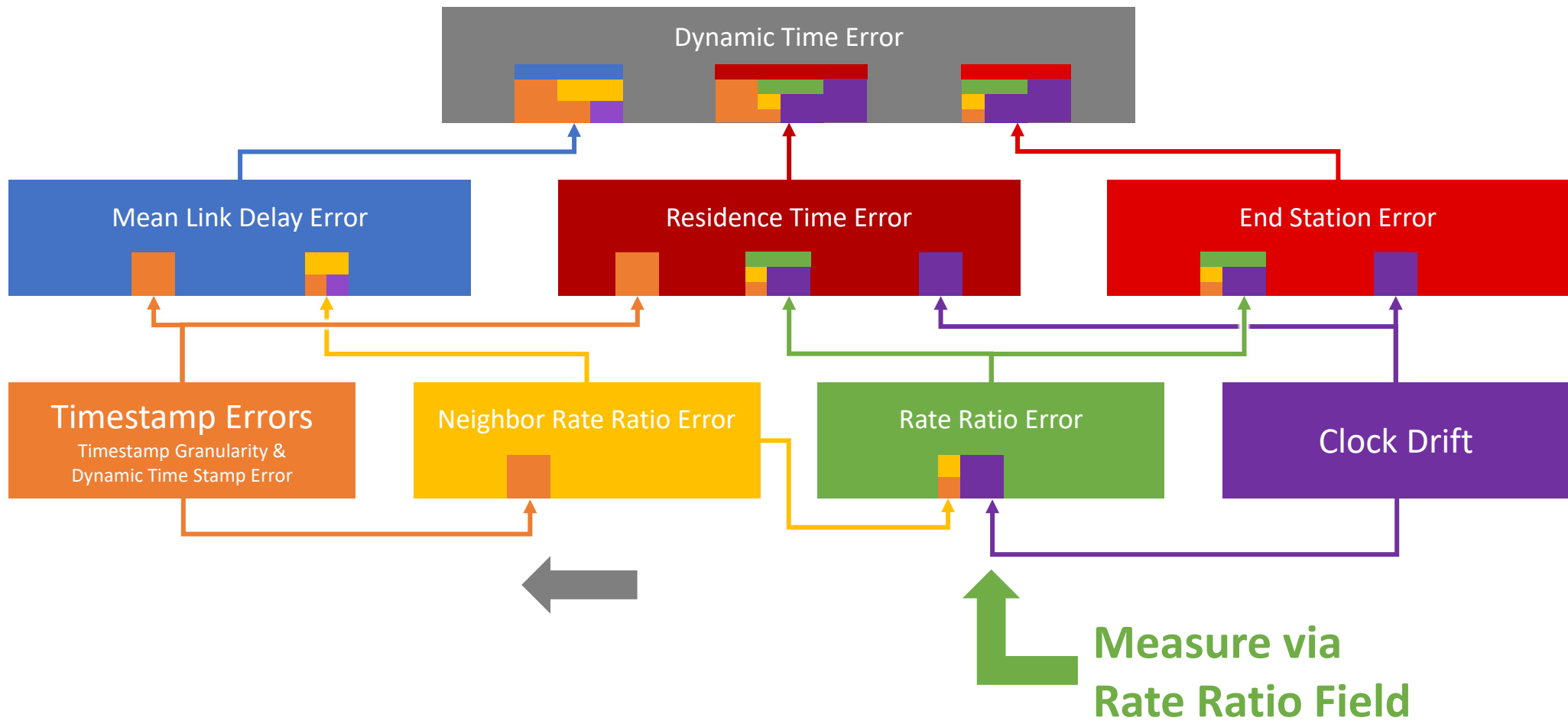
All errors in this analysis are caused by either Clock Drift or Timestamp Errors

*DTE based on protocol messaging only. Total DTE at the application level will also depend on ClockMaster, ClockSlave, ClockSource, Clock Target, etc...

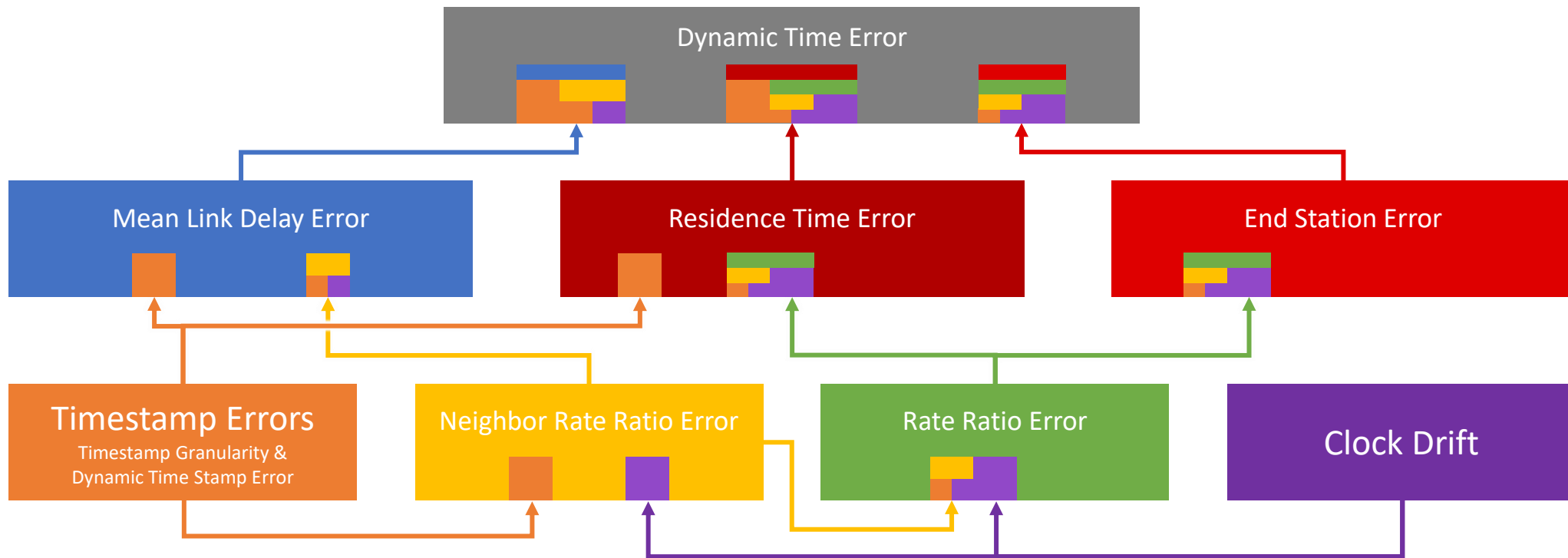
No Clock Drift



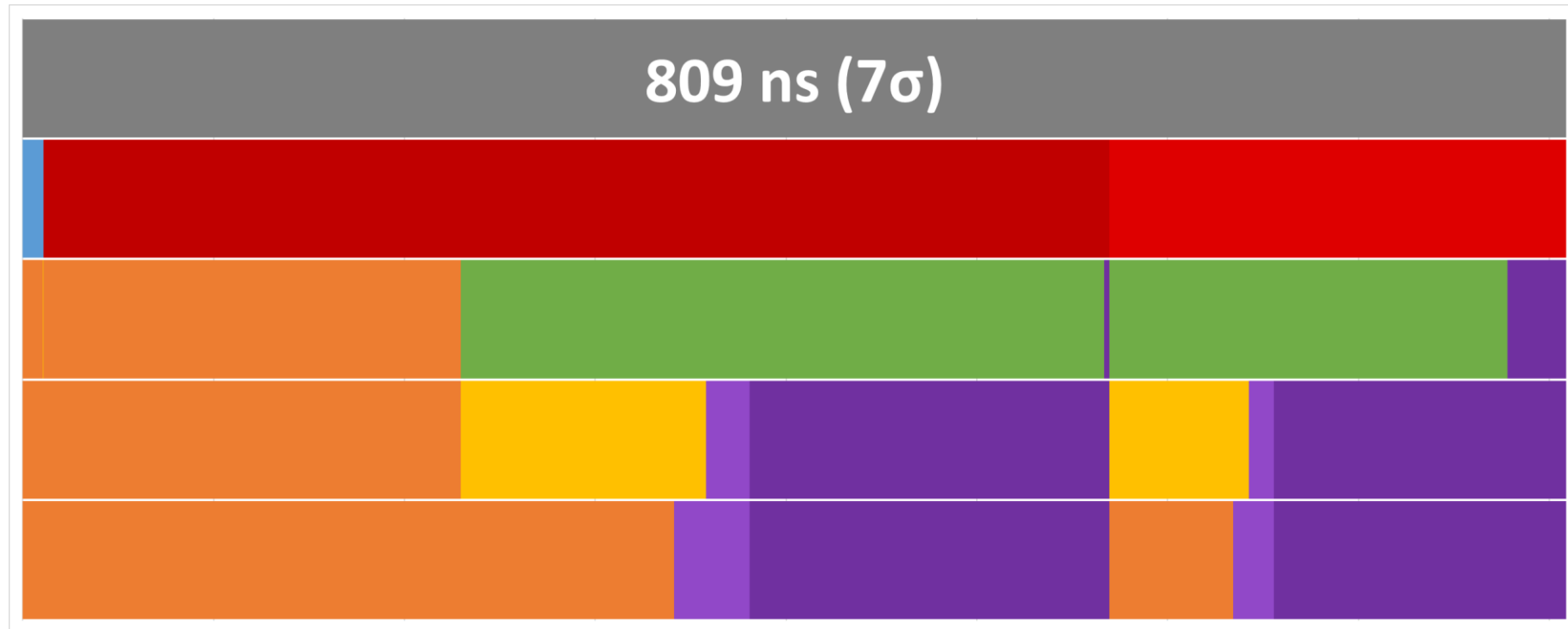
GM Clock Drift



Local Clock Drift



Other Options dTE Breakdown



Normative Requirements

Correction Field, RR & NRR “Noise” Requirements

Topic	Value
Error Generation – No Clock Drift Correction Field Error Stable GM / RR input field (RR) Stable Upstream Node Clock (NRR) Stable temperature (Local Clock)	Error Mean X ns (Constant Time Error) Error Standard Deviation Y ns (Dynamic Time Error)
Error Generation – GM Clock Drift (Emulated) Rate Ratio Field Error GM / RR input field (RR) drifting +2.1 ppm/s Stable Upstream Node Clock (NRR) Stable temperature (Local Clock)	Error Mean X ppm (Constant Time Error) Error Standard Deviation Y ppm (Dynamic Time Error)
Error Generation – Local Clock Drift (Emulated) Rate Ratio Field Error Stable GM / RR input field (RR) Stable Upstream Node Clock (NRR) drifting +2.1 ppm/s Stable temperature (Local Clock)	Error Mean X ppm (Constant Time Error) Error Standard Deviation Y ppm (Dynamic Time Error)

Clock Requirements – 1

Topic	Value
Range of fractional frequency offset relative to the TAI frequency for LocalClock (used for timeReceiver, Grandmaster, or PTP Relay Instance) or Clock Target	± 50 ppm
Range of rate of change of fractional frequency offset for LocalClock (used for timeReceiver, Grandmaster, or PTP Relay Instance)	-1.35 ppm/s to +2.12 ppm/s
Range of rate of change of fractional frequency offset for ClockTarget	± 3 ppm/s

- May split timeReceiver and Grandmaster ppm/s requirement – tighter requirement for Grandmaster.
- Is the LocalClock ppm/s requirement OK? (See next 3 slides.)
- Must be maintained over manufacturer's stated operating conditions (including temperature and temperature ramp ranges)...which 60802 does not specify.

Clock Requirements – 2

Topic	Value
Total range of frequency adjustment for ClockTarget used for Global Time	± 1000 ppm over any observation interval of 1 ms
Total range of frequency adjustment for ClockTarget used for Local Clock	± 250 ppm over any observation interval of 1 ms

- Need to align “Required Values” with comment resolution.

PTP Protocol Requirements – Sync & pDelay Interval

Topic	Value
Nominal Sync Interval (syncInterval) at the Grandmaster	125 ms
Tsync2sync at the Grandmaster	120ms to 130ms
Nominal pDelay Interval (pDelayInterval)	125 ms
Tpdelay2pdelay	120ms to 130ms

- Until now, simulations use...
 - Tpdelay2pdelay:
 - Time Series & most Monte Carlo: uniform distribution 90% - 130% of nominal value (112.5 ms to 162.5 ms)
 - Recent Monte Carlo: uniform distribution 95% - 105% of nominal value (118.75 ms to 131.25 ms)
 - Tsync2sync: Gamma distribution with 90% of messages within 10% of nominal (112.5 ms to 137.5 ms)
- IEEE 1588 requirements...
 - Tsync2sync: 90% of messages within 30% of nominal (87.5 ms to 162.5 ms)
 - Tpdelay2pdelay: minimum 90% of nominal (112.5 ms)
- Note: if we decide not to use pDelayResp messages as part of calculating NRR we may significantly increase the Nominal pDelay Interval.

Notes on PTP Protocol Requirements – Sync & pDelay Interval

- Assumptions:
 - Implementation will be via a 10 ms timer, so 10 ms limits should be used.
 - Nominal values for pDelayInterval and SyncInterval will be the same.
- Nominal values are limited to ..., 31.25 ms, 62.5 ms, 125 ms, 250 ms, etc...
 - Simulations will determine whether 125 ms is the final choice.
- If 125ms is the choice...
 - IEEE 1588 requirement means 120ms is the minimum $T_{\text{pdelay2pdelay}}$ value to remain compliant.
- May increase minimum $T_{\text{pdelay2pdelay}}$ value to remain compliant to 140ms if necessary.

PTP Protocol Requirements – residenceTime & pDelayTurnaround

Topic	Value
Maximum Residence Time (residenceTime)	10 ms
Residence Time Distribution	Mean 5 ms; Standard Deviation 1.8 ms
Sync Follow-up Message	<2.5 ms after Sync Message
Maximum pDelay Turnaround (pDelayTurnaround)	10 ms

- Residence Time with 95% < 6.5 ms is from mean 5 ms, standard deviation 0.8333 ms ($6\sigma = 5$ ms)
 - For recent Monte Carlo simulations we assumed Gaussian distribution, mean 5 ms, standard deviation 0.8333 ms, truncated to 1 ms at the lower end and 10 ms at the upper end.
- Recommendation to move to Residence Time with 95% < 8 ms.
 - For 95% below 8 ms the simulation would use Gaussian distribution, mean 5 ms, standard deviation 1.8 ms, truncated to 1 ms at the lower end and 10 ms at the upper end.
- Sync Follow-up Message timing may be too aggressive. Need more feedback.
- No need for tighter pDelay Turnaround requirement
 - Minimal impact on Mean Link Delay measurement
 - No need for improved timing consistency of pDelayResp messaging if t_{1out} TLV is implemented
- ~~Note: if we decide not to use pDelayResp messages as part of calculating NRR we may significantly increase the nominal pDelayInterval.~~
- Keep pDelayInterval the same as syncInterval to facilitate fast sync lock following change in GM.

Correction Field, RR & NRR “Noise” Requirements

- May want to split accuracy of cable delay measurement vs accuracy of residence time measurement.
 - Or not...might be better to have the expected split in informative text.
- More informative text required to clarify normative requirements.
 - Should look at other examples of how to measure static and dynamic time error from other (ITU, etc...) specs. Don't reinvent the wheel.

Using Sync message and new TLV to calculate NRR

- Normative requirement vs. informative text?
 - What is the new state machine (if there is a new state machine)? Use both pDelayResp & Sync+TLV? Implications of variability (unsynchronised processes)?
- Implications for standby & switching to a new GM?
 - pDelayInterval?
 - How to make the switch, i.e. transition process?

New TLV - Schedule

- Plan to include in a comment on next draft of 802.1ASdm
 - In parallel with 802.1ASdm PAR modification
- Will close on both comment text and PAR modification at Interim session.
- Best if we have a detailed proposed resolution (i.e. message content fully defined) to be included in the comment.
- Schedule? Experts to provide content? Review in this group?

Schedule

- Intent is to have Time Sync contribution to Jordon Woods by Christmas
- Jordon will integrate the contribution into a pre-draft during first two weeks of 2023
- Pre-draft will be reviewed during 802.1 Interim (Baltimore, MA; 15th-20th January) to ensure it addresses all comments

Informative Text

Informative Text

(not a comprehensive list; mainly to identify what isn't normative)

- Assumptions behind normative requirements
- Timestamp Granularity & Dynamic Time Stamp Error
 - Including need for consistent PHY delay
- meanLinkDelay Error Correction
- mNRRsmoothing
 - Using N^{th} previous pDelayResp / TLV information; taking an average of previous A calculations
- NRR drift measurement & compensation
 - Using N^{th} previous pDelayResp / TLV information; taking an average of previous A calculations; going back P messages and doing it again; assuming linearity between two measurements and compensating
- RR drift measurement & compensation – similar to NRR drift measurement & compensation

Discussion

- There is a lot more background to the informative text than we can probably fit into the specification.
- Should this be made easily available to readers somewhere else?
- If so, where?
 - Whitepaper? Somewhere else?
- If so, should it be referenced by the specification?

What Else?

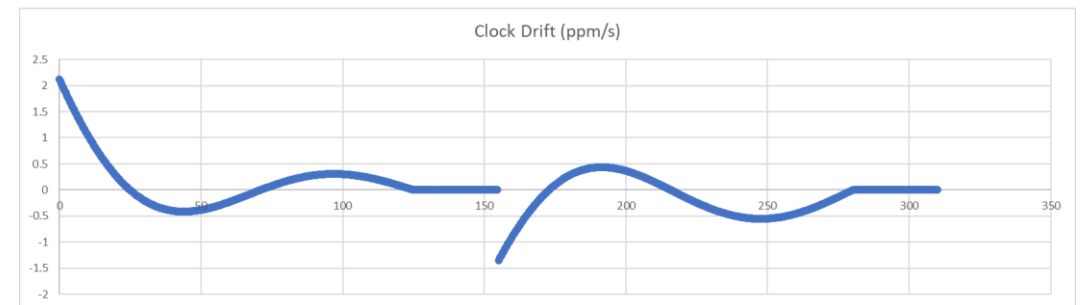
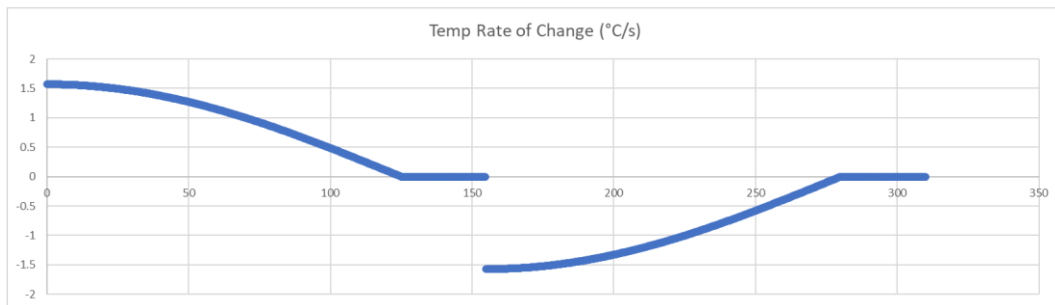
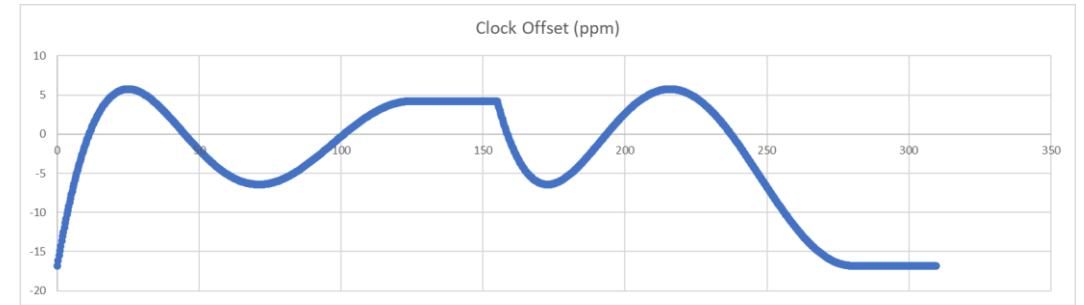
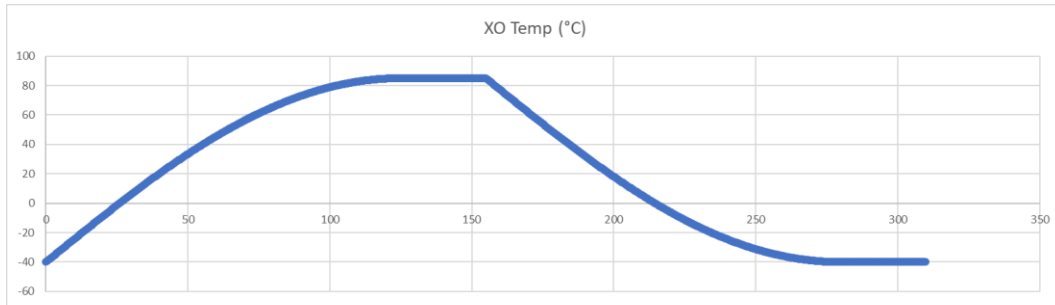
Additional Contribution Areas?

- ClockMaster / ClockSlave & ClockSource / ClockTarget?
- Error model? Dynamic time error vs. Constant time error?
- Clock filtering / control loop (independent of implementation)
 - Must ensure comments are addressed

Thank you!

Backup

Clock Drift Example – Half-Sinusoidal Temperature Ramp: 125s \updownarrow



Inputs	
Temp Max	85°C
Temp Min	-40°C
Temp Ramp Period	125s
Temp Hold	30s

Temp Rate of Change	
MAX	1.57°C/s
MIN	-1.57°C/s

Clock Drift	
MAX	2.12ppm/s
MIN	-1.35ppm/s