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A New Generation 16-core Processor for Supercomputing

SPARC64™ IXfx

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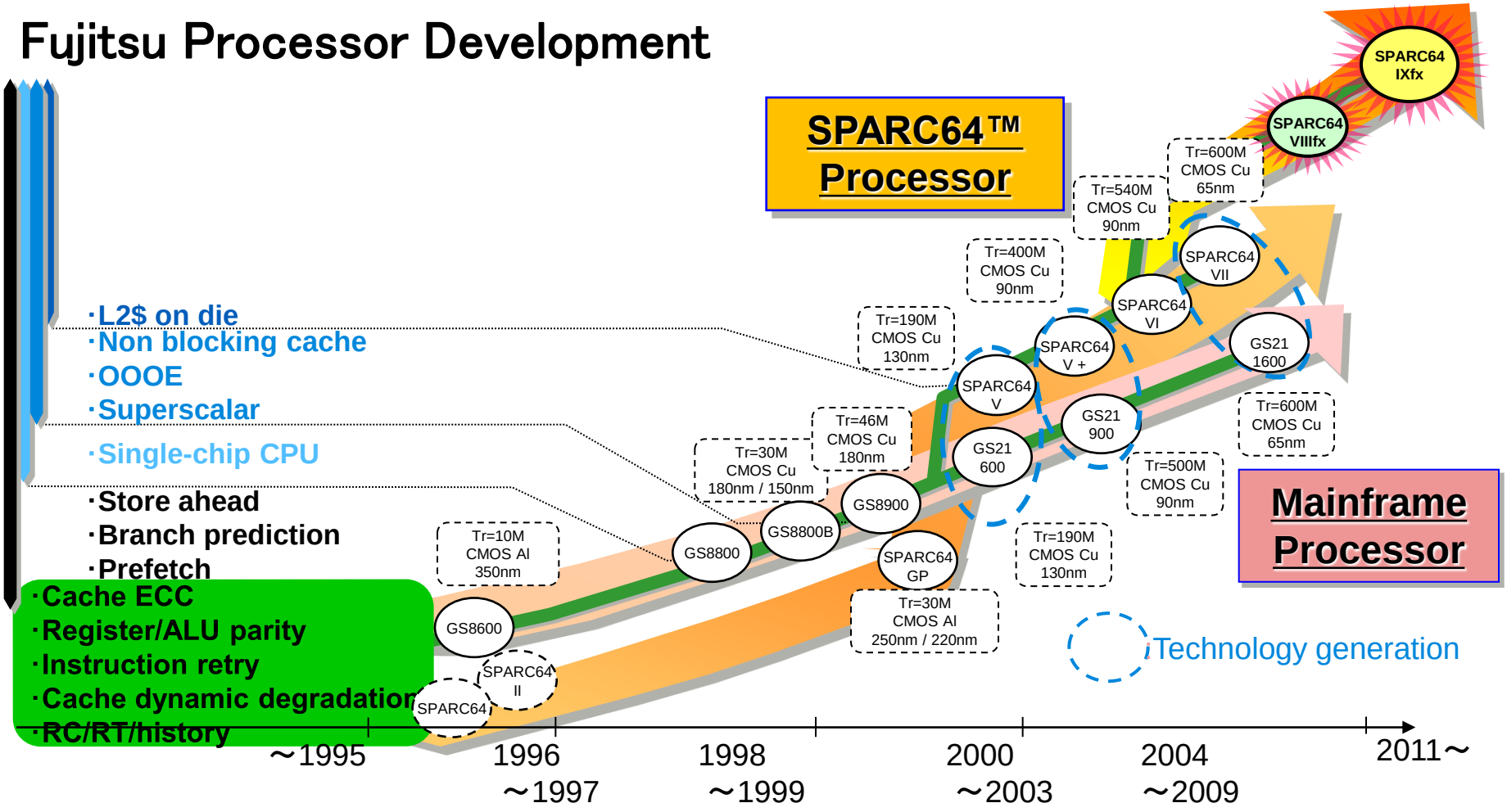
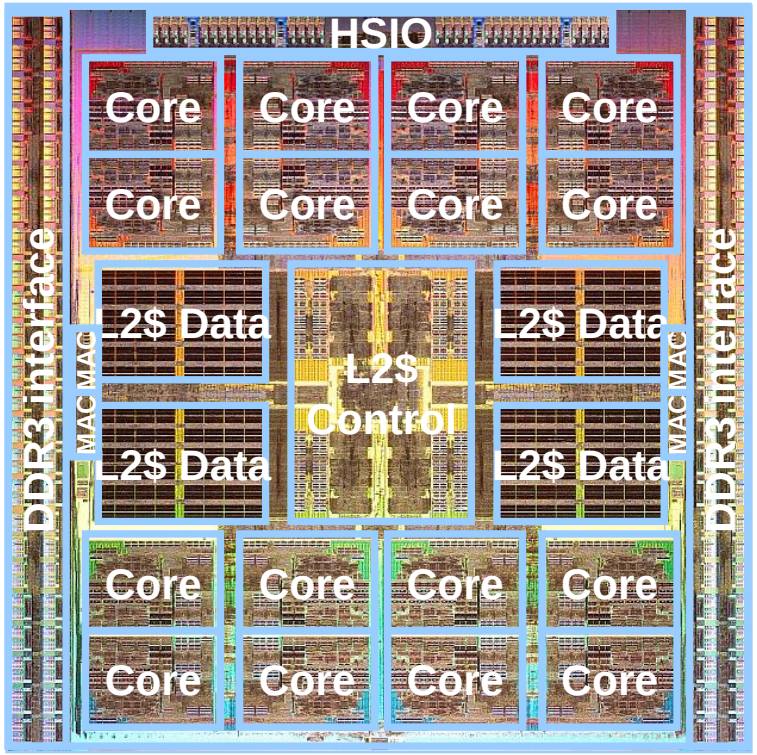
Fujitsu Processor Development



SPARC64™ IXfx

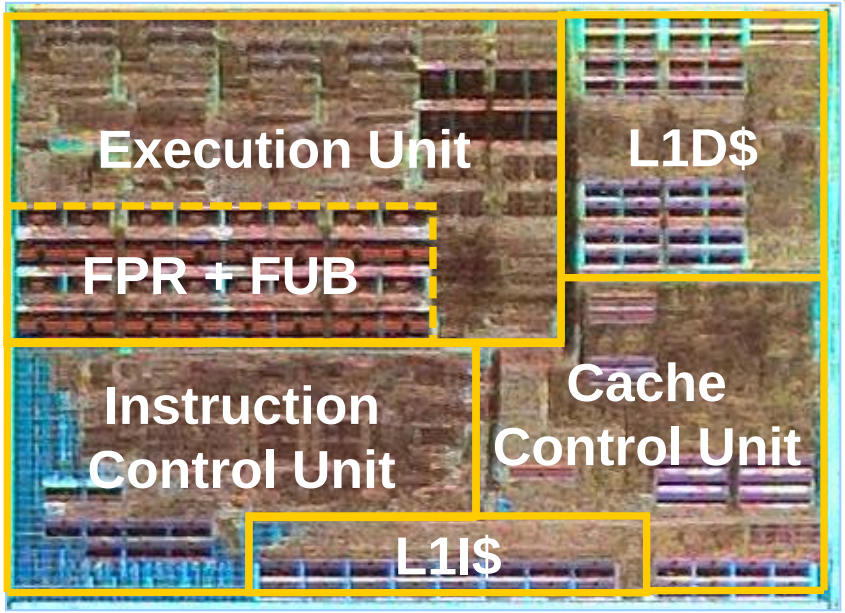
- Inherited features from SPARC64™ VIIIfx
  - High performance
    - HPC-ACE
    - Embedded memory controller
    - Hardware barrier mechanism
  - Low power
    - Moderate frequency
    - Dynamic/Leakage power reduction
  - High reliability
    - RAS features
- New features
  - Doubled number of cores
  - Doubled size of L2$



SPARC64™ IXfx

SPARC64™ IXfx Core Overview

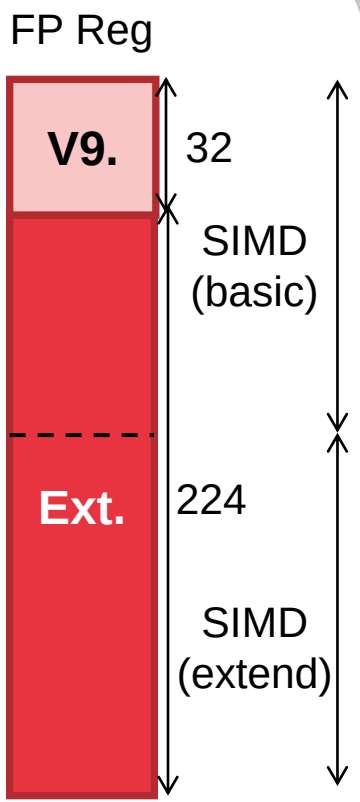
- Instruction control Unit
  - Controls the fetch, issue, and completion of instruction
- Execution unit
  - Performs integer and floating-point operations
  - Occupy the large part of a core
  - Many floating-point registers (FPR + FUB)
- Storage unit (L1D/I cache, cache control unit)
  - Executes load/store instructions



SPARC64™ IXfx Core

HPC-ACE 1/2

- Enhanced instruction set for the SPARC-V9 instruction set architecture
- Extended number of registers
  - Floating-point registers are extended the number from 32 to 256
    - ➔ Enable to extract parallelism
    - ➔ Reduce spill/fill overhead
- SIMD operation
  - Performs multiple data operation by a single instruction
  - Each core executes 2 SIMD operation per clock cycle
    - ➔ Each core executes 8 floating-point operations per clock cycle



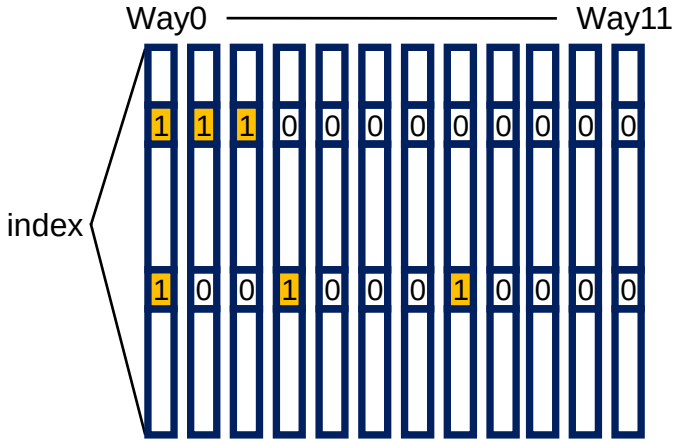
HPC-ACE 2/2

- Software-controllable cache (sector cache)
  - Software categorizes the cache data into 2 groups (sectors)

    For example:
    - sector 0: Less frequently reused data
    - sector 1: Frequently reused data
  - Combines the advantages of both the cache and local memory
    - Hardware controls as a cache memory
    - Software can control as a local memory
- Other features
  - FP Trigonometric functions
  - FP Reciprocal Approximation of divide/Square-root
  - FP Minimum and Maximum
  - Conditional operation

L2 Cache structure

Ex) Sector0:Sector1=3:9



SPARC64™ VIIIfx / IXfx Specifications

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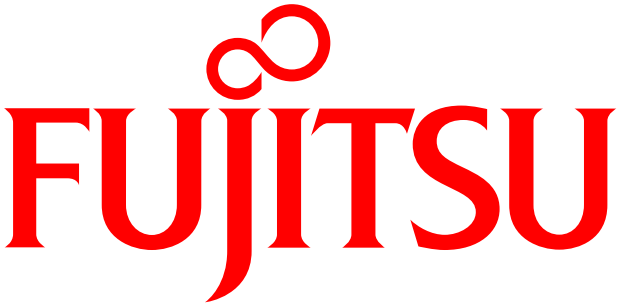
		SPARC64™ VIIIfx	SPARC64™ IXfx
Number of cores		8 cores	16 cores
Clock frequency		2 GHz	1.848 GHz
Cache	L1	I: 32KB/core, D: 32KB/core	I: 32KB/core, D: 32KB/core
	L2	6MB (Shared cache)	12MB (Shared cache)
Peak performance		128 Gigaflops	236.5 Gigaflops
Memory throughput		64 GB/s	85 GB/s
Power consumption		58W	110W
Process		45 nm	40 nm
Die size		22.7 mm × 22.6 mm	21.9 mm × 22.9 mm
Number of transistors		Approximately 760 million	Approximately 1.87 billion



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