

Electrical Engineering Department University of Delaware
Technical Report 97-3-3 March 1997

Clock Discipline Algorithms for the Network Time Protocol Version 4

David L. Mills

Abstract

This report describes the analysis, implementation and performance of engineered algorithms to discipline a computer clock to a source of standard time, such as a GPS receiver or another computer synchronized to such a source. The algorithms are designed for the Network Time Protocol (NTP) Version 4, the successor to NTP Version 3, which is in widespread use to synchronize computer clocks in the global Internet. The report includes an overview of the new NTP architecture and process decomposition as related to the clock discipline algorithm, which is implemented as a hybrid phase/frequency-lock feedback loop. An extensive engineering analysis of this algorithm is presented along with the results of a detailed simulation to evaluate and validate its performance using both synthetic data and real measurements with Internet time servers in Europe, Asia and the Americas.

Keywords: computer network time synchronization, clock discipline algorithm, oscillator error modelling, feedback control loop

Sponsored by: DARPA Information Technology Office Contract DABT 63-95-C-0046, NSF Division of Network and Communications Research and Infrastructure Grant NCR 93-01002, Northeastern Center for Electrical Engineering Education Contract A303 276-93, Army Research Laboratories Cooperative Agreement DAA L01-96-2-002, and Digital Equipment Corporation Research Agreement 1417.

Table of Contents

1.	Introduction.....	1
2.	Network Time Protocol.....	2
3.	NTP Version 4 Architecture and Algorithms.....	4
4.	Clock Discipline Algorithm.....	5
4.1	Hybrid FLL/PLL Combining Algorithm.....	9
4.2	Poll-Adjust Algorithm.....	11
4.3	Clock State Machine	13
5.	Performance Evaluation.....	16
5.1	Allan Deviation Experiments	18
5.2	Performance Using Synthetic Noise Sources.....	24
5.3	Performance Using Real Data	28
5.4	Performance with Real Data over Time	29
6.	Conclusion	30
7.	References.....	31
8.	Appendix A. NTP Simulator	32

List of Figures

Figure 1.	NTP Architecture	3
Figure 2.	Clock Discipline Algorithm.....	6
Figure 3.	FLL/PLL Prediction Functions	7
Figure 4.	USNO Weight Functions	11
Figure 5.	USNO Raw/Filtered Data Comparison.....	12
Figure 6.	Poll Interval Adjustment	13
Figure 7.	Clock State Machine	14
Figure 8.	Initial Transient Adaptation - Network Peer.....	15
Figure 9.	Initial Transient Adaptation - Telephone Modem Peer.....	16
Figure 10.	PPS Frequency	19
Figure 11.	LAN Frequency	20
Figure 12.	Comparison of PPS and LAN Data	20
Figure 13.	Allan Deviation - Combined Data	22
Figure 14.	Comparison of Raw and Filtered USNO Data.....	23
Figure 15.	Comparison of Real and Synthetic Phase Noise.....	23
Figure 16.	Allan Deviation Phase Noise Parameters.....	24
Figure 17.	Phase and Frequency Noise Comparisons With PLL and FLL	25
Figure 18.	IEN Phase Noise	26
Figure 19.	PLL Mode Standard Error by Source - Synthetic Noise.....	27
Figure 20.	Hybrid Mode Standard Error by Source - Synthetic Noise	27
Figure 21.	PLL Mode Standard Error by Source - Real Data	28

Figure 22. Hybrid Mode Standard Error by Source - Real Data.....29
Figure 23. Clock Offsets for PPS Reference Source.....29