TECHNICAL REPORT

TR-286
Testing of Metallic Line Testing (MELT) functionality on xDSL Ports

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Comments or questions about this Broadband Forum Technical Report should be directed to info@broadband-forum.org.

Editor	Aleksandra Kozarev	Lantiq
Metallic Transmission Working Group Chair	Les Brown	Lantiq
Vice Chairs	Massimo Sorbara Lincoln Lavoie	Ikanos UNH
Chief Editor	Michael Hanrahan	Huawei Technologies

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Executive Summary

TR-286 describes test cases required for verification of the Metallic Line Testing entity (MELT) according to Recommendation ITU-T G.996.2 and collocated with the DSLAM (Digital Subscriber Line Access Multiplexer). In addition, TR-286 provides testing methodology for xDSL systems, such as ITU-T G.992.5 (ADSL2plus), G.993.2 (VDSL2) and G.991.2 (SHDSL), in combination with MELT functionality.

1 Purpose and Scope

1.1 Purpose

TR-286 specifies a set of tests to be performed to assure the functionality of the MELT functions (test parameters) and accuracy as defined in Recommendation ITU-T G.996.2 Annex E (MELT-PMD) and Annex F (MELT-P).

1.2 Scope

TR-286 describes test cases required for verification of the Metallic Line Testing entity (MELT) according to Recommendation ITU-T G.996.2, Annex E (MELT-PMD) and F (MELT-P) that is collocated with the DSLAM (Digital Subscriber Line Access Multiplexer). Additionally, it focuses on xDSL data transmission tests and stability criteria in combination with MELT functions. xDSL operation is specified by ITU-T Recommendations G.992.3 (ADSL2), G.992.5 (ADSL2plus), G.993.2 (VDSL2), and G.991.2 (SHDSL).

The equipment under test includes network-end equipment (such as a DSLAM), Metallic Line testing entity (MELT), MELT specific test circuits (MTC) and customer-end equipment (such as a CPE). It is assumed that the individual DSL transceivers (DSLAM and CPE) also pass applicable DSL-specific testing requirements specified in TR-100 and TR-105 (ADSL2/ADSL2plus), TR-114 and TR-115 (VDSL2), and TR-60 (SHDSL).

2 References and Terminology

2.1 Conventions

In this Technical Report, several words are used to signify the requirements of the specification. These words are always capitalized. More information can be found be in RFC 2119 [10].

SHALL	This word, or the term "REQUIRED", means that the definition is an absolute requirement of the specification.
SHALL NOT	This phrase means that the definition is an absolute prohibition of the specification.
SHOULD	This word, or the term "RECOMMENDED", means that there could exist valid reasons in particular circumstances to ignore this item, but the full implications need to be understood and carefully weighed before choosing a different course.
SHOULD NOT	This phrase, or the phrase "NOT RECOMMENDED" means that there could exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications need to be understood and the case carefully weighed before implementing any behavior described with this label.
MAY	This word, or the term "OPTIONAL", means that this item is one of an allowed set of alternatives. An implementation that does not include this option SHALL be prepared to inter-operate with another implementation that does include the option.

2.2 References

The following references are of relevance to this Technical Report. At the time of publication, the editions indicated were valid. All references are subject to revision; users of this Technical Report are therefore encouraged to investigate the possibility of applying the most recent edition of the references listed below.

A list of currently valid Broadband Forum Technical Reports is published at www.broadband-forum.org.

Document		Title	Source	Year
[1]	TR-100 Issue 2	*ADSL2/2plus Performance Test Plan*	BBF	2012
[2]	TR-105 Issue 2	*ADSL2/2plus Functionality Test Plan*	BBF	2012
[3]	TR-114	*VDSL2 Performance Test Plan, including all in force errata and amendments*	BBF	2009
[4]	TR-115	*VDSL2 Functionality Test Plan*	BBF	2012

	Issue 2			
[5]	G.996.2	*Single-ended line testing for digital subscriber lines (DSL), including all in force errata and amendments*	ITU-T	2009
[6]	G.992.5	*Asymmetric Digital Subscriber Line (ADSL) transceivers - Extended bandwidth ADSL2 (ADSL2plus), including all in force errata and amendments*	ITU-T	2009
[7]	G.993.2	*Very high speed subscriber line transceivers 2 (VDSL2), including all in force errata and amendments*	ITU-T	2011
[8]	G.991.2	*Single-pair high speed digital subscriber line (SHDSL) transceivers, including all in force errata and amendments*	ITU-T	2003
[9]	G.997.1	*Physical Layer Management for Digital Subscriber Line (DSL) Transceivers, including all in force errata and amendments*	ITU-T	2009
[10]	RFC 2119	*Key words for use in RFCs to Indicate Requirement Levels*	IETF	1997

2.3 Definitions

The following terminology is used throughout this Technical Report.

GND	Ground
ID tone	Pair identification tone
IDLE state	a) MELT entity is inactive but ready to start the PMD measurements b) DSL port powered but no data transmitted
RING	RING wire (in some countries also known as a-wire, B-wire) is negative with respect to the TIP wire when the pair-identification tone is turned on. This definition MUST be used consistently for all MELT tests.
Showtime state	DSLAM and CPE trained up to the point of passing data
Sync state	Showtime state
TIP	TIP wire (in some countries also known as b-wire, A-wire) is positive with respect to the RING wire when the pair-identification tone is turned on. This definition MUST be used consistently for all MELT tests

2.4 Abbreviations

This Technical Report uses the following abbreviations:

ATU	ADSL2/2plus Transceiver Unit
ATU-C	ATU at the DSLAM
ATU-R	ATU at the CPE
CTN	Composed MELT Test Network
CV (-C, -CFE)	Code Violation
ES (-L, -LFE)	Error Second
FS	Far-end Signature
FVAC	Foreign Voltage AC Source

FVDC	Foreign Voltage DC Source
MELT	Metallic line testing entity
MELT-P	MELT - Processing
MELT-PMD	MELT - Physical Medium Dependent
MTC	MELT specific Test Circuitry
SES (-L, -LFE)	Severely Errored Second
STU	SHDSL Transceiver Unit
STU-C	STU at the DSLAM
STU-R	STU at the CPE
TCPAM	Trellis Coded Pulse Amplitude Modulation
VTU	VDSL2 Transceiver Unit
VTU-O	VTU at the DSLAM
VTU-R	VTU at the CPE

3 Technical Report Impact

3.1 Energy Efficiency

TR-286 has no impact on energy efficiency.

3.2 IPv6

TR-286 has no impact on IPv6.

3.3 Security

TR-286 has no impact on security.

3.4 Privacy

TR-286 has no impact on privacy.

4 General Testing Requirements

4.1 System Under Test (SUT) Settings

For MELT testing the following settings are applicable to VDSL2 [7], ADSL2plus [6] and SHDSL [8] ports.

For VDSL2 ports, the following settings SHALL be used:

- VDSL2 band defined in Table 1/TR-115 [4]
- Common line settings defined in Section 4.2.2.1/TR-115
- Specific line setting RA_I_150_150 defined in Table 11/TR-115

For ADSL2plus ports, the following settings SHALL be used:

- Common line settings defined in Table 4-1/TR-105 [2]
- Specific test profiles A2P_RA_I_30000k, B2P_RA_I_30000k or J2P60_RA_I_30000k defined in Table 1, depending on the operation mode of the system under test
- General line settings I-16/2 defined in Table 4.3 in TR-105

Table 1: Specific Test Profiles

Specific Test Profile	General line setting DS	General line setting US	XTSE	RA-Mode	DS net data rate (kbit/s) (max-min)	US net data rate (kbit/s) (max-min)
A2P_RA_I_30000k	I-16/2	I-16/2	G.992.5 Annex A	AT_INIT	30000-32	2016-32
B2P_RA_I_30000k	I-16/2	I-16/2	G.992.5 Annex B	AT_INIT	30000-32	2016-32
J2P60_RA_I_30000k	I-16/2	I-16/2	G.992.5 Annex J (ADLU-60)	AT_INIT	30000-32	4032-32

For SHDSL ports, the following profiles SHALL be used:

1.TCPAM-16

- Symmetric PSD as defined in G.991.2 [8]
- 16-TCPAM modulation
- Fixed data rate set to 384kbs, 512kbps, 1024kbps and 2048kbps
- Line probe (PMMS) disabled

2. TCPAM-32

- Symmetric PSD as defined in G.991.2
- 32-TCPAM modulation
- Fixed data rate set to 2560kbps, 4096kbps and 5696kbs
- Line probe (PMMS) disabled

No special SUT configuration for MELT testing is needed unless otherwise stated in the related test case. MELT functionality MUST be available with the initial setup. The xDSL configuration SHALL NOT have impact on the MELT functionality.

4.2 Test Plan Passing Criteria

For each test case, the actual values of components in the applicable MELT specific test circuitry (MTC) SHALL be determined by a measuring device (e.g. multimeter), prior to performing any MELT test. The maximum deviation of each component of the MTC from its nominal value SHALL meet the required tolerance limits defined in Section 4.4. Also, the measuring device SHALL meet the required accuracy limits as defined in Section 4.4.

The pass/fail criterion is defined on a per test case basis and it SHALL take into consideration the following three elements: the actual value of the MTC, the accuracy of the measuring device and the accuracy of the MELT entity.

4.3 Test Setup

A typical test setup for MELT testing consists of three elements shown in Figure 1: DSLAM, Metallic Line Testing entity (MELT) and MELT specific test circuits (MTC). The MTC (Resistor, Capacitor, DC foreign voltage source (FVDC) and AC foreign voltage source (FVAC)) is connected either between TIP and RING, TIP and Ground (GND) or RING and GND. Test setup for the far-end signature identification is shown in Figure 2. The Far-end signatures (FS) SHALL be connected only between TIP and RING.

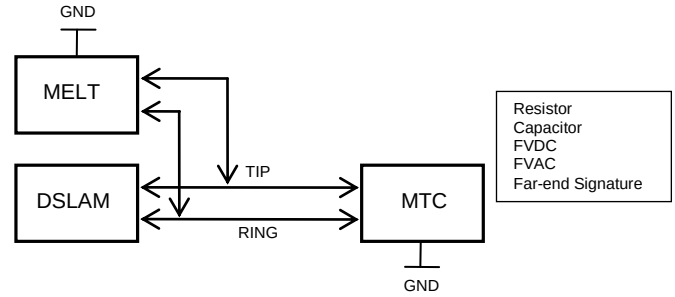

Figure 1: Test setup for MELT testing

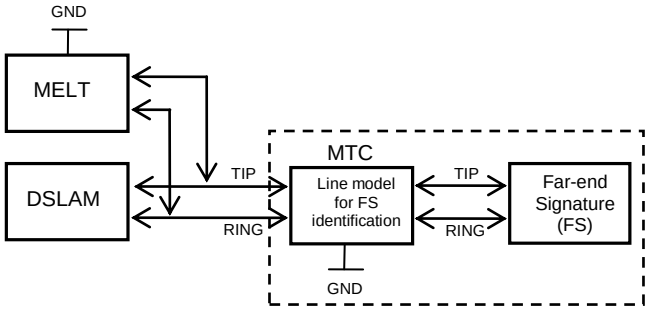

Figure 2: **Test setup for Far-end Signature identification**

Test setup for testing xDSL systems, such as ADSL2plus, VDSL2 and SHDSL, in combination with MELT functionality is shown in Figure 3. It contains the MELT entity and MTC, and a typical test configuration for testing DSL systems, defined for example in TR-105 [2] or TR-115 [4].

Figure 3 shows a typical test setup for testing MELT impact on the same pair SHDSL, ADSL2/2plus and VDSL2 system.

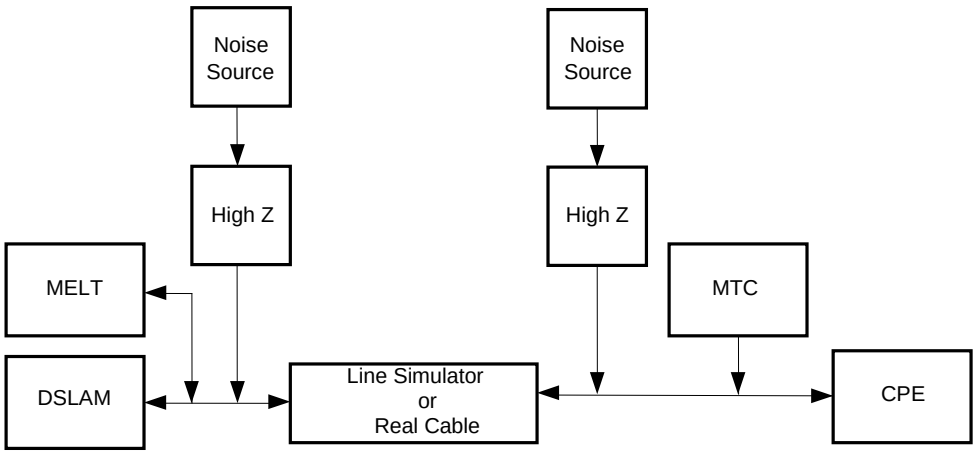

Figure 3: Test setup for testing DSL system in combination with MELT

NOTE: MTC is connected as defined in Figure 1.

4.4 MELT specific test circuits

This section defines the MELT specific test circuits, including the required tolerances of the single components and the accuracy of the measuring device used to determine their actual values (e.g. a multimeter).

See also Section 4.2 for detailed explanation.

4.4.1 Test Resistor

Test resistor is shown in Figure 4 with the appropriate values listed in Table 2. The resistors used to validate the MELT testing procedures SHALL be of a large enough wattage or a low enough thermal coefficient to prevent a resistance variation greater than 0.1% due to self-heating during the testing execution.

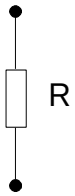

Figure 4: Test Resistor

Table 2: Test Resistors Values

Resistor	Nominal value	Multimeter accuracy
R1	10 Ω ± 5 %	± 1 Ω
R2	120 Ω ± 5 %	± 1 %
R3	270 Ω ± 5 %	± 1 %
R4	600 Ω ± 5 %	± 1 %
R5	1 kΩ ± 5 %	± 1 %

R6	47 kΩ ± 5 %	± 1 %
R7	100 kΩ ± 5 %	± 1 %
R8	470 kΩ ± 5 %	± 1 %
R9	1 MΩ ± 5 %	± 1 %
R10	4,7 MΩ ± 5 %	±1 %
R11	6,8 MΩ ± 5 %	± 1 %
R12	10 MΩ ± 5 %	± 1 %
R13	OPEN	

4.4.2 Test Capacitor

Test capacitor is shown in Figure 5 with the appropriate values listed in Table 3. The capacitors used to validate the MELT testing procedures SHALL be of a type for which the apparent capacitance does not change as a function of the AC or DC voltage applied to them. Otherwise, correlation between the MELT results and the multimeter results may not be possible due to the use of different testing voltages.

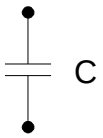

Figure 5: Test Capacitor

Table 3: Test Capacitors Values

Capacitor	Nominal value	Multimeter accuracy
C1	OPEN	
C2	10 nF ± 5 %	± 1nF
C3	22 nF ± 5 %	± 1nF
C4	47 nF ± 5 %	± 1nF
C5	100 nF ± 5 %	± 1%
C6	470 nF ± 5 %	± 1%
C7	1 µF ± 5 %	± 1%
C8	4,7µF ± 5 %	± 1%

4.4.3 Foreign Voltage Source

Foreign voltage DC source is shown in Figure 6 with the appropriate values listed in Table 4. The voltage source used to validate the MELT testing procedures SHALL be able to sink or source any current that may appear during the testing execution while maintaining a constant output voltage, except for the normal voltage drop across its source resistance.

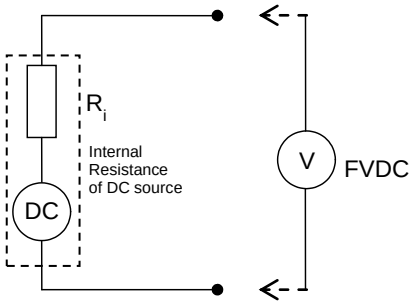

Figure 6: Foreign Voltage DC Source

Table 4: Foreign Voltages DC Source Values

FVDC	Nominal value	Multimeter accuracy
FVDC1	OPEN	
FVDC2	20 V	± 0.5 V
FVDC3	115 V	± 1 %
FVDC4	125 V	± 1 %
FVDC5	180 V	± 1 %
FVDC6	250 V	± 1 %
FVDC7	- 20 V	± 0.5 V
FVDC8	- 48 V	± 1 %
FVDC9	- 96 V	± 1 %
FVDC10	- 115 V	± 1 %
FVDC11	- 125 V	± 1 %
FVDC12	- 180 V	± 1 %
FVDC13	- 250 V	± 1 %

Each nominal value of the DC voltage (FVDC) SHALL be verified by means of a measuring device (V) and if necessary adjusted at the output of the DC voltage source, before performing any MELT Voltage test.

Foreign voltage AC source is shown in Figure 7 with the appropriate values listed in Table 5.

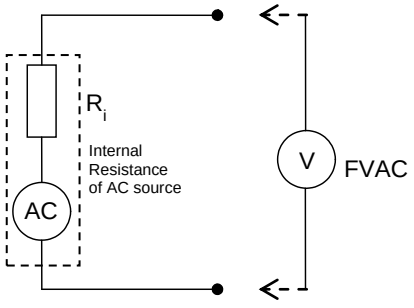

Figure 7: Foreign Voltage AC source

Table 5: Foreign Voltages AC Source Values

FVAC	Nominal value	Multimeter accuracy
FVAC1	OPEN	
FVAC2	20 Vrms	± 0.5 Vrms
FVAC3	47 Vrms	± 0.5 Vrms
FVAC4	53 Vrms	± 1 %
FVAC5	160 Vrms	± 1 %
FVAC6	250 Vrms	± 1 %
NOTE: frequency of the foreign voltage AC source is 16 2/3, 25, 50 or 60 Hz. Multimeter accuracy is ±0.1 Hz.		

Each nominal value of the AC voltage (FVAC) SHALL be verified by means of a measuring device (V) and if necessary adjusted at the output of the AC voltage source, before performing any MELT Voltage test.

4.4.4 Far-end Signature

Two types of the Far-end signature (FS) are shown in Figure 8 and Figure 9, with appropriate components listed in Table 6 and Table 7.

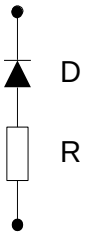

Figure 8: Far-end Signature type DR

Table 6: Components of the Far-end Signature type DR

	Nominal value	Multimeter accuracy
R	470 kΩ ± 1 %	n.a. / see NOTE
U_f (D)	0,7 V(at I_f = 10 mA) ± 0.1 V	n.a. / see NOTE

In the ZRC signature type, the 6.8 V zener diodes are used to make the signature appear high impedance for low voltage signals. They need to have a high impedance in comparison to the 100 kΩ and 470 nF components. Assuming the signal frequency is high enough for the capacitor to be much lower than 100 kΩ, the zener diode needs to be high impedance in comparison to 100 kΩ. Using an arbitrary factor of 10 gives a 1 MΩ impedance at 6 V and implies a reverse leakage current of less than 6 µA at 6 V. On the other hand, the 100 kΩ resistor seriously limits the current that can be pushed through the zener diode in its conduction region. Therefore the 6.8 V zener knee voltage must be defined at a very low current level. Some zener diodes are available that have their knee defined at 50 µA and consequently they have a low reverse conduction current. They would be suitable for this application.

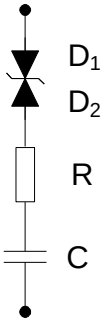

Figure 9: Far-end Signature type ZRC

Table 7: Components of the Far-end signature type ZRC

	Nominal value	Multimeter accuracy
R	100 kΩ ± 1 %	n.a. / see NOTE
C	470 nF ± 1 %	n.a. / see NOTE
U_z (D1)	6.8 V ± 5 % @ 50 µA	n.a. / see NOTE
U_z (D2)	6.8 V ± 5 % @ 50 µA	n.a. / see NOTE

NOTE: In case of using far-end signatures as an MTC, it is not needed to determine the actual values of the components by means of a measuring device. The purpose of the test is to verify if the MELT can detect the far-end signature. It is not required for the MELT to measure the single components of any far-end signature.

4.4.5 Line Model for the Far-end Signature Identification

Line model for the Far-end signature (FS) identification is shown in Figure 10. Two settings of the line model components, representing a 4.5km long 0.4mm twisted pair and a 10.5km long 0.6mm cable, are defined in Table 8 and Table 9.

The resistors used to implement the line model SHALL be of a large enough wattage or a low enough thermal coefficient to prevent a resistance variation greater than 0.1% due to self-heating during the testing execution. The capacitors used to implement the line model SHALL be of a type for which the apparent capacitance doesn't change as a function of the AC or DC voltage applied to them.

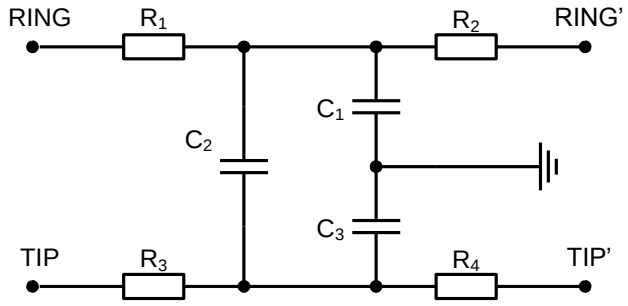

Figure 10: Line Model for the Far-end Signature Identification

Table 8: Components of the line model 1

	Nominal value	Multimeter accuracy
R1	300 Ω ± 5 %	± 1%
R2	300 Ω ± 5 %	± 1%
R3	300 Ω ± 5 %	± 1%
R4	300 Ω ± 5 %	± 1%
C1	300 nF ± 5 %	± 1%
C2	55 nF ± 5 %	± 1%
C3	300 nF ± 5 %	± 1%

Table 9: Components of the line model 2

	Nominal value	Multimeter accuracy
R1	300 Ω ± 5 %	± 1%
R2	300 Ω ± 5 %	± 1%
R3	300 Ω ± 5 %	± 1%
R4	300 Ω ± 5 %	± 1%
C1	600 nF ± 5 %	± 1%
C2	100 nF ± 5 %	± 1%
C3	600 nF ± 5 %	± 1%

4.5 MELT-PMD Configuration Parameters

This section describes the configuration parameters of the MELT-PMD function. When validating the system under test, the configurable parameters should be set to the values listed as "Configuration settings" in the following tables. Note that in some cases, the system MAY autonomously use the closest available value if the listed value is not supported.

4.5.1 Measurement Class (MELT-MCLASS)

Parameter MELT-MCLASS defines the list of measurements to be executed:

- The same combined measurement of the 4-element DC resistance, 3-element capacitance and foreign DC and AC voltage SHALL apply in a consecutive manner to the following test cases: 4-element DC resistance measurement (test case 5.1.1), 3-element capacitance measurement (test case 5.1.2) and foreign DC and AC voltage measurements (test case 5.1.3)
- A single measurement SHALL apply for the following test cases: loop capacitance (test case 5.1.4), loop resistance (test case 5.1.5), 3-element complex admittance (test case 5.1.6) and loop complex admittance (test case 5.1.7)

MELT-MCLASS setting is defined in Table 10.

Table 10: MELT-MCLASS setting

List of measurements	Range	Configuration settings
List of MELT-PMD measurement functions	single measurement or combined measurement	*test cases 5.1.4-5.1.7:* single measurement *test cases 5.1.1-5.1.3:* same combined measurement of the 4-element DC resistance, 3-element capacitance and foreign DC and AC voltage

4.5.2 Peak Metallic Voltage between Tip and Ring (MELT-PV)

Parameter MELT-PV defines the peak metallic voltage which must not be exceeded in any active measurement applying a metallic voltage between tip and ring in order to avoid operation in a non-linear range of termination located at the far-end during the measurement.

MELT-PV setting is defined in Table 11.

Table 11: MELT-PV setting

Peak metallic voltage	Range	Configuration settings
Peak metallic voltage between tip and ring	0 … 100 V	45 V

4.5.3 Signal Frequency for active AC Tests (MELT-AC-F)

Parameter MELT-AC-F defines the frequency used during the 3-element capacitance test, if performed using a sine wave signal, and during the 3-element complex admittance test. The supported set of frequencies is at the vendor's discretion with an option to operate in automatic mode for which the testing routine will select the frequency on its own.

MELT-AC-F setting is defined in Table 12.

Table 12: MELT-AC-F setting

Signal frequency	Range	Configuration settings
For active AC tests	10 … 1000 Hz	25 Hz

4.5.4 Pair Identification Tone Frequency (MELT-PIT-F)

Parameter MELT-PIT-F sets up frequency of the pair identification tone. The supported set of frequencies is at the vendor's discretion.

MELT-PIT -F setting is defined in Table 13.

Table 13: MELT-PIT-F setting

	Range	Configuration settings
Frequency of the pair identification tone	300 … 3400 Hz	800 Hz

4.5.5 Maximum Far-end Signature Conduction Voltage (MELT-MAXFE-SCV)

Parameter MELT-MAXFE-SCV specifies the maximum conduction voltage level of an expected far-end signature.

MELT-MAXFE-SCV setting is defined in Table 14.

Table 14: MELT-MAXFE-SCV setting

	Range	Configuration settings
Maximum conduction voltage level of a far-end signature	0 … 50 V	20 V

4.5.6 Minimum Far-end Signature Conduction Voltage (MELT-MINFE-SCV)

Parameter MELT-MINFE-SCV specifies the minimum conduction voltage level of an expected far-end signature.

MELT-MINFE-SCV setting is defined in Table 15.

Table 15: MELT-MINFE-SCV setting

	Range	Configuration settings
Minimum conduction voltage level of a far-end signature	0 … 50 V	6 V

4.6 MELT-P configuration parameters

This section describes the configuration parameters of the MELT-P function. When validating the system under test, the configurable parameters should be set to the values listed as "Configuration settings" in the following tables.

4.6.1 Loop resistance classification threshold (MELT-LRC-TH)

Parameter MELT-LRC-TH defines the limit values for classification of the resistances to GND of the loop under test.

MELT-LRC-TH setting is defined in Table 16.

Table 16: MELT-LRC-TH setting

Resistance to GND		Configuration settings
Maximum resistance for a short-circuit to GND		1.4 kΩ
Minimum resistance for a leakage to GND		150 kΩ
Maximum resistance for a leakage to GND		1500 kΩ

4.6.2 Loop parameters per unit length (MELT-LOOP-PARAMS)

MELT-LOOP-PARAMS defines the set of characteristic parameters necessary to determine length or distance information of the loop under test.

MELT-LOOP-PARAMS setting is defined in Table 17.

Table 17: MELT-LOOP-PARAMS setting

Cable parameters per unit length	Range	Configuration settings
Capacitance between tip and ring	0 … 100 nF/km	12 nF/km
Capacitance between tip/ring and GND	0 … 100 nF/km	60 nF/km
DC resistance (sum of both wires)	50 … 400 Ω/km	280 Ω/km

4.6.3 Hazardous DC voltage level (MELT-HDCV-L)

MELT-HDCV-L defines the level above which DC voltage SHALL be identified as hazardous.

MELT-HDCV-L setting is defined in Table 18.

Table 18: MELT-HDCV-L setting

	Range	Configuration settings
Hazardous DC voltage	0 … 200 V	120 V

4.6.4 Hazardous AC voltage level (MELT-HACV-L)

MELT-HACV-L defines the level above which AC voltage SHALL be identified as hazardous.

MELT-HACV-L setting is defined in Table 19.

Table 19: MELT-HACV-L setting

	Range	Configuration settings
Hazardous AC voltage	0 … 200 Vrms	50 Vrms

4.6.5 Foreign EMF DC voltage level (MELT-FDCV-L)

MELT-FDCV-L defines the level above which DC voltage SHALL be identified as a foreign EMF.

MELT-FDCV-L setting is defined in Table 20.

Table 20: MELT-FDCV-L setting

	Range	Configuration settings
Foreign EMF DC voltage	0 … 50 V	6 V

4.6.6 Foreign EMF AC voltage level (MELT-FACV-L)

MELT-FACV-L defines the level above which AC voltage SHALL be identified as a foreign EMF.

MELT-FACV-L setting is defined in Table 21.

Table 21: MELT-FACV-L setting

	Range	Configuration settings
Foreign EMF AC voltage	0 … 50 Vrms	10 Vrms

4.6.7 System capacitance at the CPE side (MELT-SYSC-CPE)

MELT-SYSC-CPE defines the expected value of the system capacitance at the CPE side as it appears in parallel between tip and ring in a corresponding MELT measurement.

MEL-SYSC-CPE setting is defined in Table 22.

Table 22: MELT- SYSC-CPE setting

System capacitance at the CPE side	Range	Configuration settings
VDSL2, ADSL2/2plus	0 … 2 µF	27 nF
SHDSL	0 … 2 µF	1 µF

5 MELT-PMD Testing

5.1 MELT-PMD Test Cases for Measurement Functions

5.1.1 The 4-Element DC Resistance

5.1.1.1 Measurement of the 4-element DC resistance with a controlled metallic voltage

Test procedure for measurement of the 4-element DC resistance with a controlled metallic voltage is defined in Table 23.

Table 23: 4-element DC resistance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.1 for definition of the test resistors. Each test resistor SHALL meet tolerance limits of Table 2. (3) See Section 5.1.1.2 for accuracy requirements of the DC test voltages and currents. (4) Set DSL port to IDLE .
Method of Procedure	(1) Connect resistor R1 of Table 2 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect resistor R1 between RING and GND. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect resistor R1 between TIP and GND. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10) Repeat step (1) to (9) using all other test resistors of Table 2 (R2, R3,..., R12). (11) Connect resistor R13 of Table 6 between RING and TIP (open loop). (12) Perform MELT measurement. (13) Record the reported results of the MELT measurement.

Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds, as defined in Section E.1.1/G.996.2 [5]. (2) Measured resistance values R_{TR}, R_{RT}, R_{TG} and R_{RG} SHALL meet the accuracy limits defined in Table E.1/G.996.2, after adding the multimeter tolerance values defined in Table 2.[1] (3) Measured resistance values SHALL be in the range of 0 to 10 MΩ with a granularity of 1 Ω (Section E.2.3.1/G.996.2) (NOTE1). (4) Reported voltage values VDC_{TR}, VDC_{RT}, VDC_{TG} and VDC_{RG} SHOULD meet the requirement of Section 5.1.1.2 (NOTE2). (5) Reported current values IDC_{TR}, IDC_{RT}, IDC_{TG} and IDC_{RG} SHOULD meet the requirement of Section 5.1.1.2 (NOTE3).
NOTE1: In case of an open loop (R13) measured resistance values (R_{TR}, R_{RG} and R_{TG}) greater than 10MΩ SHALL be limited to 10MΩ. NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages VDC_{TR}, VDC_{RT}, VDC_{TG} and VDC_{RG} were for further study in G.996.2. NOTE3: At the time of publication of TR-286 the accuracy requirements for the test currents IDC_{TR}, IDC_{RT}, IDC_{TG} and IDC_{RG} were for further study in G.996.2. NOTE4: The testing procedure will return values for the R_{TR}, R_{RT}, R_{TG}, and R_{RG} branches even if only one branch has a test load and the others are left open. The result obtained for the branch containing the test load SHALL be compared with the test load measurement from the multimeter. The other results SHALL be ignored.	

5.1.1.2 Test voltage and current in the measurement of the 4-element DC resistance with controlled metallic voltage

Test voltages (VDC_{TR}, VDC_{RT}, VDC_{TG} and VDC_{RG}) and test currents (IDC_{TR}, IDC_{RT}, IDC_{TG} and IDC_{RG}) for the measurement of the 4-element DC resistance SHOULD be reported within accuracy limits defined in Table 24 and Table 25. Range of valid values and granularity are defined in Section E.2.3.2/G.996.2 and Section E.2.3.3/G.996.2.

The optional voltage values are returned by the procedure and represent voltages that were present at some instant of time during the test execution. In order to compare the reported values with the actual voltages, they will have to be monitored with an oscilloscope while the test is executing. Measuring them with a multimeter will not be possible.

The optional current values are an estimate of the current that would be measured by two ammeters connected tip-to-ground and ring-to-ground, or by one ammeter connected tip-to-ring. They are not current values that can be measured during the test execution.

Table 24: Test voltages in the 4-element DC resistance measurement

[1] For example: if the required MELT accuracy is +/- 5% and the multimeter accuracy is+/-1%, the overall required accuracy is +/-6%.

Test voltage (V)	Accuracy	Granularity
$-20 \leq VDC_{XY} \leq 20$	± 1 V	100mV
$-100 < VDC_{XY} < -20$ $20 < VDC_{XY} < 100$	± 5 %	100mV

Table 25: Test currents in the 4-element DC resistance measurement

Test current (mA)	Accuracy	Granularity
$-20 \leq IDC_{XY} \leq 20$	± 2 mA	1 µA
$-100 < IDC_{XY} < -20$ $20 < IDC_{XY} < 100$	± 10 %	1 µA

5.1.2 The 3-Element Capacitance

5.1.2.1 Measurement of the 3-element capacitance with a controlled metallic voltage

Test procedure for measurement of the 3-element capacitance with a controlled metallic voltage is defined in Table 26.

Table 26: 3-element capacitance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.2.2 for accuracy requirements of the AC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect capacitor C1 of Table 3 between RING and TIP (open loop). (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect capacitor C2 of Table 3 between RING and TIP. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect capacitor C2 between RING and GND. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10)Connect capacitor C2 between TIP and GND. (11)Perform MELT measurement. (12)Record the reported results of the MELT measurement. (13)Repeat step (4) to (12) using all other capacitors of Table 3 (C3, C4,...,C8).

Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds, as defined in Section E.1.1/G.996.2. (2) Measured capacitance values C_{TR}, C_{TG} and C_{RG} SHALL meet the accuracy limits defined in Table E.2/G.996.2 and Table E.3/G.996.2 (for SHDSL, Table E.4/G.996.2 and Table E.5/G.996.2), after adding the multimeter tolerance values defined in Table 3.[2] (3) Measured capacitance values SHALL be in the range of 0 to 5 µF with a granularity of 0.1nF (Section E.2.3.4/G.996.2) (NOTE1). (4) Reported voltage values VAC_{TR-CC}, VAC_{TG-CC} and VAC_{RG-CC} and frequency SHOULD meet the requirement of Section 5.1.2.2 (NOTE2).
NOTE1: In case of an open loop (C1) measured capacitance values (C_{TR}, C_{RG} and C_{TG}) SHALL be 0nF ± 3nF. Negative results may be rounded to 0nF, see Section E.2.3.4/G.996.2. NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages VAC_{TR-CC}, VAC_{TG-CC} and VAC_{RG-CC} were for further study in G.996.2. NOTE3: The testing procedure will return values for the C_{TR}, C_{TG}, and C_{RG} branches even if only one branch has a test load and the others are left open. The result obtained for the branch containing the test load SHALL be compared with the test load measured with the multimeter. The other results SHALL be ignored.	

5.1.2.2 Test voltages in the 3-element capacitance test with a controlled metallic voltage

Test voltages (VAC_{TR-CC}, VAC_{TG-CC} and VAC_{RG-CC}) for the measurement of the 3-element capacitance (if performed with a sinewave signal) SHOULD be reported within accuracy limits defined in Table 27. Range of valid values and granularity are defined in Section E.2.3.11/G.996.2.

The optional voltage values are returned by the procedure and represent voltages that were present at some instant of time during the test execution. In order to compare the reported values with the actual voltages, they will have to be monitored with an oscilloscope while the test is executing. Measuring them with a multimeter will not be possible.

Table 27: Test voltages in the 3-element capacitance measurement

Test voltage (Vrms)	Accuracy	Granularity
$0 \leq VAC_{XY-CC} \leq 10$	± 0.5 Vrms	100mV
$10 < VAC_{XY-CC} < 100$	± 5 %	100mV

Range of valid values and granularity for the measurement frequency for a 3-element capacitance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

5.1.3 Measurement of foreign voltages

Test procedure for measurement of foreign DC voltage is defined in Table 28.

[2] For example, if the required MELT accuracy is +/-3nF and the multimeter accuracy is+/-1nF, the overall required accuracy is +/-4nF.

Table 28: Foreign DC voltage measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.3 for definition of the foreign voltage DC sources (FVDC). Each FVDC source SHALL meet tolerance limits of Table 4. (3) Set DSL port to IDLE.
Method of Procedure	(1) Connect the foreign DC source between RING and TIP and generate voltage FVDC1 of Table 4 between RING and TIP (open loop). (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect the foreign DC source between RING and TIP and generate voltage FVDC2 of Table 4. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect the foreign DC source between RING and GND and generate voltage FVDC2 of Table 4. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10)Connect the foreign DC source between TIP and GND and generate voltage FVDC2 of Table 4. (11)Perform MELT measurement. (12)Record the reported results of the MELT measurement. (13)Repeat steps (4) to (12), for all other DC source voltages of Table 4 (FVDC3,..., FVDC13).
Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds, as defined in Section E.1.1/G.996.2. (2) Measured DC foreign voltage values $V_{TR,DC}$, $V_{RG,DC}$ and $V_{TG,DC}$ SHALL meet the accuracy limits defined in Table E.6/G.996.2, after adding the multimeter tolerance values defined in Table 4. (3) Measured DC foreign voltage values SHALL be in the range of -350 to 350 V with a granularity of 0.1V (Section E.2.3.5/G.996.2) (NOTE1). (4) Measured DC foreign voltage greater than MELT-HDCV-L (see Section 4.6.3) SHALL be declared as hazardous voltage.
NOTE1: In case of an open loop (FVDC1) measured foreign voltage values ($V_{TR,DC}$, $V_{RG,DC}$ and $V_{TG,D}$) SHALL be 0V ±1V. NOTE2: The testing procedure will return values for the V_{TR}, V_{TG}, and V_{RG} branches even if only one branch has a voltage applied and the others are left open. The result obtained for the branch containing the voltage source SHALL be compared with the voltage measured with the multimeter. The other results SHALL be ignored. Because of the presence of protection components, it is possible that the source voltage be affected by the connection to the test circuit. The multimeter measurement of the applied voltage SHALL be performed during the execution of the testing procedure to compare it with the MELT result.	

Test procedure for measurement of foreign AC voltage and frequency is defined in Table 29.

Table 29: Foreign AC voltage and frequency measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.3 for definition of the foreign voltage AC sources (FVAC). Each FVAC source SHALL meet tolerance limits of Table 5. (3) Set DSL port to IDLE.
Method of Procedure	(1) Connect the foreign AC source between RING and TIP and generate voltage FVAC1 of Table 5 (open loop). (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect the foreign AC source between RING and TIP and generate voltage FVAC2 of Table 5. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect the foreign AC source between RING and GND and generate voltage FVAC2 of Table 5. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10) Connect the foreign AC source between TIP and GND and generate voltage FVAC2 of Table 5. (11) Perform MELT measurement. (12) Record the reported results of the MELT measurement. (13) Repeat steps (4) to (12), for all other AC source voltages of Table 5 (FVAC3,..., FVAC6).
Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds, as defined in Section E.1.1/G.996.2. (2) Measured AC foreign voltage values $V_{TR,AC}$, $V_{RG,AC}$ and $V_{TG,AC}$ SHALL meet the accuracy limits defined in Table E.7/G.996.2, after adding the multimeter tolerance values defined in Table 5. (3) Measured frequency values $F_{TR,AC}$, $F_{RG,AC}$, and $F_{TG,AC}$ SHALL meet the accuracy limits defined in Table E.8/G.996.2, after taking into consideration the multimeter tolerance values defined in TC(2). (4) Measured AC foreign voltage values SHALL be in the range of 0 to 250 Vrms with a granularity of 0.1V (Section E.2.3.5/G.996.2) (NOTE1). (5) Measured frequency values SHALL be in the range of 10 to 100 Hz with a granularity of 0.1 Hz (Section E.2.3.5/G.996.2,). (6) Measured AC foreign voltage greater than MELT-HACV-L (see Section 4.6.4) SHALL be declared as hazardous voltage.

NOTE1: In case of an open loop (FVAC1) measured foreign voltage values ($V_{TR,AC}$, $V_{RG,AC}$ and $V_{TG,AC}$) SHALL be 0V ±1V.

NOTE2: ER(3) and ER(5) does not apply to FVAC1 measurement.

NOTE3: The testing procedure will return values for the V_{TR}, V_{TG}, and V_{RG} branches even if only one branch has a voltage applied and the others are left open. The result obtained for the branch containing the voltage source SHALL be compared with the voltage measured with the multimeter. The other results SHALL be ignored. Because of the presence of protection components, it is possible that the source voltage be affected by the connection to the test circuit. The multimeter measurement of the applied voltage SHALL be performed during the execution of the testing procedure to compare it with the MELT result.

5.1.4 Loop Capacitance

5.1.4.1 Measurement of the loop capacitance with a high metallic voltage

Test procedure for measurement of loop capacitance with a high metallic voltage is defined in Table 30.

Table 30: Loop capacitance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.4.2 for accuracy requirements of the AC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect capacitor C2 of Table 3 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Repeat steps (1) to (3) using all other capacitors of Table 3 (C3, C4,...,C8).
Expected Result	(1) The loop capacitance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured capacitance value $C_{TR,HV}$ SHALL meet the accuracy limits defined in Table E.9/G.996.2 (for SHDSL, Table E.10/G.996.2), after adding the multimeter tolerance values defined in Table 3. (3) Measured capacitance values SHALL be in the range of 0 to 5 µF with a granularity of 0.1nF (Section E.2.3.6/G.996.2). (4) Reported voltage value $VAC_{TR\text{-}HC}$ and frequency SHOULD meet the requirement of Section 5.1.4.2 (NOTE2).
NOTE1: At the time of publication of TR-286 the maximum test time for the loop capacitance measurement was not defined in G.996.2. NOTE2: At the time of publication of TR-286 the accuracy requirement for the test voltage $VAC_{TR\text{-}HC}$ was for further study in G.996.2.	

5.1.4.2 Test voltage in the loop capacitance test with a high metallic voltage

Test voltage ($VAC_{TR\text{-}HC}$) for the measurement of the loop capacitance (if performed with a sinewave signal) SHOULD be reported within accuracy limits defined in Table 31. Range of valid values and granularity are defined in Section E.2.3.12/G.996.2.

This optional value is returned by the procedure and represents a voltage that was present at some instant of time during the test execution. In order to compare the reported value with the actual voltage, it will have to be monitored with an oscilloscope at the same time the test is executing. Measuring it with a multimeter will not be possible.

Table 31: Test voltages in the loop capacitance measurement

Test voltage (Vrms)	Accuracy	Granularity
$0 \leq VAC_{TR\text{-}HC} \leq 10$	± 0.5 Vrms	100mV
$10 < VAC_{TR\text{-}HC} < 100$	± 5 %	100mV

Range of valid values and granularity for the measurement frequency for the loop capacitance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

5.1.5 Loop Resistance

5.1.5.1 Measurement of the loop resistance with a high metallic voltage

Test procedure for measurement of loop resistance with a high metallic voltage is defined in Table 32.

Table 32: Loop resistance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.1 for definition of the test resistors. Each test resistor SHALL meet tolerance limits of Table 2. (3) See Section 5.1.5.2 for accuracy requirements of the DC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect resistor R2 of Table 2 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Repeat step (1) to (3) using the following resistors of Table 2: R3, R4, R5, R6, R7 and R8.
Expected Result	(1) The loop resistance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured resistance values $R_{TR,HV}$ and $R_{RT,HV}$ SHALL meet the accuracy limits defined in Table E.11/G.996.2, after adding the multimeter tolerance values defined in Table 2. (3) Measured resistance values SHALL be in the range of 0 to 10 MΩ with a granularity of 1 Ω (Section E.2.3.7/G.996.2). (4) Reported voltage values $VDCH_{TR}$ and $VDCH_{RT}$ SHOULD meet the requirement of Section 5.1.5.2 (NOTE2).

NOTE1: At the time of publication of TR-286 the maximum test time for the loop resistance measurement was not defined in G.996.2.

NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages $VDCH_{TR}$ and $VDCH_{RT}$ were for further study in G.996.2.

5.1.5.2 Test voltage in the measurement of the loop resistance with high metallic voltage

Test voltages ($VDCH_{TR}$ and $VDCH_{RT}$) for the measurement of the loop resistance SHOULD be reported within accuracy limits defined in Table 33. Range of valid values and granularity are defined in Section E.2.3.8/G.996.2.

This optional value is returned by the procedure and represents a voltage that was present at some instant of time during the test execution. In order to compare the reported value with the actual voltage, it will have to be monitored with an oscilloscope at the same time the test is executing. Measuring it with a multimeter will not be possible.

Table 33: Test voltages in the loop resistance measurement

Test voltage (V)	Accuracy	Granularity
$-20 \leq VDCH_{XY} \leq 20$	± 1 V	100mV
$-100 < VDCH_{XY} < -20$ $20 < VDCH_{XY} < 100$	± 5 %	100mV

5.1.6 The 3-Element complex admittance

5.1.6.1 Measurement of the 3-element complex admittances with a controlled metallic voltage

The complex admittance Y_{XY} ($Y_{XY} = abs(G_{XY} + jB_{XY})$) MAY be automatically provided by the 3-element capacitance measurement with controlled metallic voltage defined in Section 5.1.2. Alternatively, the test procedure defined in Table 34 SHOULD apply.

Table 34: 3-element complex admittance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.6.2 for accuracy requirements of the AC test voltages. (4) Set DSL port to IDLE.

Method of Procedure	(1) Connect capacitor C1 of Table 3 between RING and TIP (open loop). (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect capacitor C2 of Table 3 between RING and TIP. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect capacitor C2 between RING and GND. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10)Connect capacitor C2 between TIP and GND. (11)Perform MELT measurement. (12)Record the reported results of the MELT measurement. (13)Repeat step (4) to (12) using all other capacitors of Table 3 (C3, C4,...,C8).
Expected Result	(1) The 3-element complex admittance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured admittance values (G_{TR}, B_{TR}, G_{TG}, B_{TG}, G_{RG} and B_{RG}) SHALL be in the range of 0.1 µSiemens to 0.1 Siemens with a granularity of 0.1 µSiemens (Section E.2.3.9/G.996.2). (3) Reported voltage values VAC_{TR-CA}, VAC_{TG-CA} and VAC_{RG-CA} and frequency SHOULD meet the requirement of Section 5.1.6.2 (NOTE2).
NOTE1: At the time of publication of TR-286 the maximum test time for the 3-element complex admittance measurement was not defined in G.996.2. NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages VAC_{TR-CA}, VAC_{TG-CA} and VAC_{RG-CA} were for further study in G.996.2.	

5.1.6.2 Test voltages in the 3-element complex admittance test with a controlled metallic voltage

Test voltages (VAC_{TR-CA}, VAC_{TG-CA} and VAC_{RG-CA}) for the measurement of the 3-element complex capacitance (if performed with a sinewave signal) SHOULD be reported within accuracy limits defined in Table 35. Range of valid values and granularity are defined in Section E.2.3.13/G.996.2.

These optional values are returned by the procedure and represent voltages that were present at some instant of time during the test execution. In order to compare the reported values with the actual voltages, they will have to be monitored with an oscilloscope at the same time the test is executing. Measuring them with a multimeter will not be possible.

Table 35: Test voltages in the 3-element complex capacitance measurement

Test voltage (Vrms)	Accuracy	Granularity
$0 \leq VAC_{XY-CA} \leq 10$	± 0.5 Vrms	100mV
$10 < VAC_{XY-CA} < 100$	± 5 %	100mV

Range of valid values and granularity for the measurement frequency for the 3-element complex admittance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

5.1.7 Loop complex admittance

5.1.7.1 Measurement of the loop complex admittance with a high metallic voltage

Test procedure for measurement of the loop complex admittance with a high metallic voltage is defined in Table 36.

Table 36: Loop complex admittance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.7.2 for accuracy requirements of the AC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect capacitor C4 of Table 3 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Repeat step (1) to (3) using the following test capacitors C5, C6 and C7 of Table 3.
Expected Result	(1) The loop complex admittance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured admittance values ($G_{TR,HV}$ and $B_{TR,HV}$) SHALL be in the range of 0.1 µSiemens to 0.1 Siemens with a granularity of 0.1 µSiemens (Section E.2.3.10/G.996.2). (3) Reported voltage value $VAC_{TR\text{-}HA}$ and frequency SHOULD meet the requirement of Section 5.1.7.2 (NOTE2).
NOTE1: At the time of publication of TR-286 the maximum test time for the loop complex admittance measurement was not defined in G.996.2. NOTE2: At the time of publication of TR-286 the accuracy requirement for the test voltage $VAC_{HR\text{-}CA}$ was for further study in G.996.2.	

5.1.7.2 Test voltage in the loop complex admittance test with a high metallic voltage

Test voltage ($VAC_{TR\text{-}HA}$) for the measurement of the loop complex admittance (if performed with a sinewave signal) SHOULD be reported within accuracy limits defined in Table 37. Range of valid values and granularity are defined in Section E.2.3.14/G.996.2.

This optional value is returned by the procedure and represents a voltage that was present at some instant of time during the test execution. In order to compare the reported value with the actual voltage, it will have to be monitored with an oscilloscope at the same time the test is executing. Measuring it with a multimeter will not be possible.

Table 37: Test voltages in the loop complex admittance measurement

Test voltage (Vrms)	Accuracy	Granularity
$0 \leq VAC_{TR\text{-}HA} \leq 10$	± 0.5 Vrms	100mV
$10 < VAC_{TR\text{-}HA} < 100$	± 5 %	100mV

Range of valid values and granularity for the measurement frequency for the loop complex admittance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

5.2 MELT-PMD Test Cases for Non-Measurement Functions

5.2.1 Pair identification tone measurement

Test procedure for measurement of pair identification tone is defined in Table 38.

Table 38: Pair identification tone measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.1 for definition of the test resistor. The test resistor SHALL meet tolerance limits of Table 2. (3) See Section E1.2.1/G.996.2 for the superimposed DC test voltage. (4) See Table 13 for the parameter MELT-PIT-F. (5) Set DSL port to IDLE.
Method of Procedure	(1) Connect resistor R4 of Table 2 between RING and TIP. (2) Switch on the pair identification tone (ID tone). (3) Measure ID tone frequency, level and harmonic distortion factor and polarity of the superimposed DC voltage. (4) Switch off the ID tone. (5) Switch on the ID tone for duration of 30 seconds (runtime). (6) After the runtime expired, control whether the tone is switched off.
Expected Result	(1) ID tone SHALL be switchable on and off manually. (2) Predefined runtime SHOULD meet tolerance requirement of ±5%. (3) After the runtime is expired, ID tone SHALL be automatically switched off. (4) Measured ID tone frequency SHALL be 800Hz ± 10Hz. (5) ID tone level measured at DSL port SHALL be between 120 and 330 mVrms. (6) ID tone harmonic distortion SHALL be ≤ 5%. (7) Measured superimposed DC voltage SHALL be 10 V ± 2 V, when measured into an open-circuit load by removing resistor R4.

5.3 MELT-PMD Test cases for Reporting Parameters

5.3.1 Measurement frequency for active AC tests

This parameter (Section E.2.2.1/G.996.2) is the measurement frequency for a 3-element capacitance test (Section 5.1.2), loop capacitance test (Section 5.1.4), 3-element complex admittance test (Section 5.1.6) and loop complex admittance test (Section 5.1.7).

5.3.2 Input impedance for foreign voltage measurements

This parameter (E.2.2.2/G.996.2) reports the nominal input impedance of the measuring instrument during the foreign voltage tests (Section 5.1.3).

6 MELT-P Testing

6.1 Identification of an open wire failure

The purpose of this test (see Table 40) is to identify the type of an open wire failure (MELT-O-WIRE-type) and the estimated distance from the DSLAM (MELT-O-WIRE-DIST). The following failure types are defined in Section F.1.1.1/G.996.2:

1. *No open wire failure detected*
2. *Tip and ring wires open in equal distance*
3. *Tip wire open*
4. *Ring wire open*
5. *Undefined*

The test SHALL be performed with the following maximum absolute difference of a cable capacitance C_{TG} and C_{RG} (see Table 39) for the same length TIP and RING wire (MAXCDIF).

Table 39: Maximum absolute difference of a cable capacitance C_{TG} and C_{RG}

Range of C_{TG}, C_{RG}	Range of MAXCDIF	MAXCDIF
(0 nF , 100 nF)	(0 nF , 20 nF)	5nF
(100 nF , 1000 nF)	(0 , 50 %) of max(C_{TG}, C_{RG})	10%
NOTE: MAXCDIF SHALL be larger than the MELT accuracy for capacitance measurements in the respective range (see Section 5.1.2).		

Table 40: Open wire failure test

Test Configuration	(1) See Figure 1 for the test setup. (2) Set DSL port to IDLE.

Method of Procedure	(1) Between RING and TIP connect one of the capacitors defined in Table 3 which value is greater than that of the system capacitance at the CPE side (MELT-SYSC-CPE, defined in Section 4.6.7). (2) Perform the MELT-PMD tests. (3) Record the reported results of the MELT measurement. (4) Between TIP and GND connect one of the capacitors C2-C5 defined in Table 3. Between RING and GND connect a capacitor C_{RG} such that C_{RG}-C_{TG} is greater than the default MAXCDIF value defined inTable 39. (5) Perform the MELT-PMD tests. (6) Record the reported results of the MELT measurement. (7) Between RING and GND connect one of the capacitors C2-C5 defined in Table 3. Between TIP and GND connect a capacitor C_{TG} such that C_{TG}-C_{RG} is greater than the default MAXCDIF value defined inTable 39. (8) Perform the MELT-PMD tests. (9) Record the reported results of the MELT measurement. (10) Report the estimated distance of the open wire failure from the DSLAM. (11) Connect the line model 1 defined in Section 4.4.5 to the test setup defined in TC(1). (12) Repeat steps (1) to (10). (13) In the test setup defined in TC(1), replace the line model 1 with the line model 2 defined in Section 4.4.5. (14) Repeat steps (1) to (10).
Expected Result	(1) *No open wire failure detected* SHALL be declared, if the following applies: • the measured capacitance value $C_{TR\text{-}Term}$ is ≥ MELT-SYSC-CPE (NOTE1) • *Signature DR detected* or *Signature ZRC detected* • *Tip and ring wires shorted to each other* detected (2) *Tip and ring wires open in equal distance* SHALL be declared if $\lvert C_{TG} - C_{RG} \rvert$ is ≤ MAXCDIF and *No open wire failure detected* is not declared. (3) *Tip wire open* SHALL be declared if the capacitance value C_{TG} is < C_{RG} –MAXCDIF and *No open wire failure detected* is not declared. (4) *Ring wire open* SHALL be declared if the capacitance value C_{RG} < C_{TG} –MAXCDIF and *No open wire failure detected* is not declared. (5) Otherwise, open wire failure type 5 *Undefined* SHALL be declared
NOTE1: $C_{TR\text{-}Term}$ SHALL take into account only the termination capacitance. Therefore, the line capacitance SHALL be subtracted from the measured C_{TR} value.	

6.2 Identification of a short circuit failure

The purpose of this test (see Table 42) is to identify the type of a short circuit failure (MELT-S-CCT-type). The following failure types are defined in Section F.1.1.2/G.996.2:

1. *No short circuit detected*
2. *Tip and ring wires shorted to GND*
3. *Tip wire shorted to GND*
4. *Ring wire shorted to GND*
5. *Tip and ring wires shorted to each other*
6. *Undefined*

The test SHALL be performed with the following limit value for classification of the TIP to RING short circuit (MELT-TRSHORT-TH, see Table 41).

Table 41: MELT-TRSHORT-TH setting

Resistance to TIP-RING short circuit	Range	Configuration settings
Maximum resistance for a TIP-RING short circuit	10 Ω … 10 kΩ	1 kΩ

Table 42: Short circuit failure test

Test Configuration	(1) See Figure 1 for the test setup. (2) Set DSL port to IDLE.
Method of Procedure	(1) Connect resistor R_{SHORTL} between TIP and GND (NOTE1). (2) Perform the MELT-PMD tests. (3) Record the reported results of the MELT measurement. (4) Connect resistor R_{SHORTL} between RING and GND. (5) Repeat steps (2) to (3). (6) Connect resistor $R_{TR,SHORTL}$ between TIP and RING (NOTE2). (7) Repeat steps (2) to (3). (8) Connect resistor R_{SHORTL} between TIP and GND and resistor R_{SHORTL} between RING and GND. (9) Repeat steps (2) to (3). (10) Connect resistor R_{SHORTH} between TIP and GND, resistor R_{SHORTH} between RING and GND and resistor $R_{TR,SHORTH}$ between TIP and RING (NOTE3). (11) Repeat steps (2) to (3).

Expected Result	(1) If the measured resistor values R_{TG} and R_{RG} are > maximum resistance for a short to ground specified in MELT-LRC-TH and R_{TR} and R_{RT} are > MELT-TRSHORT-TH, the *No short circuit failure detected* SHALL be declared. (2) If the measured resistor values R_{TG} and R_{RG} are ≤ maximum resistance for a short to ground specified in MELT-LRC-TH the *Tip and ring wires shorted to GND* SHALL be declared. (3) If the measured resistor value R_{TG} is ≤ maximum resistance for a short to ground specified in MELT-LRC-TH, the *Tip wire shorted to GND* SHALL be declared. (4) If the measured resistor value R_{RG} is ≤ maximum resistance for a short to ground specified in MELT-LRC-TH, the *Ring wire shorted to GND* SHALL be declared. (5) If the measured resistor values R_{TR} and R_{RT} are ≤ MELT-TRSHORT-TH, *Tip and ring wires shorted to each other* and *No open wire failure detected* SHALL be declared . (6) Otherwise, short circuit failure type 6 *Undefined* SHALL be declared.
NOTE1: The following constraint SHALL apply: R_{SHORTL} < 90% of the maximum resistance for a short to ground specified in MELT-LRC-TH (see Section 4.6.1). NOTE2: The following constraint SHALL apply: $R_{TR,SHORTL}$ < 90% of MELT-TRSHORT-TH. NOTE3: The following constraints SHALL apply: 1. R_{SHORTH} ≥ 110 % of the maximum resistance for a short to ground specified in MELT-LRC-TH 2. $R_{TR,SHORTH}$ ≥ 110% of MELT-TRSHORT-TH	

6.3 Resistive fault identification

The purpose of this test (see Table 43) is to identify a resistive to GND failure type (MELT-RFAULT-ID). The following failure types are defined in Section F.1.1.4/G.996.2:

1. *No resistive fault detected*
2. *Resistive fault tip and ring to GND*
3. *Resistive fault tip to GND*
4. *Resistive fault ring to GND*

Table 43: Resistive fault identification test

Test Configuration	(1) See Figure 1 for the test setup. (2) Set DSL port to IDLE.

Method of Procedure	(1) Connect resistor R_{SHORTH} between TIP and GND and resistor R_{SHORTH} between RING and GND (NOTE1). (2) Perform the MELT-PMD tests. (3) Record the reported results of the MELT measurement. (4) Connect resistor R_{SHORTH} between TIP and GND. (5) Repeat steps (2) to (3). (6) Connect resistor R_{SHORTH} between RING and GND. (7) Repeat steps (2) to (3). (8) Connect resistor R_{RESL} between TIP and GND and resistor R_{RESL} between RING and GND (NOTE2). (9) Repeat steps (2) to (3). (10) Connect resistor R_{RESH} between TIP and GND and resistor R_{RESH} between RING and GND (NOTE3). (11) Repeat steps (2) to (3).
Expected Result	(1) If the measured resistor values R_{TG} and R_{RG} are ≥ minimum MELT-LRC-TH for a leakage to GND or ≤ maximum MELT- LRC–TH for a short circuit to GND, the *No resistive fault detected* SHALL be declared. (2) If the measured resistor values R_{TG} and R_{RG} are < minimum MELT-LRC-TH for a leakage to GND and > maximum MELT- LRC -TH for a short circuit to GND, the *Resistive fault tip and ring to GND* SHALL be declared. (3) If the measured resistor value R_{TG} is < minimum MELT-LRC-TH for a leakage to GND and > maximum MELT- LRC -TH for a short circuit to GND, the *Resistive fault tip to GND* SHALL be declared. (4) If the measured resistor value R_{RG} is < minimum MELT-LRC-TH for a leakage to GND and > maximum MELT- LRC -TH for a short circuit to GND, the *Resistive fault ring to GND* SHALL be declared.
NOTE1: The following constraint SHALL apply: R_{SHORTH} is defined in Section 6.2. NOTE2: The following constraints SHALL apply: R_{RESL} < 90 % of the minimum resistance for a leakage to GND (MELT-LRC-TH defined in Section 4.7.1) and ≥ $R_{SHORTH.}$ NOTE3: The following constraint SHALL apply: R_{RESH} ≥ 110 % of the minimum resistance for a leakage to GND (MELT-LRC-TH defined in Section 4.6.1).	

6.4 Leakage identification

The purpose of this test (see Table 44) is to identify a leakage to GND failure (MELT-LEAK-ID). The following failure types are defined in Section F.1.1.3/G.996.2:

1. *No leakage detected*
2. *Tip and ring wire leaking to GND*
3. *Tip wire leaking to GND*
4. *Ring wire leaking to GND*

Table 44: Leakage identification test

Test Configuration	(1) See Figure 1 for the test setup. (2) Set DSL port to IDLE.
Method of Procedure	(1) Connect resistor R_{LEAKL} between TIP and GND (NOTE1). (2) Perform the MELT-PMD tests. (3) Record the reported results of the MELT measurement. (4) Connect resistor R_{LEAKL} between RING and GND. (5) Repeat steps (2) to (3). (6) Connect resistor R_{LEAKL} between TIP and GND and resistor R_{LEAKL} between RING and GND. (7) Repeat steps (2) to (3). (8) Connect resistor R_{LEAKH} between TIP and GND and resistor R_{LEAKH} between RING and GND (NOTE2). (9) Repeat steps (2) to (3).
Expected Result	(1) If the measured resistor values R_{TG} and R_{RG} are < minimum MELT-LRC-TH for a leakage to ground or > maximum MELT-LRCTH for a leakage to ground, the *No leakage detected* SHALL be declared. (2) If the measured resistor values R_{TG} and R_{RG} are ≥ minimum MELT-LRC-TH for a leakage to ground and ≤ maximum MELT-LRCTH for a leakage to ground, the *Tip and ring wire leaking to GND* SHALL be declared. (3) If the measured resistor value R_{TG} is ≥ minimum MELT-LRC-TH for a leakage to ground and ≤ maximum MELT-LRCTH for a leakage to ground, the *Tip wire leaking to GND* SHALL be declared. (4) If the measured resistor value R_{RG} is ≥ minimum MELT-LRC-TH for a leakage to ground and ≤ maximum MELT-LRCTH for a leakage to ground, the *Ring wire leaking to GND* SHALL be declared.
NOTE1: The following constraints SHALL apply: R_{LEAKL} < 80 % of the maximum resistance for a leakage to GND (MELT-LRC-TH defined in Section 4.6.1) and ≥ 110 % of the minimum resistance for a leakage to GND (MELT-LRC-TH defined in Section 4.6.1). NOTE2: The following constraint SHALL apply: R_{LEAKH} ≥ 120 % of the maximum resistance for a leakage to GND (MELT-LRC-TH).	

6.5 Foreign voltage classification

6.5.1 Foreign voltage type

The purpose of this test (see Table 45) is to identify the following foreign voltage types (MELT-FV-TYPE), defined in Section F.1.1.5.1/G.996.2:

1. *No foreign voltage detected*
2. *16 2/3 Hz AC voltage*
3. *25 Hz AC voltage*
4. *50 Hz AC voltage*
5. *60 Hz AC voltage*
6. *POTS equipment (-48 V DC)*

7.*ISDN equipment (-96 V DC)*
8.*Undefined foreign voltage detected*

Table 45: Foreign voltage type test

Test Configuration	(1) See Figure 1 for the test setup. (2) Set DSL port to IDLE.
Method of Procedure	(1) Connect voltage V_{ForDCL} between TIP and GND (NOTE1). (2) Perform the MELT-PMD tests. (3) Record the reported results of the MELT measurement. (4) Connect voltage V_{ForDCL} between RING and GND. (5) Repeat steps (2) to (3). (6) Connect voltage V_{ForDCL} between TIP and RING. (7) Repeat steps (2) to (3). (8) Repeat steps (1) to (7) using voltage V_{ForDCH} (NOTE2). (9) Repeat steps (1) to (7) using voltage V_{ForACL} (NOTE3). (10)Repeat steps (1) to (7) using voltage $V_{ForACH,}$ of an arbitrary frequency +/-5 Hz different from the following values: 16 2/3 Hz, 25 Hz, 50 Hz, 60 Hz (NOTE4). (11)Repeat steps (1) to (7) using voltage V_{ForACH}, of frequency 16 2/3 Hz ±0.1 Hz. (12)Repeat steps (1) to (7) using voltage V_{ForACH}, of frequency 25 Hz ±0.1 Hz. (13)Repeat steps (1) to (7) using voltage V_{ForACH}, of frequency 50 Hz ±0.1 Hz. (14)Repeat steps (1) to (7) using voltage V_{ForACH}, of frequency 60 Hz ±0.1 Hz. (15)Repeat steps (1) to (7) using a foreign voltage of -48 V DC+/-1% (NOTE5). (16)Repeat step1 (1) to (7) using a foreign voltage of -96 V DC +/-1% (NOTE6).

Expected Result	(1) *No foreign voltage detected* is declared, if the absolute value of the measured voltages $V_{RG,DC}$, $V_{TG,DC}$ and $V_{TR,DC}$ are < MELT-FDCV-L, and $V_{RG,AC}$, $V_{TG,AC}$ and $V_{TR,AC}$ are < MELT-FACV-L. (2) *16 2/3 Hz AC voltage* is declared, if at least one of the measured voltages $V_{RG,AC}$, $V_{TG,AC}$ and $V_{TR,AC}$ is ≥ MELT-FACV-L, and the measured frequency is 16 2/3 Hz+/- 3Hz. (3) *25 Hz AC voltage* is declared, if at least one of the measured voltages $V_{RG,AC}$, $V_{TG,AC}$ and $V_{TR,AC}$ is ≥ MELT-FACV-L, and the measured frequency is 25 Hz+/- 3Hz. (4) *50 Hz AC voltage* is declared, if at least one of the measured voltages $V_{RG,AC}$, $V_{TG,AC}$ and $V_{TR,AC}$ is ≥ MELT-FACV-L, and the measured frequency is 50 Hz+/- 3Hz. (5) *60 Hz AC voltage* is declared, if at least one of the measured voltages $V_{RG,AC}$, $V_{TG,AC}$ and $V_{TR,AC}$ is ≥ MELT-FACV-L, and the measured frequency is 60 Hz+/- 3Hz. (6) *-48 V DC* is declared, if at least one of the measurement voltages $V_{RG,DC}$, $V_{TG,DC}$, $V_{TR,DC}$ (or $-V_{TR,DC}$) is -48 V DC+/- 4V. (7) *-96 V DC* is declared, if at least one of the measurement voltages $V_{RG,DC}$, $V_{TG,DC}$, $V_{TR,DC}$ (or $-V_{TR,DC}$) is -96 V DC+/- 8V. (8) *Undefined foreign voltage detected* is declared, if for at least one of the measurement voltages, the absolute value of $V_{RG,DC}$,$V_{TG,DC}$ or $V_{TR,DC}$ is ≥ MELT-FDCV-L, or at least one of the measurement voltages $V_{RG,AC}$, $V_{TG,AC}$ or $V_{TR,AC}$ is ≥ MELT-FACV-L, but none of the ER(1)-ER(7) applies.
NOTE1: V_{ForDCL} may be positive or negative with respect to GND and its absolute value SHALL be < 90 % of (at least 1 V below) MELT-FDCV-L (defined in Section 4.6.5). NOTE2: V_{ForDCH} may be positive or negative with respect to GND and its absolute value SHALL be ≥ 110 % of (at least 1 V above) MELT-FDCV-L. NOTE3: V_{ForACL} SHALL be < 90 % of (at least 1 Vrms below) MELT-FACV-L (defined in Section 4.6.6). NOTE4: V_{ForACH} SHALL be ≥ 110 % of (at least 1 Vrms above) MELT-FACV-L. NOTE5: -48V has to be connected between TIP-GND, RING-GND, TIP-RING and RING-TIP. NOTE6: -96V has to be connected between TIP-GND, RING-GND, TIP-RING and RING-TIP.	

6.5.2 Foreign voltage level class

The purpose of this test (see Table 46) is to identify the following foreign voltage level types (MELT-FV-LEVEL), defined in Section F.1.1.5.2/G.996.2:

1. *Hazardous potential*
2. *Foreign electromotive force*
3. *Other*

Table 46: Foreign voltage level test

Test Configuration	(1) See Figure 1 for the test setup. (2) Set DSL port to IDLE.
Method of Procedure	(1) Connect voltage V_{HazDCL} between TIP and GND (NOTE1). (2) Perform the MELT-PMD tests. (3) Record the reported results of the MELT measurement. (4) Connect voltage V_{HazDCL} between RING and GND. (5) Repeat steps (2) to (3). (6) Connect voltage V_{HazDCL} between TIP and RING. (7) Repeat step (2) to (3). (8) Repeat steps (1) to (7) using voltage V_{HazDCH} (NOTE2). (9) Repeat steps (1) to (7) using the voltage V_{HazACL} (NOTE3). (10)Repeat steps (1) to (7) using voltage V_{HazACH} (NOTE4).
Expected Result	(1) *Hazardous potential* is declared, if the absolute value of at least one of the measured voltages $V_{RG,DC}$, $V_{TG,DC}$ or $V_{TR,DC} \geq$ MELT-HDCV-L, or $V_{RG,AC}$, $V_{TG,AC}$ or $V_{TR,AC}$ is $\geq$ MELT-HACV-L. (2) *Foreign electromotive force* is declared, if the absolute value of at least one of the measured voltages $V_{RG,DC}$, $V_{TG,DC}$ or $V_{TR,DC}$ is $\geq$ MELT-FDCV-L and < MELT-HDCV-L, or $V_{RG,AC}$, $V_{TG,AC}$ or $V_{TR,AC}$ is $\geq$ MELT-FACV-L and MELT-HACV-L. (3) *Other* is declared, if the absolute value of the measured voltages $V_{RG,DC}$, $V_{TG,DC}$ or $V_{TR,DC}$ is < MELT-FDCV-L, and $V_{RG,AC}$, $V_{TG,AC}$ or $V_{TR,AC}$ is < MELT-FACV-L.
NOTE1: V_{HazDCL} may be positive or negative with respect to GND and its absolute value SHALL be < 90 % of MELT-HDCV-L (defined in Section 4.6.3). NOTE2: V_{HazDCH} may be positive or negative with respect to GND and its absolute value SHALL be $\geq$ 110 % of MELT-HDCV-L. NOTE3: V_{HazACL} SHALL be < 90 % of MELT-HACV-L (defined in Section 4.6.4). NOTE4: V_{HazACH} SHALL be $\geq$ 110 % of MELT-HACV-L.	

6.6 Far-end signature topology identification

The purpose of this test (see Table 47) is to identify the far-end signature topology type (MELT-FES-ID). The following identification classes are defined in Section F.1.1.6/G.996.2:

1. *No signature detected*
2. *Unknown signature*
3. *Signature type DR detected*
4. *Signature type ZRC detected*

Table 47: Far-end signature topology identification test

Test Configuration	(1) See Figure 2 for the test setup. (2) Set DSL port to IDLE.

Method of Procedure	(1) Connect the Far-end Signature type DR between TIP and RING. (2) Perform the MELT-PMD tests. (3) Record the reported results of the MELT measurement. (4) Connect the Far-end Signature type ZRC between TIP and RING. (5) Perform the MELT-PMD tests. (6) Record the reported results of the MELT measurement. (7) Connect the Far-end Signature type DR and the Far-end Signature type ZRC between TIP and RING. (8) Perform the MELT-PMD tests. (9) Record the reported results of the MELT measurement. (10) Connect the line model 1 defined in Section 4.4.5 to the test setup. (11) Repeat steps (1) to (9). (12) Connect the line model 2 defined in Section 4.4.5 to the test setup. (13) Repeat steps (1) to (9).
Expected Result	(1) Identification *Signature type DR detected* and *No open wire failure detected* SHALL be declared in conjunction with the reported results of MOP(3). (2) Identification *Signature type ZRC detected* and *No open wire failure detected* SHALL be declared in conjunction with the reported results of MOP(6). (3) Identification *Signature type DR detected, Signature type ZRC detected* and *No open wire failure detected* SHALL be declared in conjunction with the reported results of MOP(9).

7 Same pair DSL and MELT Operation

7.1 Same pair ADSL2plus - MELT test

A method for testing the MELT impact on ADSL2plus transmission in Showtime is shown in Table 48.

Table 48: Same Pair MELT – ADSL2plus test

Test Configuration	(1) See Figure 3 for the test setup. (2) Configure the SUT in one of the following specific test profiles associated to the ADSL2plus operation mode to be tested (see Section 4.1): • A2P_RA_I_30000k • B2P_RA_I_30000k • J2P60_RA_I_30000k (3)Connect the ATU-C to the ATU-R through 500m PE04 cable. (4)Inject white noise of -110dBm/Hz at both the ATU-C and ATU-R ends. (5)MELT entity SHALL be in IDLE mode, i.e. inactive but ready to start one of the following MELT measurements: a. 4-element DC resistance b. 3-element capacitance c. foreign voltages d. loop capacitance e. loop resistance f. 3-element complex admittance g. loop complex admittance

Method of Procedure	(1) Connect the first MTC component defined for MELT measurement of type a. (see Section 4.4). (2) Force a new initialization and wait for modems to sync (NOTE1). (3) Wait 1 minute following synchronization. (4) Record the upstream and downstream net data rate and reported noise margin. (5) Record the value of the following counters at the ATU-C: CV-C, CV-CFE, ES-L, ES-LFE, SES-L and SES-LFE, and, if available, at the ATU-R: CV-C, ES-L and SES-L. (6) Perform MELT measurement of type a. (7) Repeat step (6) 4 times (5 measurements in total). (8) Force performance counters update and wait 30 seconds. (9) Record the value of the following counters at the ATU-C: CV-C, CV-CFE, ES-L, ES-LFE, SES-L and SES-LFE, and, if available, at the ATU-R: CV-C, ES-L and SES-L. Calculate the increase of the SES counter with respect to the values recorded in (5). (10)Repeat step (2) through (9) for the loop lengths1000m and 2000m. (11)Repeat step (1) through (10) for two other MTC components defined for MELT measurement of type a, in a way that the 3 values tested cover the low, mid and high range of the component (NOTE2). (12)Repeat step (1) through (11) for all other types of MELT measurements defined in TC(5).
Expected Result	(1) No loss of synchronization SHALL occur during measurements in MOP(6) and (7). (2) No increase of SES-L and SES-LFE at the ATU-C SHALL be reported in MOP(9). (3) If available, no increase of SES-L at the ATU-R SHALL be reported in MOP(9).
NOTE1: Some MTC single components (e.g. R1, C8) may prevent system from reaching the Showtime, in which case the MELT measurement SHALL be skipped. NOTE2: Special foreign voltage value “OPEN” SHALL NOT be chosen.	

7.2 Same pair VDSL2 - MELT test

A method for testing the MELT impact on VDSL2 transmission in Showtime is shown in Table 49.

Table 49: Same Pair MELT – VDSL2 test

Test Configuration	(1) See Figure 3 for the test setup. (2) As per VDSL2 band-profile to be tested, configure the SUT in RA_I_150_150 specific line-setting (see Section 4.1). If, for the specific band-profile, profile-line combinations are defined with DPBO and/or UPBO enabled, these SHALL be applied. (3) Connect the VTU-O to the VTU-R through: • 200m PE04 cable for profiles up to 17MHz • 100m PE04 cable for 30MHz profile (4) Inject white noise of -110dBm/Hz at both the VTU-O and VTU-R ends. (5) MELT entity SHALL be in IDLE mode, i.e. inactive but ready to start one of the following MELT measurements: a. 4-element DC resistance b. 3-element capacitance c. foreign voltages d. loop capacitance e. loop resistance f. 3-element complex admittance g. loop complex admittance
Method of Procedure	(1) Connect the first MTC component defined for MELT measurement of type a. (see Section 4.4). (2) Force a new initialization and wait for modems to sync (NOTE1). (3) Wait 1 minute following synchronization. (4) Record the upstream and downstream net data rate and reported noise margins. (5) Record the value of the following counters at the VTU-O: CV-C, CV-CFE, ES-L, ES-LFE, SES-L and SES-LFE, and, if available, at the VTU-R: CV-C, ES-L and SES-L. (6) Perform MELT measurement of type a. (7) Repeat step (6) 4 times (5 measurements in total). (8) Force performance counters update and wait 30 seconds. (9) Record the value of the following counters at the VTU-O: CV-C, CV-CFE, ES-L, ES-LFE, SES-L and SES-LFE, and, if available, at the VTU-R: CV-C, ES-L and SES-L. Calculate the increase of the SES counter with respect to the values recorded in (5). (10)Repeat step (2) through (9) for the loop lengths: •600m and 1000m for profiles up to 17MHz • 300m and 500m for 30MHz profile (11)Repeat step (1) through (10) for two other MTC components defined for MELT measurement of type a, in a way that the 3 values tested cover the low, mid and high range of the component (NOTE2). (12)Repeat step (1) through (11) for all other types of MELT measurements defined in TC(5).

Expected Result	(1) No loss of synchronization SHALL occur during measurements in MOP(6) and (7). (2) No increase of SES-L and SES-LFE at the VTU-O SHALL be reported in MOP(9). (3) If available, no increase of SES-L at the VTU-R SHALL be reported in MOP(9).
NOTE1: Some MTC single components (e.g. R1, C8) may prevent system from reaching the Showtime, in which case the MELT measurement SHALL be skipped. NOTE2: Special foreign voltage value "OPEN" SHALL NOT be chosen.	

7.3 Same pair SHDSL - MELT test

A method for testing the MELT impact on SHDSL transmission in Showtime is shown in Table 50.

Table 50: Same Pair MELT – SHDSL test

Test Configuration	(1) See Figure 3 for the test setup. (2) Configure the SUT for operation in TCPAM-16 profile at fixed data rate of 384kbps, as defined in Section 4.1. (3) Connect the STU-C to the STU-R through 5500m PE04 cable. (4) Inject white noise of -110dBm/Hz at both the STU-C and STU-R ends. (5) MELT entity SHALL be in IDLE mode, i.e. inactive but ready to start one of the following MELT measurements: a. 4-element DC resistance b. 3-element capacitance c. foreign voltages d. loop capacitance e. loop resistance f. 3-element complex admittance g. loop complex admittance

Method of Procedure	(1) Connect the first MTC component defined for MELT measurement of type a. (see Section 4.4). (2) Force a new initialization and wait for modems to sync (NOTE1). (3) Wait 1 minute following synchronization. (4) Record the upstream and downstream reported noise margins. (5) Record the value of the upstream and downstream counters CV, ES and SES. (6) Perform MELT measurement of type a. (7) Repeat step (6) 4 times (5 measurements in total). (8) Force performance counters update and wait 30 seconds. (9) Record the value of the upstream and downstream counters CV, ES and SES. Calculate the increase of SES counter with respect to the value recorded in (5). (10) Repeat step (2) through (9) in TCPAM-16 profile at the following fixed data rates and loop lengths: • 512kbps at 5000m • 1024kbps at 4500m • 2048kbps at 4000m (11) Configure the STU for operation in TCPAM-32 profile (see Section 4.1) and repeat step (2) through (9) for the following fixed data rates and loop lengths: • 2560kbps at 3500m • 4096kbps at 2500m • 5696kbps at 1000m (12) Repeat step (1) through (11) for two other MTC components defined for MELT measurement of type a, in a way that the 3 values tested cover the low, mid and high range of the component (NOTE2). (13) Repeat step (1) through (12) for all other types of MELT measurements defined in TC(5).
Expected Result	(1) No loss of synchronization SHALL occur during measurements in MOP(6) and (7). (2) No increase of SES counter SHALL be reported in MOP(9).
NOTE1: Some MTC single components (e.g. R1, C8) may prevent system from reaching the Showtime, in which case the MELT measurement SHALL be skipped. NOTE2: Special foreign voltage value “OPEN” SHALL NOT be chosen.	

A Annex A MELT Test for the Composed Test Networks (Optional)

This Annex extends the test plan by adding an optional test (see Table 55) for the composed test network (CTN) shown in Figure 11. Four settings of the test network are defined in Table 51 to Table 54.

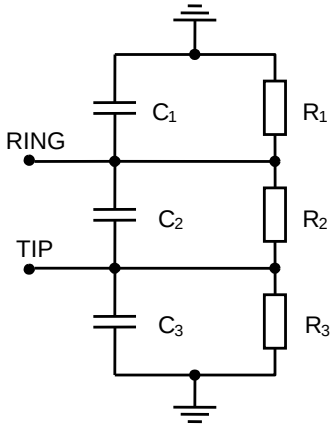

Figure 11: Composed test network (CTN)

Table 51: CTN_1 Components and accuracy limits

	Nominal value	Multimeter accuracy	Accuracy of MELT measurement	Accuracy of MELT measurement (SHDSL only)
R1	820 kΩ ± 5 %	± 1%	± 10%	± 10%
R2	910 kΩ ± 5 %	± 1%	± 10%	± 10%
R3	1 MΩ ± 5 %	± 1%	± 15%	± 15%
C1	200 nF ± 5%	± 1%	± 6%	± 8%
C2	33 nF ± 5%	± 1nF	± 20%	± 52nF (NOTE1)
C3	225 nF ± 5%	± 1%	± 6%	± 8%
NOTE1: Refer to NOTE4 in Table 54.				

Table 52: CTN_2 Components and accuracy limits

	Nominal value	Multimeter accuracy	Accuracy of MELT measurement	Accuracy of MELT measurement (SHDSL only)
R1	22 kΩ ± 5 %	± 1%	± 5%	± 5%
R2	25 kΩ ± 5 %	± 1%	± 5%	± 5%
R3	27 kΩ ± 5 %	± 1%	± 5%	± 5%
C1	50 nF ± 5%	± 1nF	± 10%	± 20%
C2	11 nF ± 5%	± 1nF	± 5nF	± 54nF (NOTE2)

C3	70 nF ± 5%	± 1nF	± 10%	± 20%
NOTE2: Refer to NOTE4 in Table 54.				

Table 53: CTN_3 Components and accuracy limits

	Nominal value	Multimeter accuracy	Accuracy of MELT measurement	Accuracy of MELT measurement (SHDSL only)
R1	10 kΩ ± 5 %	± 1%	± 5%	± 5%
R2	180 kΩ ± 5 %	± 1%	± 20%	± 20%
R3	220 kΩ ± 5 %	± 1%	± 20%	± 20%
C1	200 nF ± 5%	± 1%	± 6%	± 8%
C2	33 nF ± 5%	± 1nF	± 20%	± 52nF (NOTE3)
C3	225 nF ± 5%	± 1%	± 6%	± 8%
NOTE3: Refer to NOTE4 in Table 54.				

Table 54: CTN_4 Components and accuracy limits

	Nominal value	Multimeter accuracy	Accuracy of MELT measurement	Accuracy of MELT measurement (SHDSL only)
R1	820 kΩ ± 5 %	± 1%	± 10%	± 10%
R2	910 kΩ ± 5 %	± 1%	± 10%	± 10%
R3	1 MΩ ± 5 %	± 1%	± 15%	± 15%
C1	25 nF ± 5%	± 1nF	± 10nF	± 20nF
C2	1050 nF ± 5%	± 1%	± 10%	± 15% (NOTE4)
C3	30 nF ± 5%	± 1nF	± 10nF	± 20nF
NOTE4: The STU-C capacitance (typical 1µF) is much bigger than the C2 capacitance load (CTN_1, 2, 3) or of the same order of magnitude (CTN_4). Once the MELT measures C2 and STU-C capacitance in parallel, it is necessary to relax the accuracy limits with respect to the ADSL2plus/VDSL2 systems, where the ATU-C/VTU-O capacitance is rather small (typical 27nF).				

Table 55: MELT measurement for the combined test networks

Test Configuration	(1) See Figure 1 for the test setup. (2) See Table 51 to Table 54 for definition and tolerance limits of the composed test network (CTN). (3) Set DSL port to IDLE.

Method of Procedure	(1) Connect CTN_1 between TIP, RING and GND as shown in Figure 11. (2) Perform measurement of all R and C components. (3) Record the reported results of the MELT measurement. (4) Connect CTN_2 between TIP, RING and GND as shown in Figure 11. (5) Perform measurement of all R and C components. (6) Record the reported results of the MELT measurement. (7) Connect CTN_3 between TIP, RING and GND as shown in Figure 11. (8) Perform measurement of all R and C components. (9) Record the reported results of the MELT measurement. (10) Connect CTN_4 between TIP, RING and GND as shown in Figure 11. (11) Perform measurement of all R and C components. (12) Record the reported results of the MELT measurement.
Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds. (2) Measured resistance values SHALL be in the expected range of values defined in Table 51 to Table 54 with a granularity of 10 Ω. (3) Measured capacitance values SHALL be in the expected range of values defined in Table 51 to Table 54 with a granularity of 1 nF.

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