

TR-105 ADSL2/2plus Functionality Test Plan

Issue: 1 Corrigendum 1 Issue Date: April 2010

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Issue History

Issue Number	Issue Date	Issue Editor	Changes
1 Corrigendum 1	April 2010	Aleksandra Kozarev,	Corrigenda items for TR-105
		Lantiq	Issue 1

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Executive Summary

The document contains corrections to TR-105 Issue 1.

1 Purpose

The corrections specified in the following sections apply to TR-105 Issue 1.

2 Corrections in Section 5.5.1/TR-105, Bitswapping Test

Test procedure in bit swapping test (Section 5.5.1, Table 5-8 and Table 5-9) needs to specify at what end of the loop, ATU-R or ATU-C, the power of the interfering tone shall be increased.

2.1 Corrections in Table 5-8/TR-105

Update step (3) in the method of procedure in Table 5-8 as follows:

Table 5-8 DS Bit Swapping Test

Method of	(3) Randomly select an integer value, n, the tone number in the range of 70 to
Procedure	100 for ADSL2, and 300 to 400 for ADSL2plus. Ensure that the tone selected
	has assigned bits as described in the relevant bits per tone map. The power of
	the interfering tone SHALL be applied at the ATU-R side. Its power SHALL
	be -110 dBm or less.

2.2 Corrections in Table 5-9/TR-105

Update step (3) in the method of procedure in Table 5-9 as follows:

Table 5-9 US Bit Swapping Test

3 Correction to Table 6.5/TR-105

Test procedure for verification of the PSDMASKus configuration parameter (Section 6.4) needs to specify the loop type for Annex M.

Update step (1) in the method of procedure in Table 6-5 as follows:

Table 6-5 G.992.5 PSDMASKus control test

Method of	(1) Connect ATU-C and ATU-R through the 5kft 26AWG for Annex $A\underline{M}$ NA
Procedure	or 1500m PE04 for Annex $A\underline{M}$ EU and Annex \underline{B} and no noise injected.

End of Broadband Forum Technical Report TR-105