Fault Management for Multiservice Interworking over MPLS Version 1.0

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1 Introduction

1.1 Purpose and Scope

This specification provides fault management interworking procedures for the following multi-service interworking over MPLS scenarios:

1. FR-ATM service interworking over MPLS [5]. This extends FRF8.2 FR-ATM PVC service interworking [6] to operate across an MPLS core.

2. Transport of Ethernet-encapsulated information between dissimilar networks across an MPLS core [4].

3. Transport of IP-encapsulated information between dissimilar networks across an MPLS core, using the encapsulation specified in [1].

The MFA Forum may publish additional multi-service interworking specifications in the future, for which the fault management interworking procedures in this specification will apply. MFA Forum specifications are available at: http://www.mfaforum.org/tech/mpls_ia.shtml.

The following topics are not covered, and are for further study:

1. ATM ILMI Interworking.

2. The use of an inband pseudo wire (PW) method to notify the remote provider edge (PE) of the status of the PW.

2 Definitions and Terminology

2.1 Definitions

Must, Shall or Mandatory — the item is an absolute requirement of this specification.

Should — the item is desirable.

May or Optional — the item is not compulsory, and may be followed or ignored according to the needs of the implementer.

2.2 Acronyms and Abbreviations

The terminology specified in RFC 3985 [9] applies.

Acronym or Abbreviation	Definition
AC	Attachment Circuit
AIS	Alarm Indication Signal
ATM	Asynchronous Transfer Mode

BDI	Backward Defect Indication
CC	Continuity Check
CE	Customer Edge
CV	Connectivity Verification
FDI	Forward Defect Indication
FR	Frame Relay
ILMI	Integrated Link Management Interface
IP	Internet Protocol
LDP	Label Distribution Protocol
LMI	Link Management Interface
MPLS	Multiprotocol Label Switching
OAM	Operations and Maintenance
PE	Provider Edge
PSN	Packet Switched Network
PW	Pseudo Wire
RDI	Reverse Defect Indication
RSVP-TE	Resource Reservation Protocol with Traffic Engineering
TLV	Type Length Variable
VCCV	Virtual Circuit Connectivity Verification
VPWS	Virtual Private Wire Service

Table 1 Abbreviations

3 Generic OAM Interworking Principles

This document describes the handling of OAM in the case of faults in multi-service interworking over MPLS scenarios. The handling of OAM depends on the type of interworking scenario selected.

In multi-service interworking, a Provider Edge (PE) interworks or adapts an Attachment Circuit (AC) onto a PW (depending upon whether it terminates the attachment circuit, or the AC corresponds to the

native service for the PW). The other PE that terminates the PW is the "peer" PE; the attachment circuit associated with the far end PW termination is the "remote" AC.

Defects are described in the context of defect states, and the criteria to enter and exit the defect state.

The direction of defects is discussed from the perspective of the observing PE and what the PE may explicitly know about the information transfer capabilities of the Virtual Private Wire Service (VPWS) service.

A forward defect is one that impacts information transfer to the observing PE. It impacts the observing PE's ability to receive information. A forward defect may also imply impact on information sent or relayed by the observer (and as it cannot receive this information, a forward defect, is therefore invisible to it) and so the forward defect state is considered to be a superset of the two defect states.

A reverse defect is one that uniquely impacts information sent or relayed by the observer.

3.1 Defect Locations

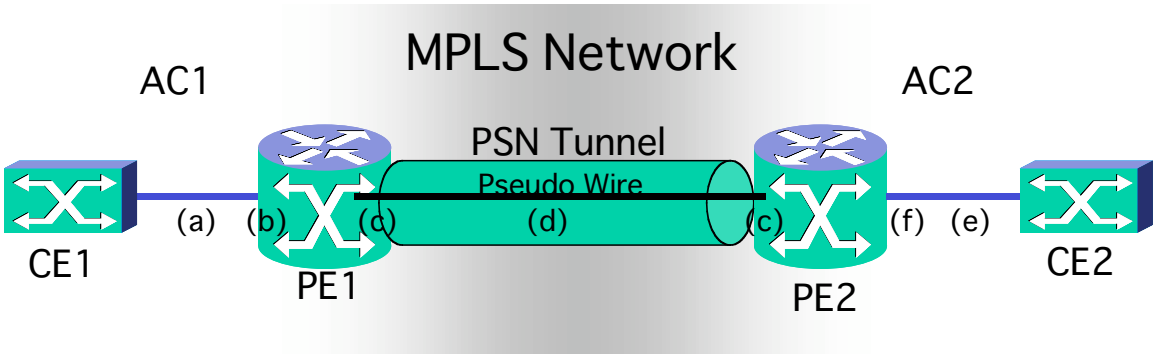

Figure 1 Defect Model for Multi-service interworking

Figure 1 shows the generic defect model for multi-service interworking. Defects are considered to occur at the following locations:

(a) Defect in the first Layer 2 network attached to PE1. This covers any defect in the network that impacts all or a subset of ACs terminating on PE1. The defect is conveyed to PE1 using a Layer 2-specific OAM defect indication.

(b) Defect on PE1 AC interface

(c) Defect on a PE MPLS interface.

(d) Defect in the MPLS network. This covers any defect in the packet-switched network (PSN) that impacts all or a subset of the PSN tunnels and PWs terminating in a PE. The defect is conveyed to the PE using an MPLS and/or a PW-specific OAM defect indication.

(e) Defect in the second Layer 2 network. This covers any defect in the network which impacts all or a subset of ACs terminating on PE2 (which is considered a remote AC defect in the

context of the procedures outlined in this document). The defect is conveyed to PE2 and to the remote Layer 2 network using a Layer 2-specific OAM defect indication.

(f) Defect on a PE2 AC interface.

3.2 Abstract Defect States

The PE is obliged to track four abstract defect states that reflect the observed state of both directions of the service on both the AC and the PW sides. Faults may impact only one or both directions of the PW. The observed state is a combination of faults directly detected by the PE, or faults that it has been made aware of via notifications. Figure 2 illustrates the forward and reverse defect states. Note that the arrows show the direction of traffic flow impacted by the defect. For example, when a PE goes into the forward defect state for the AC or the PW, it means that there is a defect affecting the traffic it is receiving on that interface.

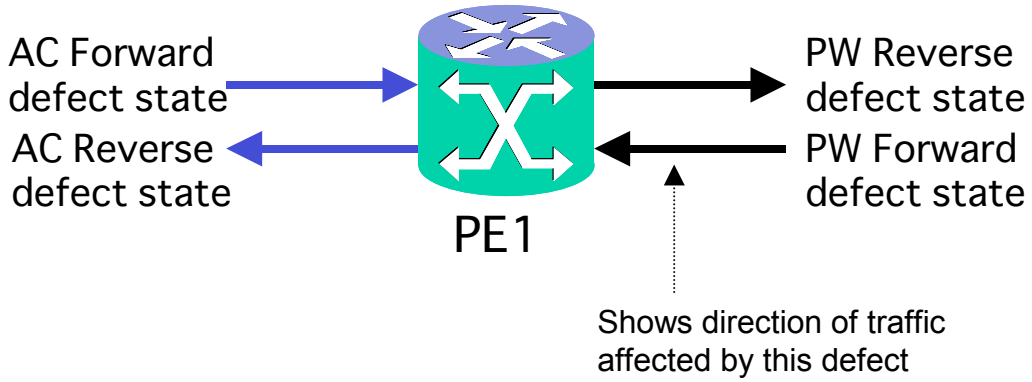

Figure 2 Forward and Reverse Defect States

When a PE has multiple sources of notification from a peer (e.g. MPLS and LDP control plane), it must track all sources, but the forward state always has precedence over the reverse state with regard to the consequent actions taken.

In the architecture shown in Figure 2, PE1 will directly detect or be notified of AC forward and PW forward defects as they occur upstream of PE1 and impact traffic being sent to PE1. PE1 may be notified of a forward defect in the AC by receiving a Forward Defect indication, e.g., ATM AIS, from CE1. This defect impacts the ability of PE1 to receive user traffic from CE1 on the AC. PE1 can also directly detect this defect if it resulted from a failure of the receive side in the local port or link over which the AC is configured. Similarly, PE1 may detect or be notified of a forward defect in the PW by receiving a Forward Defect indication from PE2. This notification can either be a "Local PSN-facing PW (egress) Transmit Fault" or a "Local Attachment Circuit (ingress) Receive Fault". This defect impacts the ability of PE1 to receive user traffic from CE2. Note that the AC or PW Forward Defect notification is sent in the same direction as the user traffic impacted by the defect.

PE1 will only be notified of AC reverse and PW reverse defects as they will universally be detected by other devices and only impact traffic that has already been relayed by PE1. PE1 may be notified of a reverse defect in the AC by receiving a Reverse Defect indication, e.g., ATM RDI, from CE1. This defect impacts the ability of PE1 to send user traffic to CE1 on the AC. Similarly, PE1 may be notified of a reverse defect in the PW by receiving a Reverse Defect indication from PE2. This notification can either be a "Local PSN-facing PW (ingress) Receive Fault" or a "Local Attachment Circuit (egress) Transmit

Fault". This defect impacts the ability of PE1 to send user traffic to CE2. Note that the AC or PW Reverse Defect notification is sent in the reverse direction to the user traffic impacted by the defect.

The procedures outlined in this document define the entry and exit criteria for each of the four states with respect to the set of potential ACs and PWs within the scope of the document, and the consequent actions that PE1 must perform to properly interwork those notifications. The abstract defect states used by PE1 are common to all potential interworking combinations of PWs and ACs.

Code points for forward defect and reverse defect notifications have not been specified for PW Status signaling. In this version of this Specification we refer to "forward defect" and "reverse defect" indications as placeholders for code point assignment. The following mapping may be performed between code points defined in [3].

Forward defect - corresponds to:

[Local Attachment Circuit (ingress) Receive Fault

Logical OR

Local PSN-facing PW (egress) Transmit Fault]

Reverse defect - corresponds to:

[Local Attachment Circuit (egress) Transmit Fault

Logical OR

Local PSN-facing PW (egress) Transmit Fault]

3.3 Pseudo Wire Defect State Entry and Exit Criteria

The following subsections refer to Figure 1 when describing directionality.

3.3.1 PW Forward Defect State Entry

PE1 enters the Forward Defect state if any of the following conditions are met:

(i) It detects or is notified of a defect upstream of PE1 in the PSN tunnel over which the PW is riding. Defects detected explicitly include loss of connectivity, label swapping errors, and label merging errors. These defects can be detected by running a MPLS-specific connectivity verification mechanism such as LSP-Ping [6], or Y.1711 CV [8]. The assumption is that deployed PSN resiliency mechanisms have not been sufficient to recover from the defect, and restore connectivity to the peer PE. Notifications of defects remote from the PE include Y.1711 FDI/BDI, and RSVP-TE PathErr message.

(ii) It receives a message from the remote PE indicating a forward defect. In the case of a MPLS PSN and a MPLS-IP PSN, this is a PW status message [1]. The use of other forward defect indications is for surther study.

(iii) It detects a loss of PW connectivity, including label errors, via an inband PW OAM connectivity verification tool, such as VCCV.

Note that if the PW control session between the PEs fails, the PW is torn down and has to be re-established. However, the consequent actions towards the ACs are the same as if the PW state were DOWN.

3.3.2 PW Reverse Defect State Entry

PE1 enters the PW Reverse Defect state when it receives a Label Distribution Protocol (LDP) status Type Length Variable (TLV) indicating a reverse defect. The use of other defect indication mechanisms is for further study.

3.3.3 PW Reverse Defects that Require PE State Synchronization

Some PW mechanisms will result in PW defects being detected by or notified to PE1 when PE1 is upstream of the fault but the notification did not originate with PE2. The resultant actions are identical to that of entering the PW Reverse Defect state, with the addition that PE1 needs to synchronize states with PE2, and the PW state communicated from PE1 to PE2 needs to indicate the state accordingly.

When the PSN uses RSVP-TE, or proactively uses LSP-Ping as a PW fault detection mechanism, PE1 must enter the AC Forward Defect state. The exit criteria is when the RSVP fault state or the LSP-Ping fault state exit criteria has been met, indicating no PW reverse defects.

3.3.4 PW Forward Defect State Exit

PE1 exits the PW Forward Defect state when both of the following conditions are true:

(i) The status communicated by PE2 via the LDP status TLV no longer indicates a forward defect. The use of other defect indication mechanisms is for further study.

(ii) Local indications indicate that PW and PSN connectivity exists in the forward direction. Note that this may result in a transition to the PW Working or the PW Reverse Defect states.

3.3.5 PW Reverse Defect State Exit

PE1 exits the PW Reverse Defect state when the status communicated by PE2 via LDP status TLV no longer indicates a reverse defect. The use of other defect indication mechanisms is for further study.

3.4 ATM Attachment Circuit Defect State Entry/Exit Criteria

3.4.1 Forward Defect State Entry

PE1 enters the AC forward defect state if any of the following conditions are met:

(i) It detects a physical layer alarm on the ATM interface.

(ii) It receives an F5 AIS OAM cell indicating that the ATM VP/VC is down in the adjacent ATM network (e.g. AC1 for PE1).

(iii) It detects loss of connectivity on the ATM VPC/VCC while running ATM continuity checking (ATM CC) with the local ATM network and CE.

Note that all interworking with ATM referred to in this document makes use of ATM VCCs as the AC. An ATM VPC cannot be terminated directly on an interworking function. Therefore only F5 OAM messages are relevant.

3.4.2 Forward Defect State Exit

PE1 exits the AC Forward Defect state when all defects it had previously detected have disappeared. The exact conditions under which a PE exits the AIS state or declares that connectivity is restored via ATM CC are explained in I.610 [2]. Note that it is possible to transition directly from the Forward to the Reverse Defect states.

3.4.3 Reverse Defect State Entry

PE1 enters the AC Reverse Defect state if it terminates the ATM layer and it receives an F5 RDI OAM cell indicating that the ATM VP/VC is down in the adjacent ATM network. The AC reverse defect state effectively equates to the ATM RDI state.

3.4.4 Reverse Defect State Exit

PE1 exits the AC Reverse Defect state if any of the following are true:

(i) It enters the Forward Defect state.

(ii) All defects it had previously detected have disappeared. The exact conditions under which a PE exits the RDI state are explained in I.610 [2].

3.5 Frame Relay Attachment Circuit Defect State Entry/Exit Criteria

Note that the FR AC “inactive” state, as communicated by the FR LMI, does not indicate direction but is assumed to be the equivalent of a forward defect and is translated to be the same. The Reverse Defect state is not valid for a FR AC.

3.5.1 Forward Defect State Entry

PE1 enters the AC Forward Defect state if any of the following conditions are met:

(i) A PVC is not “deleted” from the Frame Relay network and the Frame Relay network explicitly indicates in a full status report (and optionally by the asynchronous status message) that this Frame Relay PVC is “inactive”. In this case, this status maps across the PE to the corresponding PW only.

(ii) The LIV indicates that the link from the PE to the Frame Relay network is down. In this case, the link down indication maps across the PE to all corresponding PWs.

(iii) A physical layer alarm is detected on the Frame Relay interface. In this case, this status maps across the PE to all corresponding PWs.

3.5.2 Forward Defect State Exit

A PE exits the FR AC Down state when all defects it had previously detected have disappeared.

3.6 Ethernet Attachment Circuit Defect State Entry/Exit Criteria

Ethernet AC failures are translated directly into AC forward defects. The reverse defect state is not valid for Ethernet ACs. Current Ethenet standards do not specify an in-band mechanism for Ethernet defect notifications. Such mechanisms are for further study.

3.6.1 Forward Defect State Entry

PE1 enters the AC Forward Defect state if a physical layer alarm is detected on the Ethernet interface.

3.6.2 Forward Defect State Exit

A PE exits the Ethernet AC Down state when all defects it had previously detected have disappeared.

4 FR-ATM Interworking over MPLS Procedures

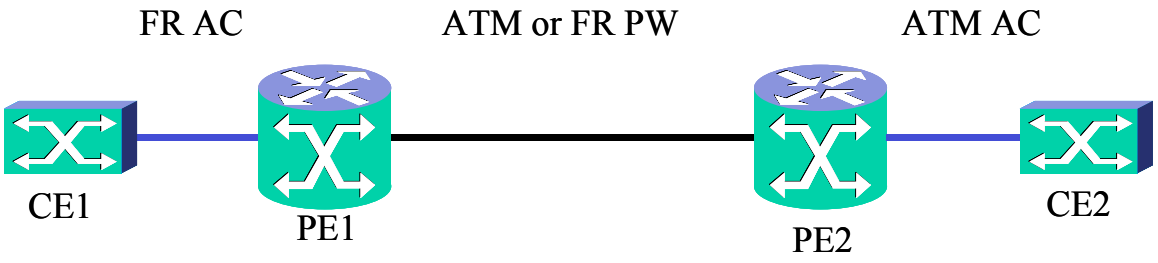

Figure 3 FR-ATM Interworking over MPLS

Figure 3 shows the reference model for Frame Relay to ATM interworking over MPLS. The section following references this figure.

4.1 Attachment Circuit Defect Entry / Exit Procedures

4.1.1 AC Forward Defect Entry

On entry into the forward defect state a PE may need to perform procedures on both the PW and the AC.

4.1.1.1 Procedures for FR and ATM AAL5 PWs

On entry into the AC Forward Defect state, the PE notifies the remote PE of a forward defect using a PW Status message indicating “forward defect”. The use of other defect indication mechanisms is for further study.

4.1.1.2 Procedures for ATM Cell PWs

On entry into the AC Forward Defect state the PE shall:

(i) Commence insertion of ATM AIS cells into the corresponding PW.

(ii) Suspend CC generation for the duration of the defect state, if it (PE1) is originating F5 I.610 CC cells.

4.1.1.3 Additional procedures for ATM ACs

On entry into the AC Forward Defect state PE2 shall commence RDI insertion into the AC as per I.610.

4.1.2 AC Reverse Defect Entry

4.1.2.1 Procedures for FR and ATM AAL5 PWs

On entry into the AC Reverse Defect state a PE notifies the remote PE of a reverse defect using a PW Status message indicating “reverse defect”. The use of other defect indication mechanisms is for further study.

4.1.2.2 Procedures for ATM Cell PWs

An ATM AC would be the only potential source of AC Reverse Defect state within the scope of this document. However, there are no procedures in this case as the AC Reverse Defect state is not valid for PE1 with an ATM AC and an ATM cell mode PW.

4.1.3 AC Forward Defect Exit

4.1.3.1 Procedures for FR and ATM AAL5 PWs

(i) On exit from the AC Forward Defect state a PE notifies the remote PE that the reverse defect state has cleared (note that this may be a direct state transition to either the working state or the forward defect state). This is indicated by a PW Status message showing all failures cleared or a transition to the “reverse defect” state. The use of other defect indication mechanisms is for further study.

4.1.3.2 Procedures for ATM Cell PWs

On exit from the AC Forward Defect state PE1 shall:

(i) Cease insertion of ATM AIS cells into the corresponding PW.

(ii) Resume CC generation if it (PE1) is originating F5 I.610 CC cells.

If the transition is to the AC Reverse Defect state, the corresponding procedures apply.

4.1.3.3 Additional Procedures for ATM ACs

On exit from the forward defect state PE1 shall cease RDI insertion into the AC as per I.610.

4.1.4 AC Reverse Defect Exit

4.1.4.1 Procedures for FR or ATM AAL5 PWs

On exit from the AC Reverse Defect state PE2 notifies the remote PE that the reverse defect state has cleared (note that this may be a direct state transition to either the working state or the forward defect state). This is indicated by a PW Status message showing all failures cleared, or a transition to the "forward defect" state. The use of other defect indication mechanisms is for further study.

4.1.4.2 Procedures for ATM cell PWs

An ATM AC would be the only potential source of the AC Reverse Defect state within the scope of this document. However, there are no procedures in this case as the AC Reverse Defect state is not valid for a PE with an ATM AC and an ATM cell mode PW.

4.2 Pseudo Wire Defect Entry / Exit Procedures

4.2.1 PW Forward Defect Entry

4.2.1.1 FR AC Procedures

These procedures are applicable only if the transition is from the working state to the PW Forward Defect state. A transition from PW Reverse Defect state to the PW Forward Defect state does not require any additional notification procedures to the FR AC as it has already been told that the peer is down.

PE1 shall generate a Full Status report with the Active bit = 0 (and optionally in the asynchronous status message), as per Q.933 annex A, into the FR network, for the corresponding FR ACs.

4.2.1.2 ATM AC Procedures

On entry into the PW Forward Defect State:

(i) PE2 shall commence F5 AIS insertion into the corresponding AC.

(ii) PE2 shall terminate any F5 CC generation on the corresponding AC.

4.2.1.3 Additional procedures for FR and ATM AAL5 PWs

If a PE explicitly detected the PW failure, it shall assume that the remote PE has no knowledge of the defect, and shall notify the remote PE in the form of a PW Status message indicating a "reverse defect". The use of other defect indication mechanisms is for further study.

Otherwise the entry into the defect state was the result of a notification from the remote PE (indicating that the remote PE already had knowledge of the fault) or loss of the control adjacency (similarly visible to the remote PE).

4.2.1.4 Additional procedures for ATM Cell PWs

If a PE explicitly detected the PW failure, causing it to enter the ATM AIS state, through loss of CC or a locally detected failure, the PE shall also commence RDI insertion into the reverse direction of the PW.

4.2.2 PW Forward Defect Exit

4.2.2.1 FR AC Procedures

On transition from the PW Forward Defect state to the PW Rreverse Defect state PE1 takes no action with respect to the AC.

On exit from the PW Forward Defect state PE1 shall generate a Full Status report with the Active bit = 1 (and optionally in the asynchronous status message), as per Q.933 annex A, into the FR network, for the corresponding FR ACs.

4.2.2.2 ATM AC Procedures

On exit from the PW Forward Defect State

(i) PE2 shall cease F5 AIS insertion into the corresponding AC.

(ii) PE2 shall resume any F5 CC generation on the corresponding AC.

4.2.2.3 Additional procedures for FR and ATM AAL5 PWs

If a PE explicitly detected the PW failure, it shall notify the remote PE by clearing the reverse defect notification using a PW Status message showing all failures cleared, or a transition to the "forward defect" state. The use of other defect indication mechanisms is for further study.

4.2.2.4 Additional procedures for ATM Cell PWs

On exit from the PW Forward Defect state the PE will cease F5 RDI generation into the corresponding PW.

4.2.3 PW Reverse Defect Entry

4.2.3.1 FR AC procedures

On transition from the PW Forward Defect state to the PW Reverse Defect state PE1 takes no action with respect to the AC.

On entry into the PW Forward Defect state PE1 shall generate a Full Status report with the Active bit = 0 (and optionally in the asynchronous status message), as per Q.933 annex A, into the frame relay network, for the corresponding FR ACs.

4.2.3.2 ATM AC procedures

On entry into the PW Reverse Defect State PE2 shall commence F5 RDI insertion into the corresponding AC.

4.2.4 PW Reverse Defect Exit

4.2.4.1 FR AC procedures

On transition from the PW Reverse Defect state to the PW Forward Defect state PE1 takes no action with respect to the AC.

On exit from the PW Reverse Defect state PE1 shall generate a Full Status report with the Active bit = 1 (and optionally in the asynchronous status message), as per Q.933 annex A, into the FR network, for the corresponding FR ACs.

4.2.4.2 ATM AC Procedures

On exit from the PW Reverse Defect State PE2 shall cease F5 RDI insertion into the corresponding AC.

5 ATM-Ethernet Interworking over MPLS Procedures

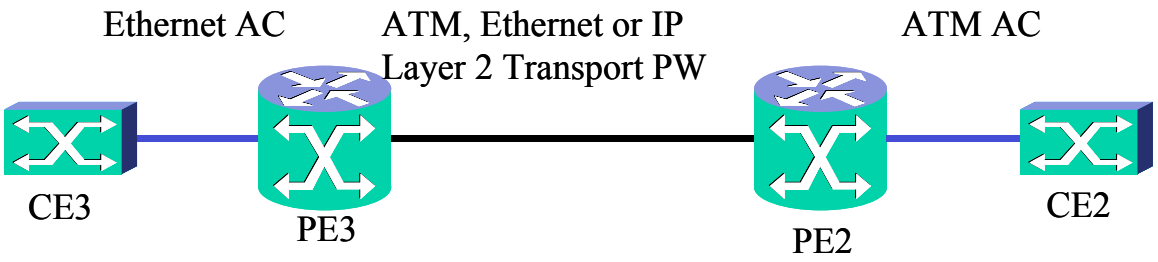

Figure 4 ATM-Ethernet Interworking over MPLS

Figure 4 shows the reference model for Ethernet to ATM interworking over MPLS. The section following refers to this figure.

5.1 Attachment Circuit Defect Entry / Exit Procedures

5.1.1 AC Forward Defect Entry

On entry into the AC Forward Defect state a PE may need to perform procedures on both the PW and the AC.

5.1.1.1 Procedures for Ethernet, IP Layer 2 Transport, and ATM AAL5 PWs

On entry into the AC Forward Defect state the PE notifies the remote PE of a forward defect using a PW Status message indicating “forward defect”. The use of other defect indication mechanisms is for further study.

5.1.1.2 Procedures for ATM Cell PWs

On entry into the AC Forward Defect state the PE shall:

(i) Commence insertion of ATM AIS cells into the corresponding PW.

(ii) Suspend CC generation for the duration of the defect state if it is originating I.610 F5 CC cells .

5.1.1.3 Additional procedures for ATM ACs

On entry into the AC Forward Defect state PE2 shall commence RDI insertion into the AC as per I.610.

5.1.2 AC Reverse Defect Entry

5.1.2.1 Procedures for Ethernet, IP Layer 2 Transport, and ATM AAL5 PWs

On entry into the AC Reverse Defect state PE2 notifies the remote PE of a reverse defect usinga PW Status message indicating “reverse defect”. The use of other defect indication mechanisms is for further study.

5.1.2.2 Procedures for ATM Cell PWs

An ATM AC would be the only potential source of the AC Reverse Defect state within the scope of this document. However, there are no procedures in this case as the AC Reverse defect state is not valid for PE1 with an ATM AC and an ATM cell mode PW.

5.1.3 AC Forward Defect Exit

5.1.3.1 Procedures for Ethernet, IP Layer 2 Transport, and ATM AAL5 PWs

On exit from the AC Forward Defect state a PE notifies the remote PE that the forward defect state has cleared (note that this may be a direct state transition to either the working state or the reverse defect state). This is done using a PW Status message showing all failures cleared, or a transition to the “reverse defect” state. The use of other defect indication mechanisms is for further study.

5.1.3.2 Procedures for ATM Cell PWs

The ATM AC would be the only potential source of the AC Reverse Defect state within the scope of this document. However, there are no procedures in this case as the AC Reverse Defect state is not valid for a PE with an ATM AC and an ATM cell mode PW.

5.1.3.3 Additional Procedures for ATM ACs

On exit from the forward defect state PE1 shall cease RDI insertion into the AC as per I.610.

5.1.4 AC Reverse Defect Exit

5.1.4.1 Procedures for Ethernet, IP Layer 2 Transport, or ATM AAL5 PWs

On exit from the AC Reverse Defect state PE2 notifies the remote PE that the reverse defect state has cleared (note that this may be a direct state transition to either the working state or the forward defect state). This is done using a PW Status message showing all failures cleared, or a transition to the “forward defect” state. The use of other defect indication mechanisms is for further study.

5.1.4.2 Procedures for ATM cell PWs

The ATM AC would be the only potential source of the AC Reverse Defect state within the scope of this document. However, there are no procedures in this case as the AC Reverse Defect state is not valid for PE2 with an ATM AC and an ATM cell mode PW.

5.2 Pseudo Wire Defect Entry / Exit Procedures

5.2.1 PW Forward Defect Entry

5.2.1.1 Ethernet AC Procedures

These procedures are for further study.

5.2.1.2 ATM AC Procedures

On entry to the PW Forward Defect State:

(i) PE2 shall commence F5 AIS insertion into the corresponding AC.

(ii) PE2 shall terminate any F5 CC generation on the corresponding AC.

5.2.1.3 Additional procedures for Ethernet, IP Layer 2 Transport, and ATM AAL5 PWs

If a PE explicitly detected the PW failure, it shall assume that the remote PE has no knowledge of the defect, and shall notify the remote PE in the form of a reverse defect notification using a PW Status message indicating all defects cleared. The use of other defect indication mechanisms is for further study.

Otherwise the entry to the defect state was the result of a notification from the remote PE (indicating that the remote PE already had knowledge of the fault) or loss of the control adjacency (similarly visible to the remote PE).

5.2.1.4 Additional procedures for ATM Cell PWs

If the PW failure was explicitly detected by a PE causing it toenter the ATM AIS state, through loss of CC or a locally detected failure, the PE shall also commence RDI insertion into the reverse direction of the PW.

5.2.2 PW Forward Defect Exit

5.2.2.1 Ethernet AC Procedures

These procedures are for further study..

5.2.2.2 ATM AC Procedures

On exit from the PW Forward Defect State

(i) PE2 shall cease F5 AIS insertion into the corresponding AC.

(ii) PE2 shall resume any F5 CC generation on the corresponding AC.

5.2.2.3 Additional procedures for Ethernet, IP Layer 2 Transport, and ATM AAL5 PWs

If a PE explicitly detected the PW failure, it shall notify the remote PE by clearing the reverse defect notification using a PW Status message with the "reverse defect" indication clear, and the remaining indicators showing either working or a transition to the "forward defect" state. The use of other defect indication mechanisms is for further study.

5.2.2.4 Additional procedures for ATM Cell PWs

On exit from the PW Forward Defect state the PE shall cease F5 RDI generation into the corresponding PW.

5.2.3 PW Reverse Defect Entry

5.2.3.1 Ethernet AC Procedures

These procedures are for further study.

5.2.3.2 ATM AC procedures

On entry into the PW Reverse Defect State PE2 shall commence F5 RDI insertion into the corresponding AC.

5.2.4 PW Reverse Defect Exit

5.2.4.1 Ethernet AC Procedures

These procedures are for further study.

5.2.4.2 ATM AC Procedures

On exit from the PW Reverse Defect State PE2 shall cease F5 RDI insertion into the corresponding AC.

6 FR-Ethernet Interworking over MPLS Procedures

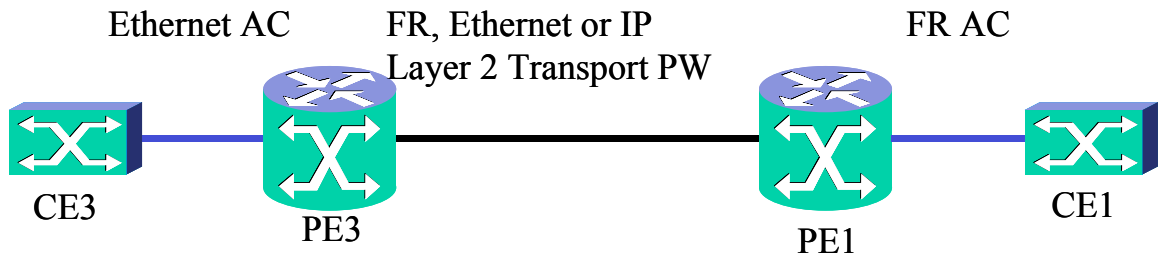

Figure 5 FR-Ethernet Interworking over MPLS

Figure 5 shows the reference model for Ethernet to Frame relay multi-service interworking. The section following refers to this figure.

6.1 Attachment Circuit Defect Entry / Exit Procedures

6.1.1 AC Forward Defect Entry

On entry into the AC Forward Defect state a PE may need to perform procedures on both the PW and the AC.

6.1.1.1 Procedures for Ethernet, IP Layer 2 Transport, and FR PWs

On entry into the AC Forward Defect state the PE notifies the remote PE of a forward defect using a PW Status message indicating “forward defect”. The use of other defect indication mechanisms is for further study.

6.1.2 AC Forward Defect Exit

6.1.2.1 Procedures for Ethernet, IP Layer 2 Transport, and FR PWs

On exit from the AC Forward Defect state a PE notifies the remote PE that the forward defect state has cleared. This will be a PW Status message indicating all failures cleared. The use of other defect indication mechanisms is for further study.

6.2 Pseudo Wire Defect Entry / Exit Procedures

6.2.1 PW Forward Defect Entry

6.2.1.1 Ethernet AC Procedures

These procedures are for further study.

6.2.1.2 FR AC Procedures

These procedures are applicable only if the transition is from the working state to the PW Forward Defect state. A transition from PW Reverse Defect state to the PW Forward Defect state does not require any additional notification procedures to the FR AC as it has already been told that the peer is down.

PE1 shall generate a Full Status report with the Active bit = 0 (and optionally in the asynchronous status message), as per Q.933 annex A, into the FR network for the corresponding FR ACs.

6.2.1.3 Additional procedures for Ethernet, IP Layer 2 Transport, and FR PWs

If a PE explicitly detected the PW failure, it shall assume that the remote PE has no knowledge of the defect and shall notify the remote PE in the form of a PW Status message indicating a “forward defect”. The use of other defect indication mechanisms is for further study.

Otherwise the entry into the defect state was the result of a notification from the remote PE (indicating that the remote PE already had knowledge of the fault) or loss of the control adjacency (similarly visible to the remote PE).

6.2.2 PW Forward Defect Exit

6.2.2.1 FR AC Procedures

On transition from the PW Forward Defect state to the PW Reverse Defect state PE1 takes no action with respect to the AC.

On exit from the PW Forward Defect state PE1 shall generate a Full Status report with the Active bit = 1 (and optionally in the asynchronous status message), as per Q.933 annex A, into the FR network, for the corresponding FR ACs

6.2.2.2 Ethernet AC Procedures

These procedures are for further study.

6.2.2.3 Additional procedures for Ethernet, IP Layer 2 Transport, and FR PWs

If a PE explicitly detected the PW failure, it shall notify the remote PE by clearing the reverse defect notification using a PW Status message showing all failures cleared or a transition to the "forward defect" state. The use of other defect indication mechanisms is for further study.

6.2.3 PW Reverse Defect Entry

6.2.3.1 FR AC procedures

On transition from the PW Forward Defect state to the PW Reverse Defect state PE1 takes no action with respect to the AC.

On entry into the PW Forward Defect state PE1 shall generate a Full Status report with the Active bit = 0 (and optionally in the asynchronous status message), as per Q.933 annex A, into the frame relay network, for the corresponding FR ACs.

6.2.3.2 Ethernet AC Procedures

These procedures are for further study.

6.2.4 PW Reverse Defect Exit

6.2.4.1 FR AC procedures

On transition from the PW Reverse Defect state to the PW Forward Defect state PE1 takes no action with respect to the AC.

On exit from the PW Reverse Defect state PE1 shall generate a Full Status report with the Active bit = 1 (and optionally in the asynchronous status message), as per Q.933 annex A, into the FR network, for the corresponding FR ACs.

6.2.4.2 Ethernet AC Procedures

These procedures are for further study.

7 References

7.1 Normative References

[1] RFC 4447, “Pseudowire Setup and Maintenance using the Label Distribution protocol (LDP)”, April 2006

[2] ITU-T Recommendation I.610, “B-ISDN operation and maintenance principles and functions”, January 1999.

[3] Internet Assigned Numbers Authority (IANA); "Pseudo Wire Status Codes Registry"; http://www.iana.org/assignments/pwe3-parameters

7.2 Informative References

[4] Cherukuri, R; " Multi-Service Interworking Ethernet Service over MPLS"; MFA Forum 12.0.0; June 2006

[5] Hunt, D; " Multi-Service Interworking – Frame Relay and ATM Service Interworking over MPLS"; mpls2005.097.00; August 2005

[6] Frame Relay Forum, “FRF 8.2 - Frame Relay / ATM PVC Service Interworking Implementation Agreement”, February 2004.

[7] RFC 4379; “Detecting Multi-Protocol Label Switching (MPLS) Data Plane Failures”, February 2006

[8] ITU-T Recommendation Y.1711, “OAM Mechanisms for MPLS Networks”, November 2002.

[9] RFC 3985; " Pseudo Wire Emulation Edge-to-Edge (PWE3) Architecture"; March 2005

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