INVITED PAPER

Through-Silicon Via (TSV)

This technology allows stacked silicon chips to interconnect through direct contact to provide high-speed signal processing and improved photo detection for image sensing.

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ABSTRACT | Recently, the development of three-dimensional large-scale integration (3D-LSI) has been accelerated. Its stage has changed from the research level or limited production level to the investigation level with a view to mass production [1]–[10]. The 3D-LSI using through-silicon via (TSV) has the simplest structure and is expected to realize a high-performance, high-functionality, and high-density LSI cube. This paper describes the current and future 3D-LSI technologies with TSV.

KEYWORDS | Chip size package (CSP); image sensor; micro bump; three-dimensional large-scale integration (3D-LSI); through-silicon via (TSV)

I. INTRODUCTION

Semiconductor integration technology has been widely spread in two-dimensional applications over the past three decades. This wide application has been employed not only in the field of the electronics industries but also in a lot of related industries such as optoelectronics, bioelectronics, medical systems, electronics analysis, computer systems, military systems, satellite systems, submarine systems, and so on. From the consumer area to ultra-high-end products and military usage, almost all industrial products incorporate semiconductor devices. One significant reason for this rapid progress is the good scalability of metal–oxide–semiconductor (MOS) devices [11]. But recently the actual device has begun to deviate from the ideal scaling theory. The main cause is difficulty of operation voltage scaling. The value of kT/q does not scale down, and thus lowering threshold voltage (Vth) of an MOS transistor is difficult without increasing subthreshold leakage. Without Vth scaling, power and performance became a tradeoff. Under this circumstance, in order to bring out high performance from LSI chips while restricting their power, there are two approaches. One is reconsidering circuits and system architecture from view point of power consumption. Another is concerning LSI structure. In recent devices, the signal propagation delay is mainly determined by wiring length and pin capacitance. Three-dimensional large-scale integration (3D-LSI) is the one solution to improve performance without increase of power consumption. One of the key issues to realize 3D-LSI is the method of information transfer and the supply of electric power among stacked chips. There are many methods to connect interchip, such as wire-bonding, edge connect, capacitive or inductive coupling method [12]–[17], and direct contact using through-silicon via (TSV). Fig. 1 shows the TSV technology road map. In this figure, there are two technologies. The upper line is for the current 3D-LSI structure in which the TSVs are formed under the peripheral bond pads. In this case, TSV design can be relaxed up to the bond pad pitch. Although the performance can be improved, the main advantages of this technology are improving form-factor without the modification of the original LSI chip layout. The lower line is for advanced 3D-LSIs. In order to facilitate the performance of

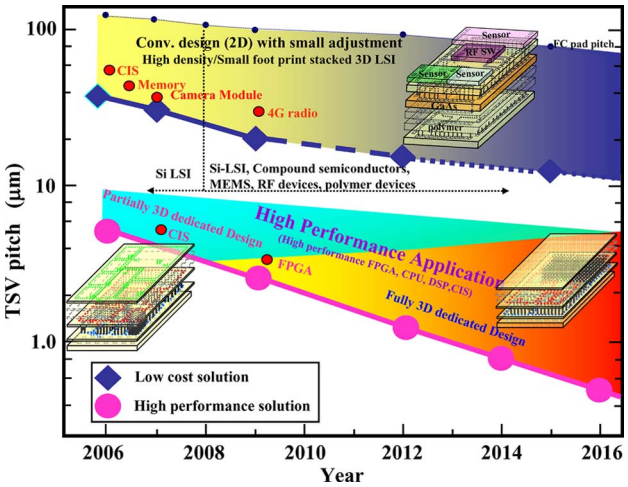

Fig. 1. *TSV for 3D-LSI technology road map.*

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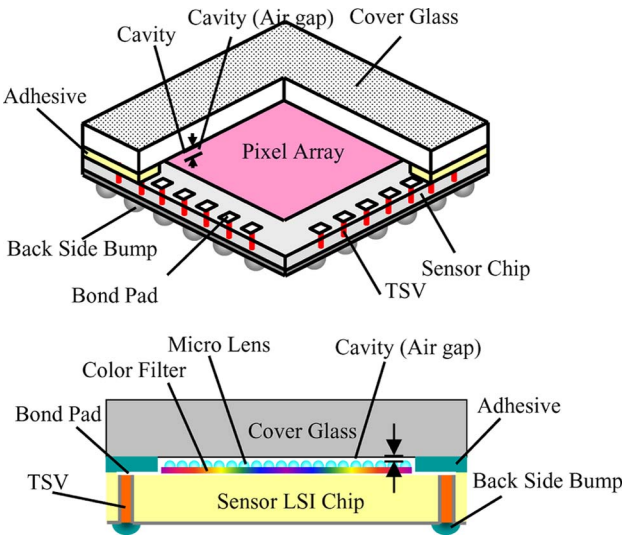

Fig. 2. *Schematic view of a new CSP structure for sensor application.*

3D-LSI, the circuit blocks in stacked chips need to connect directly with fine pitch TSVs and microbumps. Therefore, to avoid chip area penalty, their pitches need to be shrunk to less than 5 μm. Aside from the fabrication technology, many issues, such as three-dimensional computer-aided design (3D-CAD), test, heat removal, reliability assurance, supply chain supply chain of base LSI chips, application definition, etc., need to be settled simultaneously.

II. CURRENT 3D-LSI USING TSV

A. CSP Technology for Image Sensor

At the development stage, it is important to fix the target application. In an ideal image sensor, pinouts are preferably located on the opposite side from the sensor array. Fig. 2 shows the schematic view of a new chip size package (CSP) for sensor applications. This does not have a real 3-D LSI structure with stacked chips, but it applies many of the same technology features such as TSV, wafer thinning, and bump formation. Therefore it is a suitable vehicle to develop the 3D-LSI process module and easy to expand to the real 3D-stacked structure, which could include a sensor with digital signal processor (DSP) or a sensor with memory and DSP, etc. There are two issues in applying this technology to an image sensor device. One is keeping low temperature during the fabrication process because the thermal stability of the polymer microlens and the color filter is less than 200 °C. This process is analogous with the complementary MOS (CMOS) back end of line (BEOL) process. However, the process temperature of most typical BEOL unit processes is around 350 °C. Therefore, it is necessary to lower the unit process temperature to 200 °C and optimize it carefully without degradation of reliability. Another issue is avoiding the degradation of the optical characteristics during the processes. At the finished wafer stage, the surface of the pixel array is not covered with a passivation layer, which is different from other LSI chips.

B. New CSP Process [9], [18], [19]

This process uses the dead area under bond pads. The process sequence for making the new chip size package is shown in Fig. 3. After finishing the LSI process, a handle wafer is attached to the sensor LSI wafer by adhesive film, followed by wafer thinning down to about 100 μm by back grinding and polishing [Fig. 3(a)]. Subsequent process steps for TSV formation are shown in Fig. 3(b). Backside deep Si etch and successive SiO_2 etch process with photoresist mask forms through holes. Fig. 4 shows scanning electron microscope (SEM) images of 60×60 μm^2 rectangular type TSVs after deep Si etch. Fig. 5 shows a focused ion beam (FIB)-prepared cross-sectional SEM image of a 60 μm diameter through-hole with a depth of 100 μm. This sample was prepared by FIB and XeF_2 etching with amorphous carbon as etching mask. Optimizing Si/SiO_2 etch selectivity and Si etch rate, we can suppress the notch at the $Si–SiO_2$ interface. After making sidewall insulation, the through hole is filled with conductive material. Then the handle wafer is replaced with a cover glass. This is a process peculiar to sensor applications [Fig. 3(c)]. Then, after forming backside

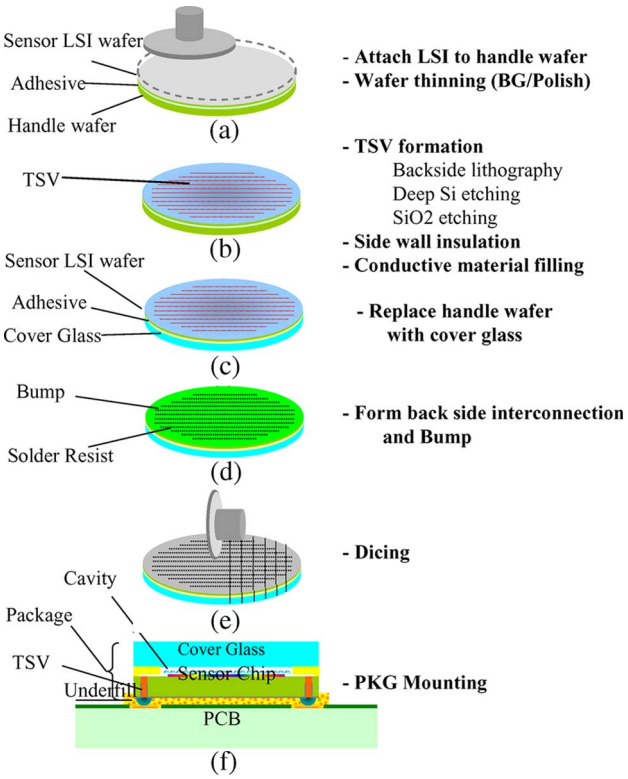

Fig. 3. *New CSP process flow.*

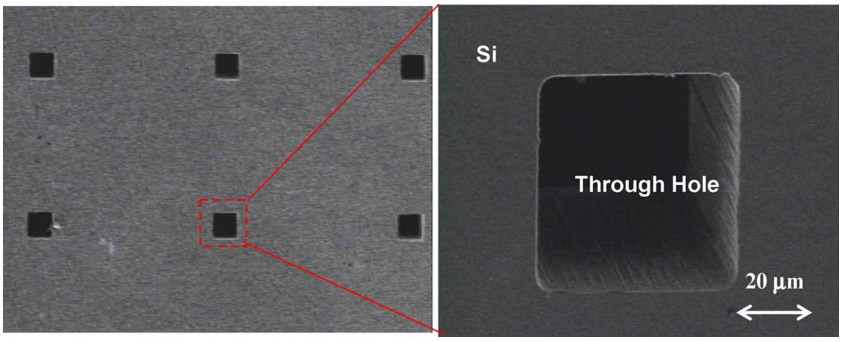

Fig. 4. *A SEM image of 60 × 60 μm^2 TSVs after deep Si etch.*

interconnection and bumps [Fig. 3(d)], the sensor wafer with cover glass is diced into the sensor chips [Fig. 3(e)]. Fig. 6 shows a cross-sectional photo image of the CSP mounted on a module test board. The sensor LSI chip is connected via TSV, backside interconnect, and Pb-free solder bump with printed circuit board. The total thickness of this sample (from bump to the surface of the cover glass) is about 0.64 mm.

C. TSV Filling Process

There are several candidates for the TSV filling process. Filling with conductive paste is a promising technology to reduce process cost. Fig. 7 illustrates the process sequence of this technique. After thinning the LSI processed wafer, through holes are formed by deep Si etch and successive SiO_2 reactive ion etch (RIE) with photoresist mask to expose the bottom side of the bonding pad [Fig. 7(a) and (b)]. Then the side-wall insulator is formed using low-temperature plasma-enhanced chemical vapor deposition (PECVD) SiO_2 deposition and subsequent SiO_2 RIE [Fig. 7(c)]. Optimizing PECVD and RIE conditions, only the bottom oxide of the through hole is completely removed to expose the backside of pad metal. After contact metal and diffusion barrier metal deposition, conductive paste is filled by printing technique [Fig. 7(d) and (e)]. Lastly, the contact metal and the diffusion barrier metal at the back side surface of the wafer are removed [Fig. 7(f)]. Fig. 8 shows a cross-sectional view of TSVs filled with Cu base paste material with a TSV diameter of 20 μm and depth of 270 μm. The paste showed excellent filling characteristics. The merits of this method are the shorter turnaround time and lower machine cost compared with other techniques, such as plating, metal CVD, etc. Fig. 9 shows new CSP with conductive paste filling TSV. The issues of this process are relatively high resistivity and the contraction of paste material during the cure cycle. In this application, the cross-section of the TSV is much larger than that of the interconnect in an LSI chip, so the parasitic resistance of the TSV does not affect device characteristics.

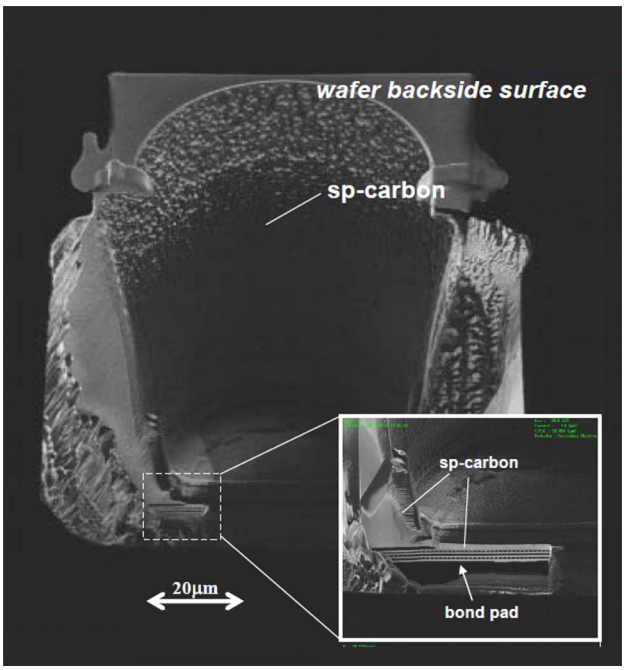

Fig. 5. *FIB prepared SEM image of TSV after SiO_2 Reactive ion etch inner surface of TSV is coated with sp-carbon layer as mask for protection from XeF_2 gas.*

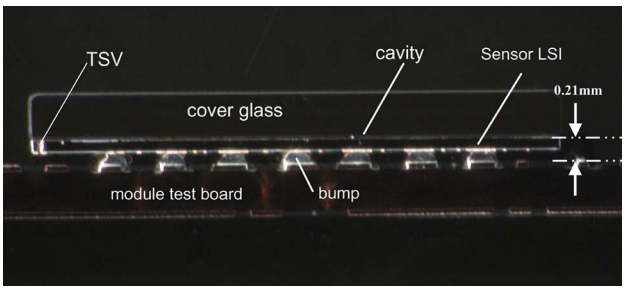

Fig. 6. *Cross-sectional photo image of new chip size package mounting on the module test board.*

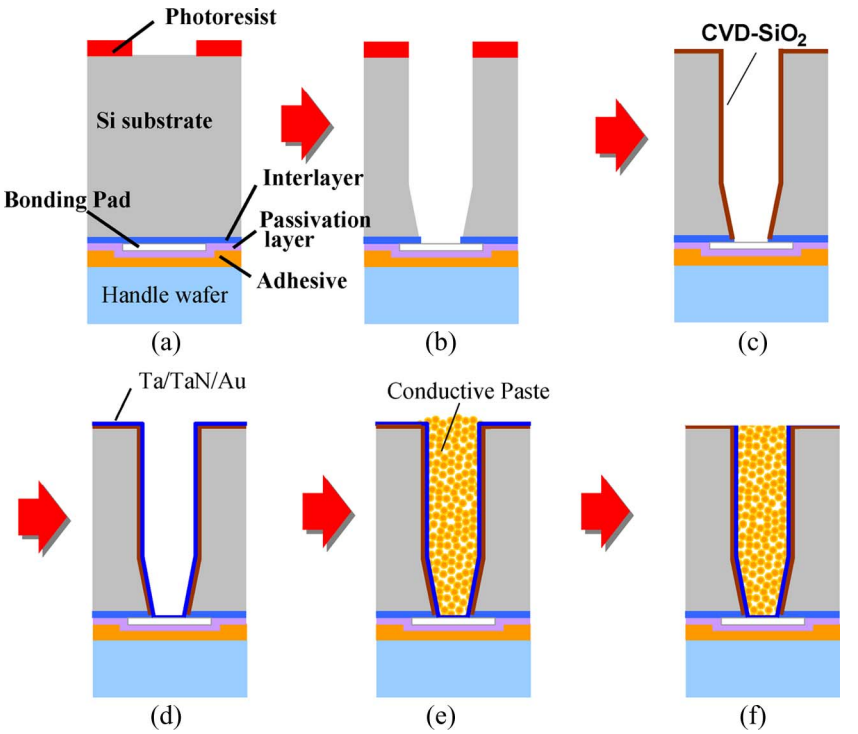

Fig. 7. *Process flow for TSV filling with conductive paste. (a) Back side lithography; (b) deep Si etch and SiO_2 RIE (1); (c) SiO_2 deposition and RIE (2); (d) contact metal/barrier metal deposition; (e) paste printing; and (f) contact and barrier metal removal.*

D. An Example of New CSP for Image Sensor

Fig. 10 shows one example of the new CSP process applied to 1.3 M pixel CMOS image sensor with 49 array bumps. As far as the sensor performance is concerned, we did not observe any degradation compared to a chip-on-board device.

III. FINE PITCH TSV FOR ADVANCED 3D-LSI

As mentioned above, in advanced 3D-LSI, TSVs connect the circuit blocks directly. Therefore, to avoid chip area penalty, the TSV pitch needs to be shrunk to less than 5 μm. So we have been developing fine pitch TSV and

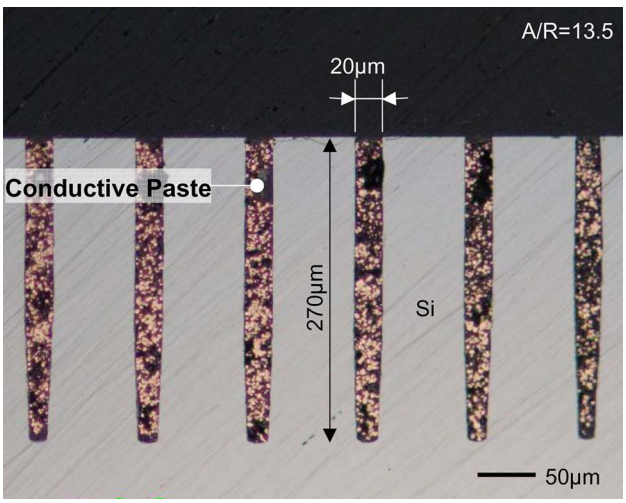

Fig. 8. *Cross-sectional photo image of TSV filling with conductive paste.*

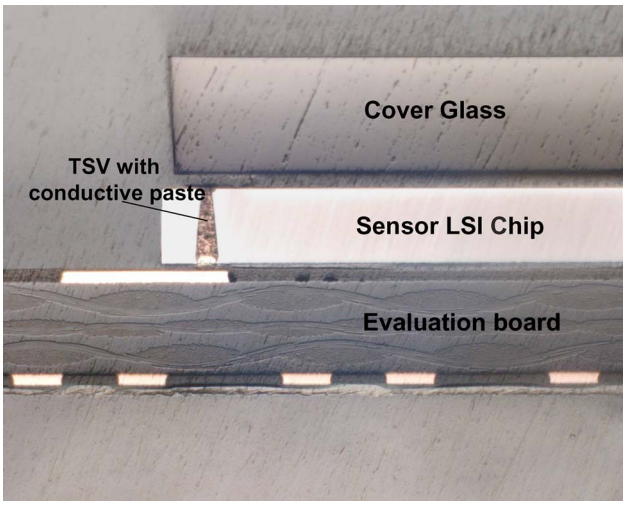

Fig. 9. *Cross-sectional photo image of new CSP with TSV filling with conductive paste.*

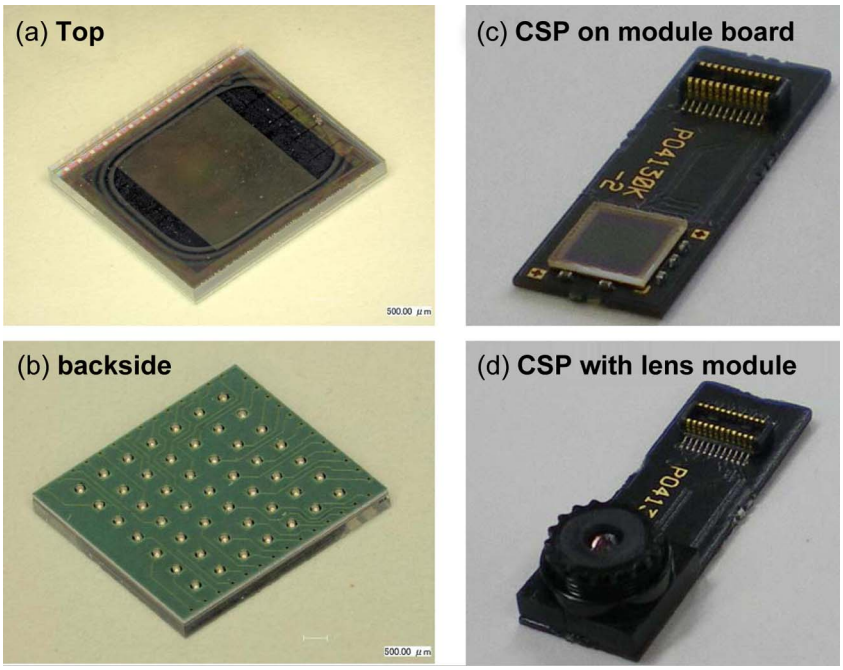

Fig. 10. *New CSP for 1.3 M pixel sensor LSI.*

microbump. In research level, we have completed the technologies of tungsten buried interconnection with diameter of 1 μm and aspect ratio of 50, polysilicon buried interconnection with diameter of 2.5 μm and aspect ratio of 20, and 5 μm pitch 2 by 2 μm^2 bump [9]. The insulator underneath the buried interconnection is silicon oxide. The tungsten buried interconnections process is compatible with wafer process and will be widely used for via-first process (TSVs are forms in front end of line) and via-last process (TSVs are formed in BEOL or after stacking). TSV filled with poly Si is suitable for metal contamination sensitive device like dynamic random access memory. Fig. 11 shows an example of a cross-sectional image of 5 μm pitch In/Au microbump chain. The junction resistance/bump is about 160 $\mu\Omega$. Fig. 12 shows a cross-sectional SEM image of 3 μm pitch TSV. One of the candidate applications is high-performance focal plane array image sensors [20], [21].

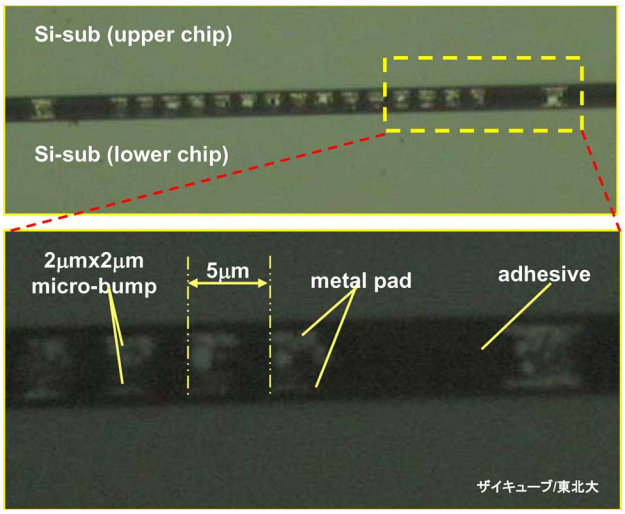

Fig. 11. *Cross-section of 5 μm pitch microbump connection.*

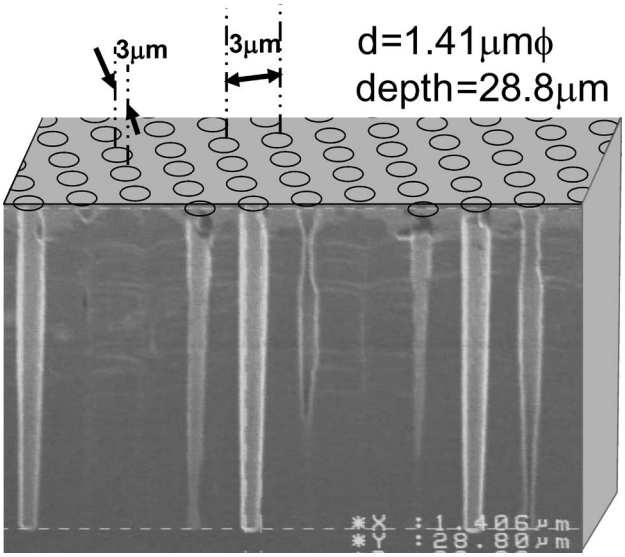

Fig. 12. *SEM cross-section of 3 μm pitch TSV.*

Three-dimensional technologies combined with a backside-illuminated image sensor device allow high-speed signal processing and 100% optical fill factor.

IV. CONCLUSION

The current and future TSV technologies for 3D-LSI are described. An image sensor is a suitable vehicle to develop the 3D-LSI process module with TSV and easy to expand the real 3D-stacked structure. The CSP for a 1.3 M pixel CMOS image sensor is successfully fabricated without performance degradation. Among many potential applications of 3D-LSI technology with fine pitch TSV is high-performance focal plane array image sensors. This technology will allow high-speed signal processing and 100% optical fill factor. ■

REFERENCES

[1] M. Bonkohara, in *Proc. 6th Annu. KGD Ind. Workshop, Session II-3*, 1999.

[2] M. Koyanagi, "Roadblocks in achieving three-dimensional LSI," in *Extended Abst. 8th Symp. Future Electron Devices*, 1989, pp. 50–60.

[3] H. Takata, T. Nakano, S. Yokoyama, S. Horiuchi, H. Itani, H. Tsukamoto, and M. Koyanagi, "A novel fabrication technology for optically interconnected three-dimensional LSI by wafer aligning and bonding technique," in *Extended Abst. 1991 Int. Semiconduct. Device Res. Symp.*, 1991, pp. 327–330.

[4] M. Koyanagi, H. Kurino, T. Matsumoto, K. Sakuma, K. W. Lee, N. Miyakawa, H. Itani, and T. Tsukamoto, "New three dimensional integration technology for future system-on silicon LSIs," in *Proc. IEEE Int. Workshop Chip Package Co-Design*, 1998, pp. 96–103.

[5] M. Koyanagi, H. Kurino, K. W. Lee, K. Sakuma, N. Miyakawa, and H. Itani, "Future system-on-silicon LSI chips," *IEEE Micro*, vol. 18, no. 4, pp. 17–22, 1998.

[6] H. Kurino, K. W. Lee, T. Nakamura, K. Sakuma, H. Hashimoto, K. T. Park, N. Miyakawa, H. Shimazutsu, K. Y. Kim, K. Inamura, and M. Koyanagi, "Intelligent image sensor chip with three dimensional structure," in *IEEE IEDM Tech. Dig.*, 1999, pp. 879–882.

[7] K. W. Lee, T. Nakamura, T. Ono, Y. Yamada, T. Mizukusa, H. Hashimoto, K. T. Park, H. Kurino, and M. Koyanagi, "Three-dimensional shared memory fabricated using wafer stacking technology," in *IEEE IEDM Tech. Dig.*, 2000, pp. 165–168.

[8] T. Ono, T. Mizukusa, T. Nakamura, Y. Yamada, Y. Igarashi, T. Morooka, H. Kurino, and M. Koyanagi, "Three-dimensional processor system fabricating by wafer stacking technology," in *Proc. Int. Symp. Low-Power High-Speed Chips*, 2002, pp. 186–193.

[9] M. Motoyoshi, K. Kamibayashi, M. Bonkohara, and M. Koyanagi, "3D-LSI and its key supporting technologies," in *Tech. Dig. 3D Architect. Semiconduct. Integr. Packag.*, Nov. 2006.

[10] M. Koyanagi, T. Nakamura, Y. Yamada, H. Kikuchi, T. Fukushima, T. Tanaka, and H. Kurino, "Three-dimensional integration technology based on wafer bonding with vertical buried interconnections," *IEEE Trans. Electron Devices*, vol. 53, pp. 2799–2808, Nov. 2006.

[11] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, *IEEE J. Solid-State Circuits*, vol. SC-9, p. 256, 1974.

[12] J. Stern and V. Ozguz, "Beyond 3D integration: 3D systems," in *Tech. Dig. Int. 3D Syst. Integr. Conf.*, 2007, pp. 12.1–12.17.

[13] B. Haba, "Wafer-level stacking: Novel approach to stacking very thin die," in *Proc. Conf. 3-D Architect. Semiconduct. Integr. Packag.*, Oct. 2007.

[14] F. Carson, "Fan-in PoP: Enabling smaller form factor 3D integration," in *Proc. Conf. 3-D Architect. Semiconduct. Integr. Packag.*, Oct. 2007.

[15] M. Robinson, "Bridging the gap to TSV," in *Proc. Conf. 3-D Architect. Semiconduct. Integr. Packag.*, Oct. 2007.

[16] A. Fazzi *et al.*, "A 0.14 mAW/Gbps high-density capacitive interface for 3D system integration," in *Proc. IEEE CICC*, Sep. 2005, pp. 101–104.

[17] K. Kanda *et al.*, "A. 1.27 Gb/s/ch 3 mW/pin Wireless Superconnect (WSC) interface scheme," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2003, pp. 142–143.

[18] M. Bonkohara, M. Motoyoshi, K. Kamibayashi, and M. Koyanagi, "Three dimensional LSI integration technology by 'chip on chip,' 'chip on wafer' and 'wafer on wafer' with system in a package," *Proc. Mater. Res. Soc. Symp.*, vol. 970, pp. 35–45, 2007.

[19] M. Motoyoshi, K. Kamibayashi, M. Bonkohara, and M. Koyanagi, "Current and future 3 dimensional LSI technologies," in *Tech. Dig. Int. 3D Syst. Integr. Conf.*, 2007, pp. 8.1–8.14.

[20] W. Suntharalingam, R. Berger, J. A. Burns, C. Chen, C. Keast, J. M. Knecht, R. D. Lambert, K. L. Newcomb, D. M. O'Mara, D. D. Rathman, D. C. Shaver, A. M. Soares, C. N. Stevenson, B. M. Tyrrell, K. Warner, B. D. Wheeler, W. Yost, and D. J. Young, "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology," in *ISSCC Dig. Tech. Papers*, 2005, pp. 356–357.

[21] C. Keast, B. Aull, J. Burns, C. Chen, J. Knecht, B. Tyrrell, K. Warner, B. Wheeler, V. Suntharalingam, P. Wyatt, and D. Yost, "Three-dimensional integration technology for advanced focal planes," in *Dig. Int. 3D Syst. Integr. Conf.*, 2007, pp. 3.1–3.16.

[22] D. Temple, D. Malta, A. Huffman, M. Lueck, J. E. Robinson, P. R. Coffman, T. B. Welch, M. R. Skokan, A. J. Moll, and W. B. Knowlton, "3-D process technologies for highly integrated microsystems," in *Tech. Dig. Int. 3D Syst. Integr. Conf.*, 2007, pp. 4.1–4.12.

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