SPARC M6 PROCESSOR

SPARC M6 KEY FEATURES

Integrated and scalable enterprise server compute engine

12 SPARC V9 multi-threaded cores with full binary compatibility

96 compute threads

Private 128K Level 2 Cache per core and unified 48MB Level 3 Cache

Integrated coherency control unit and scalability links enable systems with up to 96 CPUs

Dual integrated PCIe 3.0 ports on-chip

Cryptographic Instruction Accelerators integrated in the pipeline

Oracle Solaris OS compatibility guaranteed

KEY BENEFITS

Very high single-thread performance while still scaling to high levels of throughput

Scales to cost-effectively meet needs of growing data center requirements

Integrated crypto provides wire speed security capabilities without performance penalties

Built-in virtualization technology enables dynamic scaling and resource utilization for simpler operations

On-chip networking functionality to drive high capacity network-intensive content and eliminate storage bottlenecks

Oracle's SPARC M6 processor is the industry's most scalable multi-thread, multi-core processor, delivering exceptional single thread performance and very high throughput while enabling systems with up to 96 sockets.

Processor Overview

The SPARC M6 processor design elevates multi-thread, multi-core processor technology to an unprecedented level of scalability. Featuring twelve multi-threaded cores, 96 compute threads, a 3.6GHz clock, dedicated 128K L2 cache per core, and a massive 48MB L3 cache, the SPARC M6 processor is powerful and versatile enough to take on any workload. Combined with advanced, high speed coherency links and additional scalability link units, systems built using the SPARC M6 processor can scale-up to 96 sockets and over a thousand logical domains, which means no application is out of reach.

The SPARC M6 processor leverages an integrated chip design featuring an innovative high-bandwidth memory controller, advanced reliability algorithms, the latest generation PCIe 3.0 interfaces, and cutting-edge power management features all in one package. By integrating system level features directly on to the silicon, applications perform more efficiently while overall system reliability is improved due to reduced part count in the server.

In addition to outstanding multithreaded performance, the SPARC M6 processor offers exceptional single-thread performance as well. In particular, the processor has a robust out-of-order, dual-issue processor core that is heavily threaded among eight strands. The core of the SPARC M6 processor has a 16-stage integer pipeline to achieve high operating frequencies, advanced branch prediction to mitigate the effect of a deep pipeline, and dynamic allocation of processor resources to threads. This allows the SPARC M6 processor to achieve very high single-thread performance while simultaneously scaling to high levels of throughput.

The SPARC M6 processor was designed from the ground up with security as a focus and has Crypto Instruction Accelerators integrated directly into each processor core. These accelerators enable high-speed encryption for over a dozen industry standard ciphers including DES, 3DES, AES, SSL, and RSA. By integrating encryption capabilities directly inside the

instruction pipeline the SPARC M6 processor eliminates the performance and cost barriers typically associated with secure computing.

SPARC M6 Processor Features and Specifications

Processor Features
12 SPARC V9 cores
Die size 643 mm^2
Frequency: 3.6 GHz
28nm process technology
Up to 96 threads per CPU
Up to 32 DDR3 DIMMs per SPARC M6 processor supporting DDR3 1066 MHz memory
Cryptographic stream processing unit in each core accessible through user-level crypto instructions
48 MB, 12-way, Level 3 Cache
7 coherence link channels, 12 lanes each direction per channel, 12 Gbps per lane
6 scalability link channels, 4 lanes each direction per channel, 12 Gbps per lane
Dual PCI Express 3.0 x8 interfaces integrated in silicon
Security: supports AES, Camellia, CRC32c, DES, 3DES, Kasumi, MD5, RSA, ECC, DSA, SHA-1, SHA-224, SHA-256, SHA-384, SHA-512

Processor Core Specifications	
15.4 mm^2 core size	128 KB Level 2 unified cache per core
8 threads	16 KB Level 1 D-cache and 16 KB Level 1 I-cache
Sophisticated branch predictor	2 out-of-order integer execution pipelines, one floating-point unit (FGU), and cryptographic stream-processing integrated in the pipeline
Hardware data prefetcher	

Oracle Hardware Warranty

Visit http://www.oracle.com/us/support/policies/index.html for more information about Oracle's hardware warranty for the SPARC M6 processor.

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