evatronix
We turn engineering into art

Electronic Design Department
Poland, 44-100 Gliwice, Dubois 16
Phone/Fax: +48 32 2311171, +48 32 2313027
e-mail: ipcenter@evatronix.pl
url: www.evatronix.pl

T8051

Tiny 8051-compatible Microcontroller

Overview

The T8051 is a very low gate count, single-chip 8-bit microcontroller which executes ASM51 instruction set. It provides an interface for serial communication, timer, multi-purpose I/O ports, hardware interrupts and debugger interface.

The T8051 design bases on another well-proven Evatronix' product - the R8051XC, however, the T8051 architecture is designed to achieve a very low gate count. To meet this requirement, a wide range of resources is effectively shared between several stages of instruction execution inside the CPU. The gate count is the trump card of the T8051 – there is no 8051-compatible microcontroller on the market that would even come close to the achieved values. Target applications for the T8051 are those in which the microcontroller replaces hard-coded control logic, being easy re-programmable and allowing modifications to the control algorithm without the need to re-design the chip. An implemented complex debugging system is an additional value.

The T8051 is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

Implementation Results

Target		Area			Speed
		Total	incl.CPU	incl.OCDS	
ASIC	TSMC* 0.35µm	0.4730mm^2 / 6.8k gates	2.2k gates	2.5k gates	45MHz
	UMC 0.25 µm	0.2096mm^2 / 8.8k gates	3.2k gates	3.5k gates	85MHz
	UMC 0.18µm	0.1084mm^2 / 8.9k gates	3k gates	3.2k gates	130MHz
	TSMC* 0.18 µm	0.0849mm^2 / 8.5k gates	2.8k gates	3.1k gates	115MHz
	UMC 0.13µm	0.0477mm^2 / 9.2k gates	3.3k gates	3.8k gates	155MHz
	TSMC* 0.13µm	0.0429mm^2 / 8.4k gates	2.8k gates	3.1k gates	133MHz
	TSMC* 0.09µm	0.0236mm^2 / 8.4k gates	2.7k gates	3k gates	233MHz
	UMC 0.065µm	0.0127mm^2 / 8.9k gates	2.9k gates	3.2k gates	450MHz
XILINX	Spartan3e XC3S1200E-5	1344SLICEs + 28 RAMB			33MHz
	Virtex 2 pro XC2VP20-7	1317SLICEs + 47 RAMB			50MHz
	Virtex 4 XC4VLX40-12	1324SLICEs + 46 RAMB			55MHz
	Virtex 5 XC5VLX85-3	796SLICEs + 0 RAMB			62MHz
ALTERA	Cyclone II EP2C5F256C6	2456 LCs			50MHz
	Cyclone III EP3C5F256C6	2459 LCs			80MHz
	Stratix II EP2S15F484C3	1712 ALUT + 0 DSP + 0 M4Ks			100MHz
	Stratix III EP3SE50F484C2	1698 ALUT + 0 DSP + 0 M4Ks			140MHz

Notes:
Optimized for area. The OCDS can be removed from the design.
* Artisan TSMC library

Features

- 100% MCS51® compliant Central Processing Unit
- Input/Output ports
  - Single 8-bit I/O port
  - Alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051
- 16-bit Timers/Counters
  - 80C51-like Timer 0
- Full Duplex Serial Interface
  - Serial 1 (80517-like)
    - 8-bit UART mode, variable baud rate
    - 9-bit UART mode, variable baud rate
    - Baud Rate Generator
- Interrupt Controller
  - Four Priority Levels with 11 interrupt sources (80C517-like)
  - Eight External Interrupts
    - Two Low Level- or Falling Edge-Sensitive
    - Two Falling Edge- or Rising Edge-Sensitive
    - Four Rising Edge-Sensitive
- Internal Data Memory interface
  - addresses up to 256 B of Data Memory Space
- External Memory interface
  - addresses up to 64 kB of External Program Memory
  - addresses up to 64 kB of External Data Memory
  - De-multiplexed Address/Data Bus to ease the connection with memories
  - Program memory write mode
- On-Chip Special Function Registers interface
- Power Management Unit
- On Chip Debug Support (OCDS)

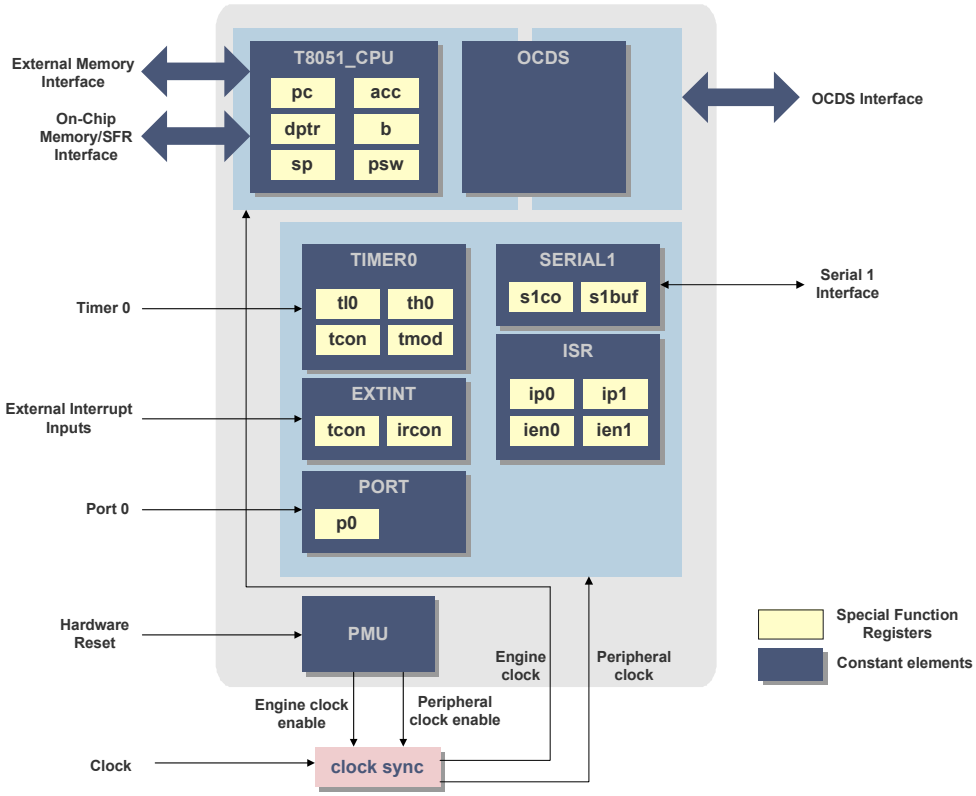
Applications

- Mixed-signal systems
- Low-speed and low-power control systems
- Small FPGA-based systems

Benefits

- The lowest gate count 8051-compliant architecture
- Low power consumption
- Relatively high performance
- Complete debugging solution compatible with other Evatronix 8051 products
- Dummy replacements for even lower gate count
- On-demand customization

Block Diagram



Functional Description

The T8051 core is partitioned into modules as shown in figure above and described below.

T8051 CPU – Central Processing Unit

The CPU fetches instructions from program memory and uses RAM or SFRs as operands. It provides the ALU with 8-bit arithmetic, logic, multiplication and division operations as well as Boolean manipulations. The RAM and SFR interfaces can address up to 256 bytes of Read/Write Data Memory Space and built-in or off-core Special Function Registers. The memory interface can address up to 64kB of both Program Memory and External Data Memory.

Port

The parallel I/O port controller serves the parallel 8-bit I/O port to be used with off-core buffers. It is compatible with the classic 80C51.

Serial1

The core includes a flexible UART (Universal Asynchronous Receiver / Transmitter) port for full-duplex communication. The Serial1 port has two operating modes: 8- and 9-bit UART mode, with variable baud rate generated internally.

Extint

Eight external interrupt inputs are sampled and edge/level checked in this module. Two interrupts are falling edge or low level sensitive, two are rising or falling edge, and the remaining four are rising edge sensitive.

Timer0

The Timer 0 provides four modes of operation: 13-bit timer/counter, 16-bit timer/counter, 8-bit timer/counter with auto reload, and dual 8-bit timer. The Timer 0 can count external pulses (1 to 0 transition) on the corresponding "t0" pin. Another option is to gate the timer/counter using an external control signal, which allows it to measure the pulse width of external signals.

ISR - Interrupt Service Routine

The T8051 provides an 80C515-compatible Interrupt Controller with eleven sources and four priority levels. Each source has its own request flag(s) located in a dedicated SFR. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

PMU - Power Management Unit

The PMU serves two power management modes: IDLE and STOP. The IDLE mode leaves the clock for peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupt or reset. In the STOP Mode, all internal clocks are turned off. The CPU will exit this state with a non-clocked external interrupt (i.e. one of two, level-triggered interrupts) or reset condition. Thus internally generated interrupts (timer, serial port) are not useful.

OCDS

The OCDS unit serves interface for On Chip Debug Support through an IEEE1149.1 (JTAG) port. The OCDS unit provides the following functions - Run, Stop, Single-step, hardware and software breakpoints, debugger program execution and Read/Write Access to Program Memory, External/Internal Data Memory and SFRs.

Pin Description

Name	Type	Polarity/ Bus size	Description
General signals			
clkcpu	I	Rise	Engine clock
clkcpuen	O	High	Engine clock enable output
clkper	I	Rise	Peripheral clock
clkperen	O	High	Peripheral clock enable output
reset	I	High	Hardware reset input
ro	O	High	Reset output
Port 0			
port0i port0o	I O	8 8	8-bit bi-directional I/O port with separated inputs and outputs
External interrupt inputs			
int0	I	Low/Fall	External interrupt 0
int1	I	Low/Fall	External interrupt 1
int2	I	Fall/Rise	External interrupt 2
int3	I	Fall/Rise	External interrupt 3
int4	I	Rise	External interrupt 4
int5	I	Rise	External interrupt 5
int6	I	Rise	External interrupt 6
int7	I	Rise	External interrupt 7
Serial Port 1 interface			
rxd1	I	-	Serial 1 receive data
txd1	O	-	Serial 1 transmit data
Timer 0 interface			
t0	I	Fall	Timer 0 external input
On-Chip Debug Support interface			
trst	I	Low	Debug logic reset input
tck	I	Rise/Fall	Debug clock
tms	I	-	Test Mode Select
tdi	I	-	Debug Data Input
tdo	O	-	Debug Data Output
Program / External Data Memory interface			
memdatai	I	8	Memory data input
memdatao	O	8	Memory data output
memaddr	O	16	Memory address
mempswr	O	High	Program store write enable
mempsrd	O	High	Program store read enable
memwr	O	High	Data Memory write enable
memrd	O	High	Data Memory read enable
On-Chip Data Memory (IRAM) interface			
ramdatai	I	8	Data bus input
ramdatao	O	8	Data bus output
ramaddr	O	8	Data file address
ramwe	O	High	Data file write enable
ramoe	O	High	Data file output enable
Custom (off-core) Special Function Registers interface			
sfrdatai	I	8	SFR data bus input
sfrdatao	O	8	SFR data bus output
sfraddr	O	7	SFR address
sfrwe	O	High	SFR write enable
sfroe	O	High	SFR output enable

Performance

The key value of the T8051 is its compact size. The core occupies about 8.5k gates in a typical 0.18 um process. By removing the On-Chip Debug Support circuitry, it shrinks by another 3.2k gates, fitting in 0.0539 mm^2 footprint.

Moreover, the T8051 has more computing power than the original 80C51 architecture. The performance improvement is at rate of **4.1** (in terms of Dhrystone MIPS) with respect to the 80C51 device working at the same clock frequency. However, the real speed improvement seen in any system will depend on the instruction mix.

Dhrystone benchmark comparison	
12-clock (C8051)	1
4-clock (D80530)	2.1
T8051	**4.1**
1 clock (R8051XC)	6.9..9.6

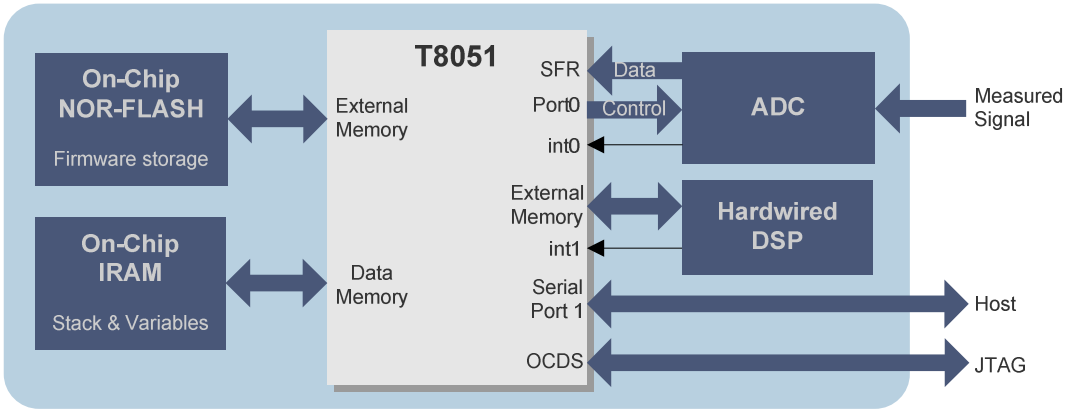
Verification Methods

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The test suite for the peripherals has also been developed in their own testbenches, based on either hardware or behavioral models.

The trial ATPG coverage figures met the requirements and reached level of 99%. Additionally the value of IDDQ reached level of 99%.

Example Application

The figure below illustrates an example application of the T8051 microcontroller core as an industrial meter (e.g. energy or rotation meter). The Analog/Digital Converter (ADC), controlled by the T8051 through the Special Function Registers (SFR) interface, provides measured data which are processed initially by the CPU, then by the custom-designed DSP block providing high-precision arithmetic. The processed data are stored back in the on-chip RAM, and can be read by the external host using UART (Serial Port 1) interface. For firmware (algorithm) development, debugging and modifications, the JTAG-accessible OCDS is provided. It can also be used for production programming of the on-chip NOR-FLASH memory.



Options

Typically the core is delivered as an HDL source code for ASIC implementations. The following options may be ordered according to user's requirements.

- EDIF netlist for FPGA and low volume production
- Complete debug solution including software plug-in for Keil environment and USB Pod
- Annual maintainance
- On-site support and training

Additional parts of the system or modifications to the core may be developed by Evatronix, according to the user's application.

Third Party Reference

The T8051 On-Chip Debug Support is compatible with that of Evatronix R8051XC, which is well supported by Keil uVision3 compiler/debugger. The tool can be used for code compilation and on-line hardware debugging.

Product Versions

R8051XC – the fastest, most configurable single-chip 8-bit microcontroller core that can implement a variety of fast processor variations executing the MCS® 51 instruction set.

Standard Deliverables

- HDL source code for the T8051
- Synthesis support (Synopsys) with a complete set of synthesis scripts
- Simulation support (MTI, Cadence) with a set of scripts and macros for compilation & simulation
- Extensive Verilog 2001 Test Bench that instantiates:
  - The T8051 Microcontroller
  - The T8051 CPU behavioral model
  - Clock and reset generator
  - On-Chip & External RAM models
  - Program Memory model including random code generation mode
  - Memory access comparators
  - Verification components that drive and compare pins dedicated to several peripherals of the T8051
  - Collection of 8051 assembler programs which are executed directly by the Test Bench
  - Set of expected results
- Documentation
  - Design Specification
  - Verification Specification
  - Test Plan
  - Integration Manual
  - Application Notes
- Reference design for proprietary development board This design uses the T8051 and illustrates how to build and connect memories and port modules

Headquarters
Przybyly 2, 43-300 Bielsko Biala, Poland, Phone: +48 33 499 59 15, Fax: +48 33 499 59 18
ipcenter@evatronix.pl
www.evatronix.pl