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Cover Story

Introducing Intel® XScale™ Microarchitecture

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Overview

Intel® XScale™ microarchitecture, introduced at the August Intel® Developer Forum Conference, combines performance, speed, and cutting-edge engineering in a compact, high-performance/ultra-low-power design. From battery-powered, wireless and handheld applications like digital phones, personal digital assistants, and communicators to Internet infrastructure applications like routers and bridges, the Intel XScale microarchitecture is breaking new ground for products that will expand the future of the Internet.

Low Power, High Performance

This new microprocessor core enables a new generation of integrated microprocessors, designed to optimize both ultra-low power consumption and high-performance processing from the same processor core. Designed as a revolutionary follow-on to the Intel® StrongARM* microarchitecture, this new microarchitecture extends Intel's commitment to ultralow-power/high-performance ARM* compliant Reduced Instruction Set Computing (RISC) processors with enhancements for wireless, handheld devices. See Figure 1.

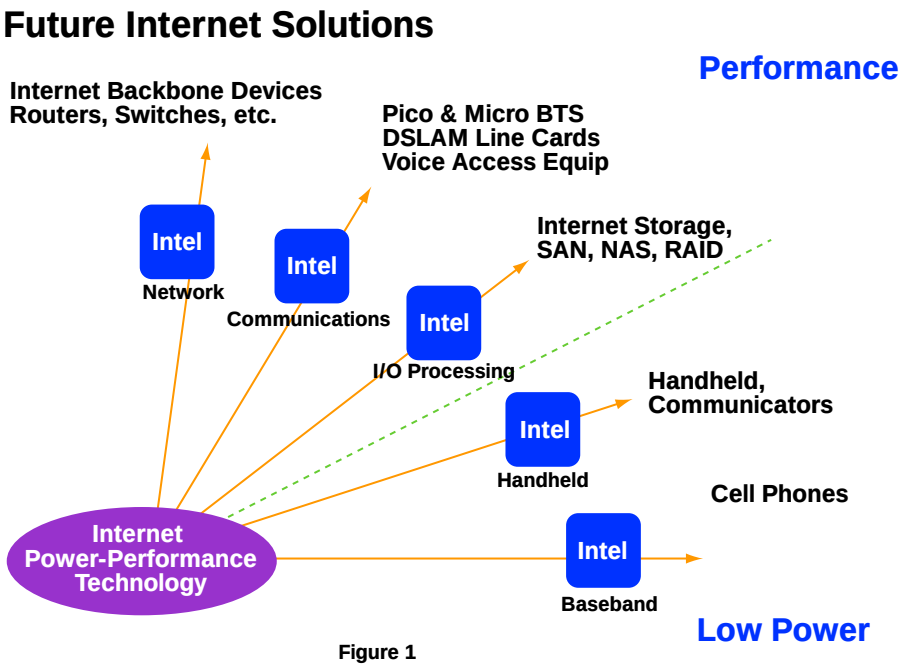

Figure 1

Intel® XScale™ Microarchitecture Solutions

The Intel XScale microarchitecture will be combined with peripherals to provide Applications Specific Standard Products (ASSP) targeted at selected market segments. For example, the microprocessor core can be integrated with peripherals such as an LCD controller, multimedia controllers and an external memory interface. This helps OEMs develop smaller, more cost-effective handheld devices with long battery life and the ability to deliver rich multimedia applications. Or the microprocessor core could be surrounded by high-bandwidth PCI interfaces, memory controllers, and networking micro-engines to provide a highly integrated, low power, I/O or network processor.

Architecture Overview

As the successor to Intel's StrongARM microarchitecture, a general-purpose embedded RISC microarchitecture, the new microarchitecture is an Internet focused RISC solution compliant with the ARM instruction set. Future products based on the processor core will be manufactured in Intel's state-of-the-art 0.18-micron production semiconductor process technology. Together with design enhancements added to the new core, this technology allows the Intel XScale microarchitecture to operate over a wide range of speed and power, producing industry-leading MIPS/Watt performance.

With this new microprocessor core, Intel has improved low power and multimedia capabilities and established the benchmark in this performance class through these important technologies. See Figure 2.

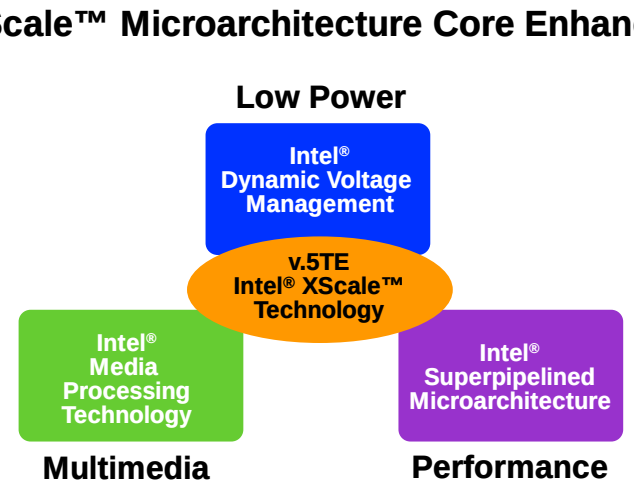

Figure 2

Intel® Dynamic Voltage Management provides system-level power management through dynamic voltage and frequency scaling and new, lower power modes. The result being that applications can on the fly utilize the performance they need when they need it, then quickly reduce the power and frequency to save battery life. Additionally Intel's designers achieved low power through customized circuits making extensive use of clock gating, leakage suppression circuitry, and a variety of special circuit techniques support low voltage operation, and balanced pipeline partitioning adds greater efficiency.

Intel® Media Processing Technology is the first in a series of planned media enhancements. Utilizing ARM coprocessor space, the new enhancements include 16-bit SIMD multiplies with 40-bit accumulation for efficient media processing.

Intel® Superpipelined Technology enables performance approaching 1 GHz and better throughput and interrupt handling capabilities. This improved pipeline technology includes 7-stage integer/8-stage memory superpipelined for fast clock rates, dynamic branch prediction, extensive data bypassing, and high-speed custom circuits.

These solutions for the wireless world deliver market leading O/S support for the convergence of voice, video, data, and Internet connectivity in handheld devices.

Key Features

This new high-performance, ultra-low-power microarchitecture is compliant with the ARM Version 5TE Instruction Set Architecture (ISA). The microarchitecture implements the ARM's instruction set with Intel's own instruction and data memory management units; instruction, data, and Mini-Data caches; write, fill, pend, and branch target buffers; power management, performance monitoring, debug, and JTAG units; coprocessor interface; MAC coprocessor; and core memory bus. In addition, the Intel XScale microarchitecture delivers key advantages for Internet focused devices in these important areas.

- *Intel Superpipelined Technology*—7-stage integer/8-stage memory superpipelined core achieves high speed and ultra-low power
- *Intel Dynamic Voltage Management*—Dynamic voltage and frequency scaling on-the-fly allows applications to utilize the right blend of performance and power
- *Intel Media Processing Technology*—Multiply-Accumulate Coprocessor performs two simultaneous 16-bit SIMD multiplies with 40-bit accumulation for efficient media processing
- *Power Management Unit*—Gives power savings via idle, sleep, and quick wake-up modes
- *128-entry Branch Target Buffer*—Keeps pipeline filled with statistically correct branch choices
- *32-KB Instruction Cache*—Keeps local copy of important instructions to enable high performance and low power
- *32-KB Data Cache*—Keeps local copy of important data to enable high performance and low power
- *2-KB Mini-Data Cache*—Avoids “thrashing” of the D-Cache for frequently changing data streams
- *32-entry Instruction Memory Management Unit*—Enables logical-to-physical address translation, access permissions, I-Cache attributes
- *32-entry Data Memory Management Unit*—Enables logical-to-physical address translation, access permissions, D-Cache attributes
- *4-entry Fill and Pend Buffers*—Promotes Core efficiency by allowing nonblocking and "hit-under-miss" operation with Data Caches
- *Performance Monitoring Unit*—Furnishes two 32-bit event counters and one 32-bit cycle counter for analysis of hit rates, etc.
- *Debug Unit*—Uses Hardware Breakpoints and 256-entry Trace History Buffer (for flow change messages) to debug programs
- *32-bit Coprocessor Interface*—Provides high-performance interface between core and coprocessors
- *64-bit Core Memory Bus with ECC*—Gives up to 4.8-Gbytes/second bandwidth for internal accesses
- *8-entry Write Buffer*—Allows the Core to continue execution while data is written to memory

Summary

The Intel XScale microarchitecture provides the flexibility needed between low power and high performance for wireless and handheld Internet devices as well as Internet infrastructure products, allowing complex data to be processed over both the wired and wireless Internet. The Intel XScale microarchitecture will break new ground in the devices that expand the future of the Internet.

More Info

Find out more about the Intel XScale microarchitecture at the Intel Developer Web site.

Author Bios

David B. Rogers joined Intel in May 2000 and is a senior marketing engineer in the Handheld Computing Division. Formerly a director of business development at Motorola, David was responsible for the 1997 launch of the Motorola M-CORE* Architecture. Additionally, David was responsible for creating IP licensing, product development and tools strategies for the electronics distribution channel. David is a graduate of Austin College, with a B.A. in Political Science.

Joe W. English is a senior marketing program manager with the Server Storage Business Unit of Intel's I/O Processor Division. Joe joined Intel last year, bringing with him marketing management experience at Gateway 2000 Corp., Advanced Logic Research, Inc., AST Research, Inc., and IBM Corporation.

Joe holds a B.A. in Communications from the University of Washington, an M.A. in Communications Management from the University of Southern California, and a J.D. from Western State University.

Columns

From the Editor

Donna Loveland
Managing Editor
Technology and Initiative Marketing
Intel Corporation

Column

Last week, the Intel® Developer Forum Conference, Fall 2000, popularly known as Fall IDF, lived up to its promise to be the biggest and best ever. With more than 150 technical sessions and a white-hot focus on the Internet, IDF proved once again why it's considered the premier event for the worldwide developer community.

As a result, this month's issue of Intel Developer Update is double the usual size. It brings you the details on some of Fall IDF's key announcements, with more still to come in the months ahead.

Introducing Intel® Xscale™ Microarchitecture—cover story—Announced at Fall IDF, Xscale microrchitecture enables a new generation of integrated microprocessors optimally balanced between ultra-low-power consumption and high-performance processing. It's based on Intel's StrongARM* architecture, and it's breaking new ground for products that will expand the future of the Internet.

Intel® Internet Exchange™ Architecture Moves to Applications—With its wide range of programmable silicon and software building blocks, IXA enables a fast and cost-effective way to add intelligence to network infrastructure, access devices, and appliances. Its straightforward design solutions are ready for OEMs and developers to implement now.

Get on the Fabric with InfiniBand Architecture*—Industry leaders believe that InfiniBand* Architecture, with its support for greater system scalability, reliability, and performance, has the potential to transform data center I/O—and the way data centers are developed.

Solving BIOS Boot Issues with EFI—EFI provides a standardized interface between an OS and a hardware platform, eliminating the need for the OS to be hardware-specific, and it allows for new innovations in hardware platforms.

CDSA Now Includes HRS Biometric Authentication, Authorization—Two recently introduced technologies—Human Recognition Services and Simple Public Key Infrastructure—offer new security services to application developers and extend the functionality of Common Data Security Architecture.

Intel Press Publishes IA-64 Book — Intel Press introduces *IA-64 Architecture for Software Developers* by Walt Triebel, an in-depth look at IA-64 architecture written for novices and experts alike. Read the first chapter of the book, "Introduction," now online at the Intel Press Web site.

Innovative PC Recognition Program: Designing Outside the Box—This Intel program showcases designs that merge innovation and simplicity, and encourages developers to create a more compelling PC platform. Three OEMs that advanced the state of the art in innovation, simplicity, and style received the program's latest awards at last week's IDF Conference.

New Test Suites and Matrix for IAPC—With the EPA's new Energy Star requirements in effect, developers should be testing in-house now for S3 compatibility for PCs. Intel now offers a free PCI-D3 test suite and an Instantly-Available PC text matrix to developers to help ensure S3/D3 compatibility.

Intel® 815 Chipset for microATX and a Super New ATX Board—The new Intel® Desktop Board D815BN delivers mainstream features in the microATX form factor, resulting in extreme versatility and cost effectiveness. The new Intel® Desktop Board D820LP is Intel's highest performance desktop board, with more power for the Internet and networks.

Intel's Value Communications Appliance Reference Design—With Intel's new Value Communications Appliance Reference Design, OEMs in the communications appliance market segment can reduce their time-to-market with a complete design that can easily be modified without reworking the core microprocessor or chipset design.

Intel® Internet Phone SDK Enhances Net Phone Quality—Soon to be distributed by Dialogic Corporation, an Intel company, the SDK provides an interoperable solution for developers, offers IP telephony service providers an opportunity for services innovation and market differentiation, and delivers a higher quality experience to end users.

ROMB: The Rest of the Story—For a growing number of users looking for improved network storage performance, data protection, data availability, network reliability, and ease-of-use, ROMB—RAID (redundant array of independent disks) on motherboard—is the next "must-have" feature in servers.

Software to Deliver Ease of Use to Internet Users—Developers should include a Design for Usability in their current software projects. When usability is factored into every phase of the design process, problems are solved early, resulting in faster, lower cost development. The article shares tips and techniques for usability design.

System Test-IF Introduces PC 2001 Tests—The fourth System Test-Implementers Forum took place in San Diego in July. Co-sponsored by Intel and Microsoft, the event comprised the PC 2001 Test Specification Review and the first Test Fest based on PC 2001-related tests.

Deadwood, Old Masters—In the light of all the announcements and advancements showcased at last week's IDF Conference, *Inside Looking In* columnist David Barkai considers whether more can be done to benefit from the past experiences of an older generation of engineers.

If you'd like to do more with your design and development efforts, visit the articles in this month's double IDF Conference issue of Intel Developer Update.

Enjoy.

Author Bio

Donna Loveland is the editor of *Intel Developer Update* magazine. She joined Intel's Platform Marketing group in 1999 as the editor of Platform Solutions News. Donna began her career with Intel in 1982 as a technical editor in an advanced microprocessor development group. Since then, she's held technical and marketing positions in leading-edge technology areas ranging from stereoscopic display to digital broadcast to scalable online content. Donna has a B.A. degree in English from the University of Rochester and an M.A. in Expository Writing from the University of Iowa.

Inside Looking In

Deadwood, Old Masters

David Barkai
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Intel Architecture Group
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Column

In the field of theoretical physics the majority of new ideas come from researchers under the age of 30. This may sound extreme, but practitioners in this esoteric field generally accept it as a truism. In general, however, we all recognize that our creativity peaks much sooner than our retirement age. By creativity I mean both coming up with new ideas and implementing them. The young adult is likely to be more intellectually prolific and a more efficient producer than his older alter ego would be. Just think about who is driving the new Internet economy.

The reasons for this phenomenon are varied and complex, and I won't delve into them here. Instead, let's consider those of us who are on the far side of their creativity peak. There is no set age for that point when most of our original and creative work is behind us. The creative phase typically stretches over more than 20 years, leaving most of us at our mid-forties or beyond at its conclusion. Where might a mature person be at this stage of his or her career? Some are managers at various levels of their organizations. If they're doing their job right, they spend much of their time mentoring staff, imparting past learnings and accumulated knowledge. Some continue to be productive as individual contributors.

But many from this population do not belong to either of these two groups—the managers or the still-creative contributors. They're not formal managers, supervisors, or mentors either because they're not so inclined or because there's room for only so many managers. They've lost some of the innovation, energy, and excitement that characterize the "kids" out of college. They're governed by a more even-keel, steady rhythm of life. And they, typically, end up on the fringes of the projects they are a part of. Are we missing opportunities or wasting our own efforts by letting these experienced engineers drift out of the mainstream of professional activities?

Yes—definitely. Most of us subscribe to the cliché that with age comes wisdom, and with good reason. We recognize that years on the job result in a seasoned approach to problem solving and a familiarity with tricks of the trade and the circumstances where they apply. Everyone knows some older engineer in the group, just there in the background, who, out of the blue, will come out with gems of suggestions that save a lot of trial and error on the way to the desired outcome. In these cases, experience beats youth and creativity.

It's hard to quantify the benefits of applying past knowledge, though some notable activities provide striking examples of missed opportunities.

A few years ago Intel added new instructions to the x86 instruction set. The enhancements came in several phases, starting with the later days of the Intel® Pentium® processor and continuing through the most recent Pentium® 4 processor. For the purpose of this discussion, suffice it to say that these new instructions enabled the processors to produce multiple, simultaneous results with a single instruction. For example, the program can issue a special addition instruction that will operate on four pairs of numbers and return four results, and do it at the rate of a single normal addition. The programming techniques and compiler optimizations that take advantage of the capabilities of these new instructions are the same techniques used by programmers of vector supercomputers, and they were invented 15 to 25 years before their introduction into the Intel® Architecture. Yet, they were reinvented at Intel by a younger generation of engineers.

This isn't an isolated occurrence. Here at Intel, we're in the midst of developing the Intel® Itanium™ processor, Intel's first product to use 64-bit architecture. Porting software and applications to the 64-bit environment, and developing new software that will run on both 32-bit and 64-bit platforms is a relatively new activity for us and some of our fellow travelers. In our midst we have some engineers who worked for companies that went through various forms of this transition starting some 30 years ago and continuing on for 15 years or more. Many more engineers from that older generation and with that experience are out there. They are, to a large extent, an untapped body of knowledge that can help accelerate what is, by all accounts, a critical process for Intel and the rest of the industry.

The problem of finding the right role for the older, experienced engineers is not unique to Intel. The high-tech industry is evolving and changing at such a dazzling speed that the span of the generational gap referred to here has shrunk considerably. Methods and techniques are being invented and left behind at ever-increasing frequencies. The opportunities for recycling past solutions are more abundant, and the older engineers are the key to realizing them. In this business environment an interesting social phenomenon is beginning to emerge: young Internet entrepreneurs, CEOs, and founders of new companies are hiring their parents as a way to balance ideas, risks, process, and discipline. In bigger companies like Intel, the parents' generation is already among us. Deadwood or old masters? It is up to us.

Author Bio

David Barkai joined Intel in 1996. Before assuming responsibility for IDF Conference content, he worked in the company's Microcomputer Software Lab, where he focused on applications for Intel Architecture workstations. Prior to that, David specialized in scientific and engineering supercomputing applications and conducted pioneering work on vector processors. He holds a Ph.D. in theoretical physics and has published over 20 papers in the areas of physics, numerical methods, and computer technical applications and architectures.

Departments

Applied Computing

Intel's Value Communications Appliance Reference Design

Chris Hubbard
Technical Marketing Engineer
Embedded IA Division
Intel Corporation

Overview

With Intel's new Value Communications Appliance Reference Design, OEMs in the communications appliance market segment can reduce their time-to-market with a complete design that can easily be modified to fit their needs without reworking the core microprocessor and chipset design. The value reference design builds on Intel's highly successful Entry-Level Communications Appliance Reference Design by adding higher performance, twice the hard disk interface bandwidth, additional security features, and smart integration, which reduces board real estate requirements and system cost.

Targeted for small business to mid-size user environments, applications for the reference design include network attached storage, Virtual Private Network (VPN), Web caching, network security, load balancing, Voice-over-IP (VoIP) and multi-service access devices (MSAD).

Big Benefits for Developers

The Value Communications Appliance Reference Design is a scalable solution that enables developers to design a single board that can be populated with an Intel® Pentium® III or Celeron™ processor in a 370-pin PGA package. Developers can base a variety of communications appliances on the reference design's common platform. This saves development time and results in a faster time-to-market, allowing developers to focus on other parts of their business.

The platform includes two Intel® 82559ER 10/100 Fast Ethernet controllers. Two Ethernet controllers permit the platform to be used for security products, such as firewalls and VPNs, where one port is connected to the secure network while the second port is connected to the insecure network. A gateway appliance, likewise, can use the two Ethernet ports—one port connected to the internal network and the second port connected to a Wide Area Network (WAN) connection such as DSL modem or cable modem.

The design also includes two RS-232 serial ports—which are important features for implementing communications appliances. These serial ports can be used for communication with other devices such as uninterruptible power supplies, or for console redirection. Since most appliances are headless (they do not have keyboard, mouse, or monitor) there needs to be a method of interacting with the underlying operating system and application software. Many embedded operating systems and BIOS allow for keyboard and monitor information to be routed over the serial port. A PC can then be used to remotely control and configure the appliance by using the PC's monitor and keyboard. Console redirection can be used in the field by technicians as well as in the laboratory by developers.

The Value Communications Appliance Reference Design enables small form factor designs, which are required in the marketplace. This design has been implemented in form factors as small as 5.1" by 8.5" while still supplying connectors for dual Ethernet, two USB ports, dual IDE channels (up to four devices), dual RS-232 serial ports, parallel port, and a floppy drive. The platform uses a laptop-standard SoDIMM memory socket, which keeps the form factor small while still using industry-standard components and allowing for design flexibility.

To help developers add functionality, the design incorporates a PCI Mezzanine Card (PMC) connector. PMC is an industry standard that is rapidly gaining acceptance in embedded markets due to its low-profile design. The PMC connector is electrically equivalent to the standard PCI connector, yet it orients the daughterboard parallel to the baseboard instead of perpendicular to the baseboard. The PMC connector allows developers to easily add functionality while maintaining the flexibility of the PCI bus in a low-profile form factor.

In addition, the design also meets a variety of customer requirements by supporting application-specific software and peripherals while maintaining compatibility with operating systems, BIOS, and peripheral interfaces. Figure 1 shows the Value Communications Appliance Reference Design in a communications application.

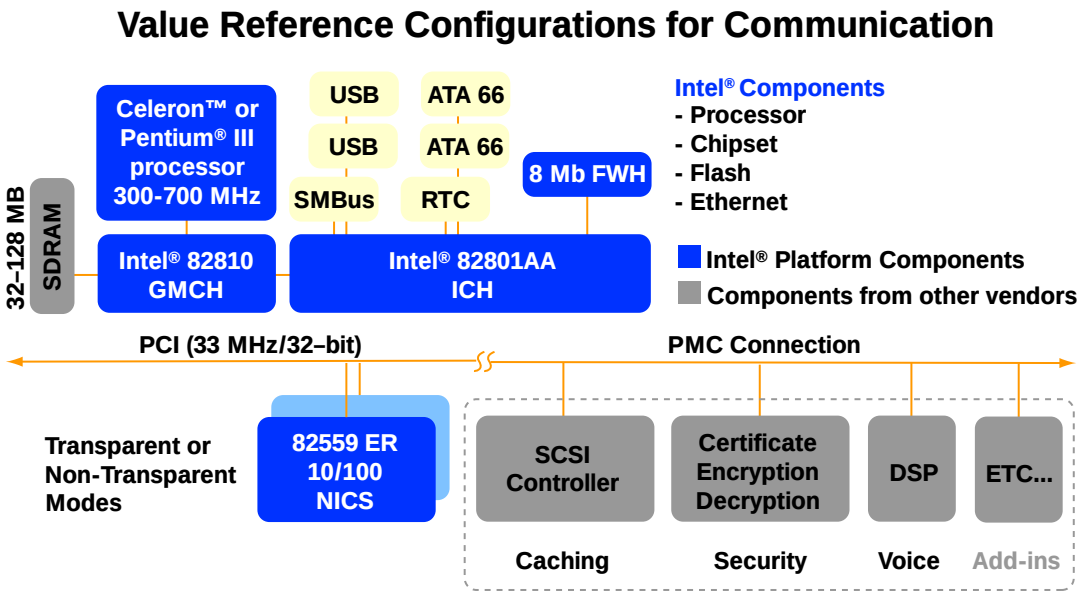

Figure 1

Building on quality

Intel's value reference design is based on the Intel® 810 Chipset. The Intel 810 chipset contains three core components: the Graphics Memory Controller Hub, the I/O controller hub, and the Accelerated Firmware Hub (FWH). In the host controller, the Intel® 82810 Graphics and Memory Controller Hub integrates a 66/100-MHz system bus, 100-MHz SDRAM controller, and a high-speed Accelerated Hub Architecture for communication with the I/O Controller Hub. It has been validated for use with both the Pentium III and Celeron processor families. An integrated centralized memory arbiter allocates memory bandwidth to multiple system agents to optimize system memory utilization. The Accelerated Hub Architecture, a new chipset components interconnect, is designed into the Intel 810 chipset to provide an efficient communication channel between the Graphics Memory Controller Hub and the I/O controller hub.

The key benefits of using the 810 chipset include:

- Double the IDE throughout from ATA/33 to ATA/66
- Smart integration reduces overall system cost and real estate
- The Firmware Hub with Random Number Generator (RNG), which enables stronger encryption, digital signing and security protocols
- Scalable processor support to address different price/performance needs

The Pentium III processor (FC-PGA) features an integrated on-die, 256 Kbyte, 8-way set associative level-two (L2) cache, and is available at 600 MHz and 700 MHz with a 100-MHz processor side bus. This processor includes a 16-Kbyte level-one (L1) instruction cache and 16-Kbyte L1 data cache. These cache arrays run at the full speed of the processor core. The Celeron processor features an integrated 128-Kbyte L2 cache with a separate 16-Kbyte instruction and 16-Kbyte data L1 cache and is available at speeds of 300, 366, 433, and 566 MHz with a 66-MHz processor side bus.

Key Reference Design Features

Intel's new Value Communications Appliance Reference Design offers these key features:

- Fully-proven schematics in Orcad* 9.0 and Adobe Acrobat* formats.
- Scalable performance using Intel® Celeron (300 to 566 MHz) to Pentium III (600 MHz to 700 MHz) in a PGA 370-Pin socket.
- 32-MB to 128-MB SoDIMM SDRAM
- Versatile networking and I/O capabilities:
  —Two Ethernet ports (10/100 Mbps)
  —Two IDE channels (ATA-66)
  —Dual USB ports (Revision 1.1)
  —Two serial ports (RS232)
  —Parallel port (ECP)
  —FDD port
  —One PCI Mezzanine Card (PMC) connector for ease of connectivity to the PCI bus (32 Bit/33 MHz)
- VGA output via pin header and small adapter
- Small form factor design
- Ease of use and stand-alone functionality
- Uses external power supply "brick"

Third-Party Vendor Support

Intel works with multiple independent hardware and software vendors to quickly enable the implementation of designs based on Value Communications Appliance Reference Design. These vendors have the software and hardware in place to aid the designer:

Independent Hardware Vendors

- Force Computers
- ITOX
- Teknor
- Trenton Technology, Inc.
- WIN Enterprises

Independent Software Vendors

The following companies have application software that has been ported to the platform.

- Technauts
- CrosStor
- eSoft
- LynuxWorks
- Microsoft

This list is provided for your convenience. Intel does not endorse other companies supplying products or services.

Summary

With increasing demands for new technology, developers are tasked with delivering applications and services to market quickly. In combination with embedded Intel® Architecture's flexibility and scalability, the Value Communications Appliance Reference Design helps developers meet these needs. The flexibility, scalability, and reliability of this reference design lets developers reduce time-to-market by delivering a complete design that is easily modified without reworking the core microprocessor and chipset design.

More Info

To receive a copy of Intel's Value Communications Appliance Reference Design visit the Platform Solutions area of Intel's Developer Web site

Visit Intel's Developer Site for information on:

- Intel 810 Chipset
- Pentium III processor
- Celeron processor

Author Bio

Chris Hubbard is a senior technical marketing engineer for Communication Appliances in Intel's Embedded IA Division. He joined Intel in 1995 and has worked on microcontrollers, digital cameras, and DSPs. Chris is currently responsible for the definition and development of communication appliance platforms based on Intel Architecture. Chris holds a B.S. in electrical engineering from Brigham Young University.

Intel® Internet Exchange™ Architecture Moves to Applications

Kerry Bott
Director of Product Marketing
Intel® Internet Exchange™ Architecture Platform Operation
Intel Corporation

Overview

The growth of the Internet and proliferation of e-Commerce are driving the evolution of networking technology at an unprecedented rate. New applications are fueling the demand for more bandwidth and richer data types as voice, data, and video begin to share the same network. The rapid development of the Internet infrastructure is creating tremendous opportunities for network equipment OEMs and independent vendors of software and hardware products.

Networking equipment vendors have traditionally relied on fixed-function application-specific integrated circuit (ASIC) designs to deliver high-speed, high-service packet processing solutions such as network switching. As system requirements continue to grow in complexity, driven by the need to support multiple protocols and service levels, ASIC-based designs are becoming too costly and inflexible to satisfy time-to-market requirements.

Intel® Internet Exchange™ architecture (IXA) provides a set of programmable and interoperable hardware and software building blocks that overcome the inherent limitations of ASIC-based design methods. IXA enables network OEMs and developers to flexibly and rapidly deliver differentiated services across multiple network protocols on all levels of the OSI (Open System Interconnection) model.

Intel® IXA is more than a multi-layer stack of building blocks. It is a growing architecture that integrates product development platforms that provide real solutions, including DSL access multiplexers, multi-service switches, enterprise switches, CPE (customer premises equipment) devices, and 10-Gigabit optical devices.

Intel Internet® Exchange™ Architecture Building Blocks

Intel IXA provides a wide range of programmable silicon and software building blocks that enable a relatively fast and cost-effective way to add intelligence to network infrastructure, access devices, and appliances. The programmability of many of the IXA building blocks also creates new opportunities for software developers to provide applications and tools.

One element of Intel Internet Exchange architecture is a new networking framework based on the programmable Intel® IXP1200 network processor and corresponding APIs that help simplify and expedite the product development cycle.

Building blocks in the Intel Internet Exchange architecture family include:

- Embedded Intel® Architecture processors and chipsets—providing a host computing platform for applications, control, and services
- IXE Application Engines—building blocks used to provide high-performance switching functionality for ATM, Gigabit, and 10/100-Mbit/second Ethernet
- IXF Formatting Devices—a wide range of devices used to format ATM cells, T1/E1 frames, Sonet/SDH frames, and Gigabit and 10/100-Mbps Ethernet packets
- LXT Physical Interfaces—interfaces for T1/E1 lines, HDSL, HDSL2, Sonet/SDH PHYs, and 10/100-Mbps Ethernet
- Service-specific network processors for network access and customer premises equipment (CPE) applications
- Intel IXA software libraries and tools to easily deploy IXA capabilities

Flexible Enterprise Router

The Intel Internet Exchange architecture enterprise router shown in Figure 1 provides an excellent example of how IXA provides compelling solutions for OEMs and third-party developers.

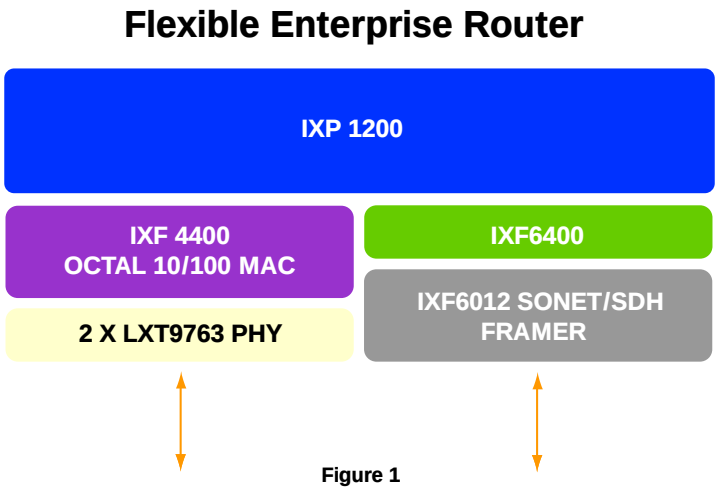

Figure 1

The IXP1200 network processor is the heart of a flexible platform that replaces fixed-function ASICs. This high-performance network processor supports software-based switching and routing at wire-speed, with programmability that enables software algorithms to be added to support new services over the life cycle of the router. The new services are those that require deep packet inspections, such as firewalls or VPNs. The IXP1200 is a low-power device that supports high-density communications equipment applications.

Intel IXA supports a standardized hardware interface that enables the relatively fast and simple integration of IXF framing devices without significant amounts of interface logic. The IXF components support Octal 10/100 Ethernet and OC-12 SONET, and include the IXF64xx SAR (segmentation and reassembly) device.

Software Solutions

In addition to hardware building blocks, Intel IXA-based platforms utilize libraries and development tools from Intel and third-party software components that can be mixed and matched by OEMs. Software stack options include the Linux* operating system or a real-time operating system, and a variety of protocol stacks and protocol engines supplied by Intel and third-party software developers.

Intel Internet Exchange architecture also includes the IX-API, a simplified development and programming environment that will allow a single data plane code stream to be used over a family of network processors. A complete solution would consist of the data plane solutions built using the IX-API development tools, and control and management processes that are typically provided by the OEM or third- party software developers.

A typical software solution is shown in Figure 2.

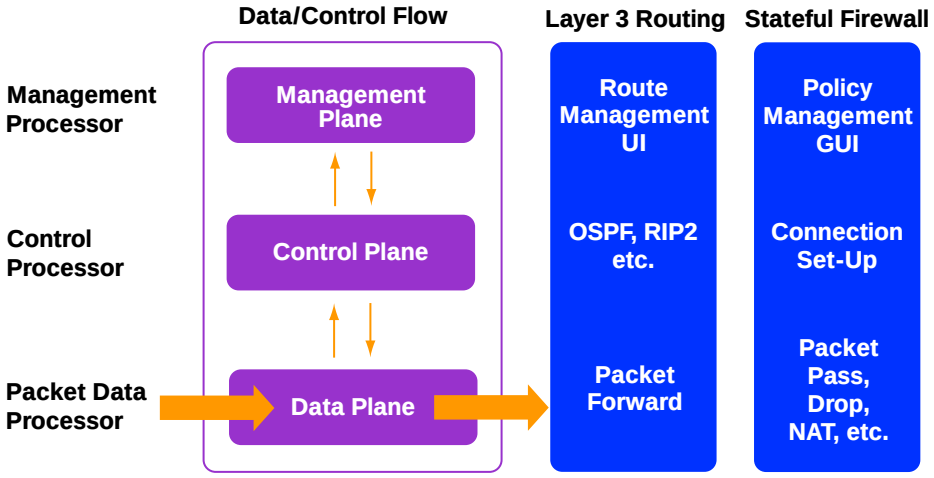

Figure 2

Evaluation Kit

Intel will be providing reference designs similar to the Enterprise Router described in this article. Available now is the IXP1200 Network Processor Evaluation Kit, designed to facilitate product development. It includes software and hardware that support new designs that incorporate the performance, scalability, and low-power requirements of the Intel IXP1200 network processor.

The IXP1200 Network Processor Evaluation Kit includes:

- The Intel IXP1200 network processor software development environment
- An example of network application code
- Documentation
- PCI form factor board (based on IXP1200 network processor) with two Gigabit Ethernet ports
- Passive PCI backplane
- Network interface card that enables a system host processor to communicate to the IXP1200 network processor.

Summary

As the growth of the Internet drives requirements for more complex products and the continuing differentiation of network services, Intel Internet Exchange architecture provides straightforward design solutions that can help OEMs and developers meet customer needs. The IXA-based enterprise router described in this article provides an excellent example of how the IXP1200 network processor can be used to deliver ASIC-level packet processing performance, with low-power components that support high-density designs and embedded product life cycles.

The combination of a consistent hardware interface with APIs and programming tools can dramatically shorten time-to-market compared to ASIC-based designs while enabling a comprehensive solution using best-in-class components. The use of a programmable network processor provides a high level of scalability and product upgradability for network equipment OEMs while enabling third-party developers to create a variety of new software applications and platform solutions.

More Info

For more information on Intel Internet Exchange architecture, visit Intel's IXA Web site.

Detailed information on the benefits of membership in the Intel IXA Developers Forum is available on the IXA Developers Forum Web site.

For additional information on the Evaluation Kit for the Intel IXP1200 Network Processor visit Intel's Developer Site.

Author Bio

Kerry Bott directs Intel Internet Exchange architecture platform strategies as the director of Product Marketing. He joined Intel in 1988 and has been primarily involved in Networking Products including print servers, storage servers, and networking architecture. Prior to joining Intel, Kerry served in various engineering capacities at Graphics Software Systems and Motorola, Inc. Kerry holds a B.S. degree in Mathematics and Computer Science from Oregon State University.

Desktop

System Test-IF Introduces PC 2001 Tests

Chuck Woodman
Product Marketing Engineer
Platform Compliance Operation
Intel Corporation

Overview

The System Test Implementers Forum (IF) is a group of industry system builders and PC platform developers who gather semi-annually to review test specifications and requirement tests that relate to design guidelines contained in the PCxx System Design Guide.

Representatives from many companies throughout the industry attended the fourth System Test-IF (System Test-IF 4) in San Diego July 18 through 20. The event, co-sponsored by Intel and Microsoft, was made up of the PC 2001 Test Specification Review and the first Test Fest based on PC 2001 related tests. One attendee said System Test-IF events are "a great means of obtaining contacts and one-on-one time with key Microsoft and Intel personnel…more people should come, and more companies should be involved."

PC 2001 Test Specification

The PC 2001 Test Specification that results from this summer's event will be the third generation of PCxx Test Specifications to be produced by the System Test-IF. As with the PC 99 Test Specification Release 2, published in December 1999, the PC 2001 Test Specification will introduce areas of test coverage not found in previous versions. The 0.7 draft under review at the event represents the latest opportunity developers have to review and influence the testing criteria that will apply to PC hardware designs planned for market release in the later part of 2001.

PCxx Test Specifications are designed to make it easier for developers to meet requirement baselines by providing an objective set of pass/fail criteria. By defining test criteria for feature requirements as well as for industry standards and specifications, these test specifications form a technical interpretation of the System Design Guide. PCxx Test Specifications are co-authored by Intel and Microsoft, and publicly reviewed by System Test-IF members prior to the test assertions being finalized. These reviews offer the industry an opportunity to participate very early in the process of test development.

Specification Review

Throughout the first two days of System Test-IF 4, participants reviewed the 0.7 draft of PC 2001 Test Specifications. Topics under review included EFI, USB, ATA, ACPI, and Legacy Free. Participants discussed controversial issues involved in the testing of the new PC 2001 System Design Guide requirements such as various methods of testing a given requirement and coverage of various implementation methods.

Also included in the event were forward-looking discussions on Bluetooth, CNR, and USB 2.0. These sessions included technology overviews as well as in-depth discussions on testing the technologies. They were among the best attended sessions, and the audience indicated that the technology overviews were very helpful.

In both the Spec Review and forward-looking sessions, test designers received direct feedback concerning issues that present hurdles for the industry in terms of product design and testing. The Forum used an audience response system to tally and record audience opinions on these topics. For example, in the USB 2.0 session, it was determined that system port testing is very important (37 percent of the audience considered this the most important area for USB testing, and 60 percent rated the importance of testing this area a 5 on a scale of 1 to 5). A detailed set of scribe notes was also recorded for each session and has been posted on the System Test-IF Web site.

Test Fest for One-on-One Testing

System Test-IF 4 also featured Test Fest, a members-only event where attendees brought early products, and Intel and Microsoft engineers provided individual, one-on-one testing sessions with each member company. OEMs and IHVs were able to bring their latest designs and run tests on them in the presence of the test authors.

This Test Fest was the second sponsored by the Forum. It featured the debut of the first alpha-level release of the PC 2001 tests, and all sessions were full. According to one participant, “This is a great opportunity for developers to test/debug their hardware/software. Thanks, it was a great event.”

Tests

Alpha-level tests for PC 2001 are available now for download by members only at the System Test Web site. By running these tests in this early stage, Forum members help to improve the quality of the tests, as well as getting an early indication of product compliance.

A special addition to System Test-IF 4 was a “Usability Study” in which conference attendees ran the tests and provided feedback on the usability of the tests. A lot of great feedback was gathered, and one test subject commented, “I think [the Usability Study] was a great idea. I would participate even if you didn’t give away shirts.”

Beta-level tests for PC 2001 are scheduled for release by the end of the year and will be available for download to the general public. This approach gives everyone the opportunity to perform early testing and to design in the features and functionality described in the System Design Guide. Comments on the tests are welcome at comments@systemtest.org.

Summary

The System Test Implementers Forum is an industry group that gathers to review test specifications and requirement tests. Members recently attended the fourth System Test-IF (System Test-IF 4) in San Diego. Throughout the first two days of System Test-IF 4, participants reviewed the 0.7 draft of PC 2001 Test Specifications. System Test-IF 4 also featured the System Test-IF Test Fest, a members-only event in which attendees brought their products, and Intel and Microsoft engineers provided individual, one-on-one testing sessions with each member company.

The PC 2001 Test Specification will be the third generation of PCxx Test Specifications to be produced by the System Test-IF. The 0.7 draft represents the latest opportunity developers have to review and influence the testing criteria. PCxx Test Specifications are co-authored by Intel and Microsoft, and publicly reviewed by System Test-IF members. According to an attendee at System Test-IF 4, the forum “has made some significant strides toward better system testing and documentation of these tests.”

Alpha-level tests for PC 2001 are available now for download – by members only – at the System Test Web site. Beta-level tests for PC 2001 are scheduled for release soon through the System Test Web site. Members and nonmembers are encouraged to download and run these tests and send comments to comments@systemtest.org.

More Info

For details on the System Test-IF, Test Specifications and tests, future Forum events, and an application for membership, visit the System Test-IF site.

Author Bio

Chuck Woodman joined Intel in 1996. He currently works in the Intel Platform Compliance Operation, where his responsibilities include industry engagement in support of PCxx Test Specifications and related tests, and event management. Prior to that, Chuck worked in Intel Customer Support, focusing primarily on product support of Intel Desktop System Boards. He holds a B.S.C.S. from Portland State University.

Intel® 815 Chipset for microATX and a Super New ATX Board

Aditya Waghray
Senior Product Marketing Engineer
OEM Platform Solutions Division
Intel Corporation

Overview

Two new Desktop Boards, the versatile microATX D815BN and the D820LP ATX powerhouse, are now available. This article surveys these products' outstanding features.

The Intel® Desktop Board D815BN delivers mainstream features in the microATX form factor. Key D815BN features and benefits include extreme versatility and cost effectiveness. D815BN supports both Intel® Pentium® III and Celeron™ processors, both PC100 and PC133 SDRAM memory, and both integrated Intel® graphics and fast AGP 4x external graphics. System integration costs are reduced by the flexibility to fit into smaller chassis and features such as integrated super-I/O and USB hub providing four USB ports.

The Intel® Desktop Board D820LP is Intel's highest performance desktop board. Key D820LP features and benefits include support for processors with 133/100-MHz system bus and 256K L2 Advanced Transfer Cache, the advanced 370-pin socket connector to support processors in the Flip-Chip Pin Grid Array (FC-PGA) package, and Direct RDRAM for up to twice the bandwidth of SDRAM. AGP 4x capability supports more realistic 3D graphics, 2x I/O performance delivers lifelike audio and video, and the Instantly Available PC feature adds a consumer electronics look and feel. This ATX form-factor board provides more power for the Internet, your network, and beyond.

Desktop Board D815BN – a Closer Look

Graphics Options for Consumers and Business

The Intel Desktop Board D815BN combines versatility with performance to serve the needs of the mainstream, the performance-driven, and the value-based consumer and business markets, all in a single solution. Based on the new technology of the Intel® 815 Chipset with integrated graphics, the D815BN supports Intel Pentium III processors with 100/133-MHz system bus speeds and Intel Celeron processors at 66-MHz system bus speed through the PGA 370 socket. The Intel 815 Chipset allows users to choose the integrated graphics capability with a Graphics Performance Accelerator for higher display cache, or upgrade to a high performance AGP graphics card with the ability to extend to a 4x data transfer.

Design Flexibility for Low-Cost Solutions

The D815BN is built on the microATX form factor, which offers significant cost savings through smaller and more flexible chassis. In addition, the 815 Chipset provides a mainstream I/O controller hub feature that leverages the reliability of the PCI system bus and IDE controller with ATA-66 access speeds, at a low cost. Also, the D815BN offers system integrators the options of ADI 1885 soft audio and an integrated Intel® 82559 LAN controller, to enable additional product offerings. The D815BN thus provides a range of price/performance points in the adaptable microATX form factor.

D815BN Details

Processors: Supports Pentium III processors and Celeron processors in the Pin Grid Array (PGA) socket with 133-MHz, 100-MHz, or 66-MHz system bus.

Chipset: The 815 Chipset, Intel's latest, provides flexibility to support all system bus designs with new performance features. The 815 Chipset delivers integrated graphics capability, which can be scaled for multiple system price/performance points.

Graphics: A universal AGP 4x connector supports the latest graphics technology.

Expandability: One AGP slot and three PCI slots. In addition, up to four USB ports (dual-stack rear connectors and header for two front panel connectors).

Connectivity: Optional Intel 82559 LAN controller for 10/100 Ethernet connectivity.

Memory: Supports PC133 and PC100 SDRAM in three DIMMs, for up to 512 Mbytes of memory.

Audio: Optional ADI 1885 soft audio, with audio line in, line out, and microphone.

BIOS: OPSD Enhanced AMI Core BIOS, BIOS Security Suite and Intel® Rapid BIOS Boot for faster system availability.

Management Features: Advanced power management, Wake-On-LAN, and WfM (Wired for Management) are implemented, and the Heceta 4 Hardware Monitor is optional.

Other Features: Optional Digital Video Out header, enabling digital CRT, flat panel, or TV-out functions.

Desktop Board D820LP – a Closer Look

Advanced Technologies for Performance PCs

The Intel Desktop Board D820LP features the new Intel® 820 Chipset, offering system integrators the latest in PC technology, while enabling new and exciting performance capabilities. The Desktop Board D820LP is a follow-on to the VC820 platform, supporting the latest FC-PGA package Intel Pentium III processors at 133-MHz system bus speed. In addition, it supports RDRAM memory technology, which delivers twice the bandwidth of SDRAM. The Desktop Board D820LP is the leading-edge performance platform solution for system integrators who want to provide their customers the latest in PC technology.

New Performance Features

The D820LP with the new Intel 820 Chipset supports exciting new technologies, including a 133-MHz system bus, RDRAM memory, AGP 4x, Ultra ATA/66, and the Instantly Available PC power management mode as well as Intel Rapid BIOS Boot and Express BIOS Update. The combination of these features with the Intel Pentium III processor enables exciting system designs. The friendly ATX form factor, five PCI slots, and AGP connector give system integrators a reliable, stable, and flexible platform.

Design Flexibility, Easy Integration

The Desktop Board D820LP also provides system integrators with maximum design flexibility by supporting both 133-MHz and 100-MHz system bus designs. System integrators benefit from Intel's extensive compatibility and validation testing that helps ensure consistent and reliable performance.

D820LP Details

Processors: Supports Pentium III processors in the latest FC-PGA socket with 133-MHz system bus.

Chipset: The 820 Chipset provides flexibility to support both 133-MHz and 100-MHz system designs, with new performance features. Three components make up the chipset: Intel® 82820 Memory Controller Hub (MCH), Intel® 82801AA I/O Controller Hub (ICH), and Intel® 82802AB Firmware Hub (FWH).

Graphics: A universal AGP 4x connector supports the latest graphics technology.

Expandability: One AGP slot and five PCI slots. Two USB ports on back panel. Optional five USB ports, configured three back/two front.

Connectivity: Optional Intel 82559 LAN controller for 10/100 Ethernet connectivity and Wake-On-LAN.

Memory: Two RDRAM RIMM connectors, for up to 512 Mbytes of memory. Supports PC600, PC700, and PC800 RAMBUS* memory with both ECC and non-ECC.

Audio: Optional Creative 1373 Digital and Crystal 4297 codec.

BIOS: AMIBIOS and Intel Rapid Boot BIOS for faster system availability.

Summary

Intel has introduced two new Desktop Boards. The Intel Desktop Board D815BN delivers mainstream features in the microATX form factor, which offers significant cost savings through smaller and more flexible chassis. Key D815BN features and benefits include extreme versatility and cost effectiveness. The Intel Desktop Board D820LP is Intel's highest performance desktop board. This ATX form-factor board provides more power for the Internet, your network, and beyond.

More Info

Information on Intel® Boxed Desktop Boards is available at Intel's channel site.

Also see the Desktop Board pages on Intel's Developer Site, specifically the pages on the Desktop Board D815BN and the Desktop Board D820LP.

Information is also available in the desktops/workstations section of Intel's Support Site.

Author Bio

Aditya Waghray is a senior product marketing engineer with Intel's OEM Platform Solutions Division (OPSD). Before joining Intel and OPSD earlier this year, Aditya worked for Hewlett-Packard and Ernst & Young. He holds an M.B.A. from Carnegie-Mellon University and a B.S. in Industrial Engineering from the University of Illinois.

Software to Deliver Ease of Use to Internet Users

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Overview

Although the industry has made enormous strides in speeding up PC processes, studies show that end users still perceive the PC as slow and sometimes difficult to use. Often this is because the user still has to go through a series of steps to perform one action in a given application, such as downloading and reading e-mail.

Usability is an ongoing industry issue that Intel has addressed in OPSD (OEM Platform Solutions Division) Software Engineering. The group developed Ease of Use applications targeted for the consumer market. This article shares some tips and techniques for usability design that the group has learned over the past 18 months.

Foundations of Our Approach

To develop Ease of Use applications that would speed up the Internet experience and make the process more enjoyable for end users, OPSD adopted the concept of Design for Usability, a methodology for including human factors thinking in product development, introduced by Intel's User Centered Design Group. A key factor in implementing Design for Usability in many of the applications was Instantly Available PC (IAPC) technology with the OnNow Power Management API from Microsoft.

IAPC technology allows OEMs to design full-featured, high-performance systems that meet stringent sleep state targets while delivering new, useful, and exciting platform capabilities. APC employs a configuration-independent mechanism that removes power from all major subsystems such as graphics, audio, the processor, and the hard drive when the system is asleep. The IAPC architecture also allows certain parts of the system, such as modems and network interface cards, to draw a small trickle current that enables them to wake the machine when an external event, such as an incoming fax or phone call, occurs.

OnNow provides enhanced features for end users and improves system power efficiency and robustness for Internet or intranet applications, multimedia applications, and scheduling applications.

Why Design for Usability

The earlier Ease of Use is implemented into application design, the less expensive and time consuming development, testing, and deployment will be because usability problems are more likely to be solved early in the process. Intel® IAPC and OnNow API both help speed the development of software applications that make PCs easier to use. Contributing adopters who want to use the two specs to integrate usability into their applications can download them today.

The Advantages of Human Factors Engineering

Having a human factors engineer (HFE) on board when developing applications reaps huge dividends in terms of both time and money when developing applications. The HFE provides usability expertise during each stage of development, testing, and implementation. This involvement ensures your application will be more user friendly and successful from first release, and it greatly cuts down on the time and cost of fixing usability problems later on. See Figure 1.

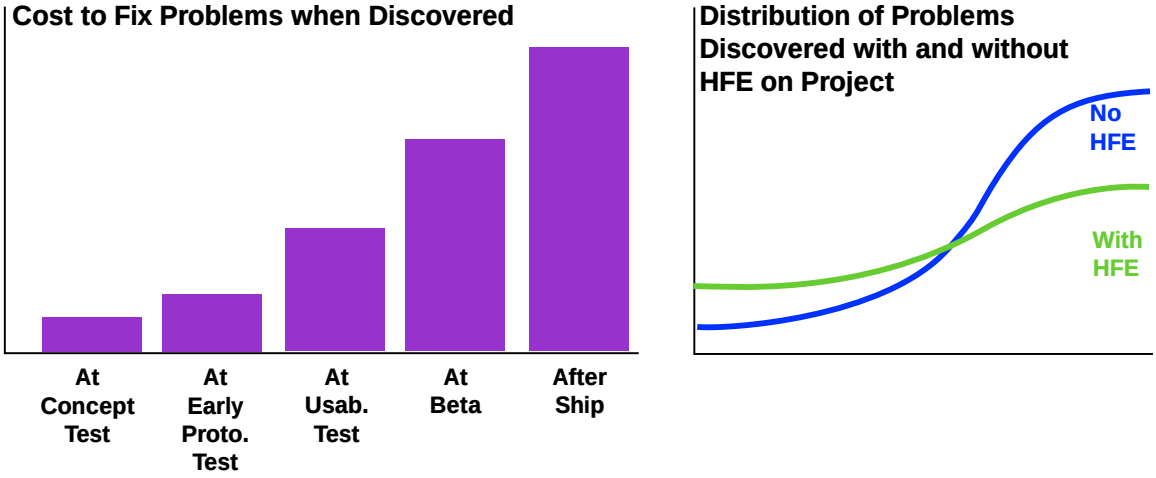

Figure 1

The Design for Usability Process

Investigation Phase

Initial project plans for the investigation phase of designing for usability requires early input on usability objectives. Create a usability plan for your applications, then communicate these plans to third parties. Analyze your requirements to identify and characterize your users and their environment. Identify system requirements for the user interface, then conduct a competitive analysis as well as a task analysis. During the earliest stages of design, translate your requirements into design concepts and define your major user interface objects. Develop a user interface interaction model, then establish measurable usability goals.

Design Phase

In refining your design, conduct iterative prototype tests, and verify compliance with standards. This is the time to test the usability of user interface icons.

Development Phase

During implementation, conduct usability tests on the product, as well as the associated user documentation and learning materials. This is the time to find and correct any usability problems. Incorporate usability testing in your beta and post release plans.

Testing Phase

Monitor your beta testing, and work with customer service to track all usability problems.

Sustaining Phase

Perform a post-release assessment, and use this usability information in next-generation application design plans.

New IAPC Capabilities Benefit Internet Users

Some end users perceive the PC as too slow because of their experience with the Internet. Modems sometimes connect at a rate slower than 56K, users must wait for connections, and banner ads need to be downloaded, which takes additional time. Intel IAPC used together with OnNow APIs, lets developers address this problem by giving applications the ability to preload content. A system can be programmed to awaken at off-hours, connect to the ISP, and download a user's preselected content, including e-mail messages, from various Web sites.

In Figure 2, the Mail Load program dials up the ISP and downloads e-mail. Mail Mon monitors the Inbox and flashes the Message Waiting LED (usually the power LED) if there are unread messages. Both programs are added to an existing Windows* 9X-based system.

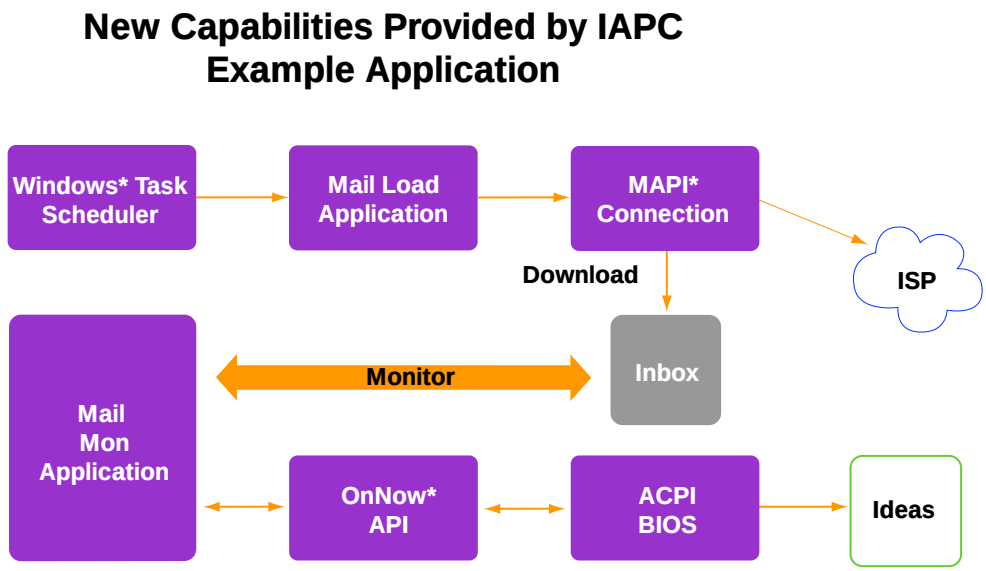

Figure 2

Before implementing this scenario, the end user must follow several or all of the following steps in order to read e-mail:

- Power on system
- OS boot
- Connect to ISP
- Start e-mail application
- Download e-mail

By adding the capability to preload content to the e-mail application, developers can reduce the user's efforts to just one step–hitting the e-mail button on the keyboard when the message LED flashes.

Summary

Developers should include a Design for Usability approach in their current software projects. When usability is factored into every phase of the design process, usability problems are solved early, resulting in faster, lower cost development. Intel IAPC specs and OnNow APIs for IAPC can be downloaded now, and used by developers to speed up and enrich the Internet experience for end users.

More Info

You can find more information about OnNow Power Management Architecture for Applications and Windows Power Management Configuration Tools on Microsoft's Web site.

To learn more about the Advanced Configuration and Power Interface Specification, visit the ACPI specification Web site.

Cost Justifying Usability, Randolf G. Bias & Deborah J. Mayhew, Academic Press, 1994.

Author Bios

David C. Stewart is the software engineering manager for Intel's Desktop Board business. His projects include consumer entertainment software, board bringup tools, system integrator tools, manageability, and set top user environments. He has worked in the software development business for 17 years. David received both his B.S. and M.S.C.S. degrees in Computer Science from Colorado State University.

Paul F. Sorenson manages Intel's User Centered Design Group, an internal consulting team focused on understanding how end users interact with technology. He began his career at Intel in 1994 with the company's PC Enhancement Operation, which marketed Intel's first consumer products.

Paul has been a core team member on the PC Ease of Use Roundtable since its inception. He leads Roundtable efforts on the Design for Supportability Guidelines and the Initial Experience Predictor Tool now in use by Intel and many PC OEMs.

Before joining Intel, Paul spent a more than a decade at IBM Corp., Lockheed Martin Corp., and the Hewlett-Packard Co. working on a wide range of products, including the first PC mice, advanced User Interface prototyping systems, and the first palm-top PCs.

Paul holds a bachelor's degree in biology from Willamette University and a master's degree in Neurophysiology/Linguistic-semantics/Experimental Psychology from the University of Oregon. His doctoral work was with the University of Texas, Austin in Human Experimental Psychology.

New Test Suites and Matrix for IAPC

Raju Doshi
Initiative Technical Manager
Technology and Initiatives Marketing
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Overview

On July 1, 2000, the new Environmental Protection Agency (EPA) ENERGY STAR specifications went into effect. For more information on this refer to the July 2000 article titled "ENERGY STAR and Instantly Available PCs." These specifications included a sleep state power requirement for personal computers (PC). Now, ENERGY STAR certification requires that the sleep state draws less than 15 watts while still retaining full communication capabilities. The ENERGY STAR logo is required for many federal, state, and local government purchases.

The Instantly Available PC (IAPC) power management technology gives developers a set of recommendations for power delivery requirements. These recommendations help ensure that future PCs achieve full IAPC S3 (system sleep state) and D3 (device sleep state) functionality.

Developers need to immediately begin implementing S3/D3 capabilities in their systems. Developers also need to start testing for S3/D3 compatibility in-house.

What is IAPC?

"Instantly Available" refers to a power management system that allows a PC to go into a low-power sleep state when not in use. In this sleep state, the PC must still be able to return to fully functional state triggered by a wake event in order to answer a phone, receive a fax, send or receive e-mail, and so on.

Having a quick resume time eliminates the need to power-down the PC to save energy when the PC is not in use. By keeping the machine in a sleep state instead of powered down, the lengthy reboot process is virtually eliminated. The sleep state itself reduces power consumption of an idle PC from 25 to 30 watts (a 1998 PC) to 15 watts or less (an S3-compliant PC).

The S3/D3 power management system provides IAPC capability. For example, when a PC is placed in the S3 sleep state, system contents are saved to memory, and the power consumption drops (ideally) to 5 watts or less. A trickle power is maintained in communication subsystems and peripherals, such as modems, and in wake-capable buses (such as a keyboard or mouse). When the PC is awakened, the previous state is restored from memory.

Already many PCs are drawing less than 5 watts while in the sleep state. Some systems draw less than 3 watts. Worldwide, many OEMs are now shipping systems with S3 capability. For example, Compaq recently started shipping the Deskpro EN* series with S3 Suspend to RAM (STR) as the default. These Deskpro PCs draw about 3 watts while in the S3 sleep state. Other manufacturers who are shipping PCs with S3 capabilities include HP, Fujitsu, Siemens, IBM, Samsung, Legend, Mitac, ACER, and PB/NEC.

Resume Times and Reliability

The S3/D3 implementation must be as reliable as booting up the system. In general, the operating system (OS) has ways of determining how to implement sleep states. For example, if something fails during the resume process for a Windows* 2000 operating system, the OS can go back into S1 mode during the next power-down cycle.

Currently, resume times from S3 are running about 4 to 5 seconds for Windows 2000 operating systems, and 9 to 15 seconds for Windows* 98 Second Edition operating systems, depending on the implementation. These resume times must be further reduced so that they are similar to the resume times of consumer electronics (such as VCRs and TVs). A reasonable goal is a PC resume time of 5 seconds or less.

The IAPC Ideal

The IAPC technology is a key ingredient in the end user ease-of-use effort. Ideally, an IAPC should be able to receive faxes, e-mail, pings, and so on, even in the sleep state. The ideal IAPC should have the following features:

- ACPI (advanced configuration power interface) BIOS support.
- S3 support.
- A low-power draw (5 watts or less) in the sleep state.
- Fast resume time (5 seconds or less).
- Vaux (auxiliary voltage) to maintain trickle power to PCI (peripheral communications interconnects) devices while the rest of the PC is in its sleep state.
- The ability to wake up from PCI and CNR (communications network riser) devices, USB wake-capable devices, and PS/2 keyboards and mouse.
- No noise in the sleep state–the fans are off. The fans should not be needed because, in the sleep state, the power to the processor is cut off and only memory gets power.

Achieving ideal instantly available functionality for peripherals or add-in cards depends on the specific peripheral or add-in card.

Current and Future S3, S4, and S5 Requirements

Current design guide requirements state that all PCI devices should support the D3 sleep state, and wake-capable PCI devices must support wake from the D3 sleep state. This enables the PCs that support S3 to wake on ring (WOR) and wake on LAN (WOL). Graphics and display devices must support D0-D3 states, and audio devices must also implement and support D0-D3 states. S3 implementation for systems is recommended but not required at this time. This is expected to change in the PC 2001 design guide.

Future Hardware Compatibility Tests are expected to test the ability of wake-from-PS/2 keyboard and mouse, USB devices, CNR devices, and other wake-capable devices.

The future of IAPC is clear. Developers should start looking at implementing the features that are even now being drafted into the PC 2001 System Design Guide draft 0.9. The PC 2001 draft requirements for system design include:

- S3, S4, and S5 sleep-state support
- S3 wake from PS/2 keyboard/mouse
- S3 wake from USB wake-capable devices
- S3 wake from CNR devices

The requirements for peripherals and add-in cards are also in the PC 2001 System Design Guide.

WHQL Logo and S3

Currently, WHQL (Windows Hardware Quality Labs) logo certification requires D3 compatibility for all PCI devices. Compatibility is verified through the PCI-D3 test suite (incorporated into HCTs).

Intel now offers the PCI-D3 test suite as a free download to developers. The PCI-D3 test suite covers:

- Modem (WOR) and LAN (WOL) devices for D3 compatibility
- Graphics, display, and audio devices for D3 compatibility

Intel also offers developers a free IAPC test matrix. This includes the above PCI-D3 test and also goes through steps to check the motherboard for S3 compatibility and peripherals for D3 compatibility.

The IAPC test matrix lists the categories for testing at a system level. Categories include verifying BIOS, verifying wake-from-PS/2 keyboard/mouse, verifying wake-from-USB keyboard/mouse, and so on. Once the test matrix is filled out, the matrix is a good indicator of the level of your system's S3-STR compliance.

System integrators and IHV can download a free copy of the Intel PCI-D3 test suite and the IAPC test matrix from the Intel Developer's IAPC Web site. The test suite has been incorporated by Microsoft into the Microsoft hardware compatibility test (HCT), version 9.6.

What's Ahead

Currently, the WHQL logo requires that PCI devices are tested for and support D0-D3-D0 transitions. To ensure D3 compliance, developers should test their PCI devices whether they are add-in cards or are on the motherboard before they submit the devices for WHQL logo certification. Developers can use the PCI-D3 test suites and the IAPC test matrix as the test tools. Microsoft's latest release of HCT 9.6 incorporates the PCI-D3 test suite.

In the near future, when PC 2001 SDG is released, systems will be required to support S3. Systems will also be required to support wake from all wake-capable devices/buses. Add-in card and device manufacturers will also be affected by the change, since all wake-capable devices (not just PCI devices) will be required to support D0-D3-D0 transitions. This includes USB and CNR devices.

Tests that ensure compliance with the new requirements will be added to the HCTs. OEMs and independent hardware vendors (IHV) are strongly encouraged to review the draft version of the PC 2001 system design guide and begin implementations that will ensure compliance with the new requirements.

Summary

With the EPA's new ENERGY STAR requirements in effect, developers should be testing in-house now for S3 compatibility for PCs. Developers should also be testing in-house for D0-D3 compatibility for graphics, display, audio, LAN, and modem devices. Developers who want to plan for the future should be implementing now for the PC 2001 design-guide recommendations, which include S3 compatibility for all wake-capable buses, CNR devices, USB devices, and so on.

PC 2001 System Design Guide draft 0.9 is available free for download for developers. Developers are strongly encouraged to review it and begin implementing the changes in requirements for S3 and D3 functionality.

Intel now offers a free test suite and test matrix to developers to help ensure S3/D3 compatibility. The PCI-D3 test suite and IAPC test matrix are available online at the Intel's Developer Site. The site also includes articles, lists of S3-compatible platforms and devices, and other information valuable to developers.

More Info

Intel's Developer Site offers in-depth articles on IAPC, design-guide requirements, known-good S3-compatible platforms and devices, and other information. Check out the Instantly Available Technology area of Intel's Developer Site to download the S3 test suite and IAPC test matrix, which are freely available to developers.

Intel also offers a Web page that lists reference platforms. This area includes information about some of the systems that Intel has tested and found to be robust. Each of these systems has gone through several thousand cycles of S3 and the test suite. Vendors can use the list to identify a reliable system on which to test add-in cards and other peripherals.

The industry involvement area lists information about peripherals (such as add-in cards) that have been tested and that comply with S3. System vendors can use this list to identify a reliable add-in card on which to test an audio subsystem, a graphics subsystem, and so on.

For details on IAPC and Intel's role in the new EPA ENERGY STAR requirements, see "ENERGY STAR and Instantly Available PCs," published in the July issue of Intel Developer Update magazine.

Author Bio

Raju Doshi is an initiative technical manager in the Technology and Initiatives Marketing unit of the Intel Architecture Group. She has been with Intel for five years. Prior to her current position, Raju worked as a technical marketing engineer for the Intel® Pentium® 4 processor and as a hardware reliability engineer for servers. She holds a B.S.E.E. from Michigan Tech University.

Innovative PC Recognition Program: Designing Outside the Box

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Overview

Consumers want PCs that are simple to set up, easy to expand, and are more energy efficient, smaller, and quieter. Today, there are many innovations that make PCs easier or simpler to use: S3 Suspend to RAM (STR) sleep state, the Universal Serial Bus (USB), FlexATX motherboards, which enable small size and light weight, integrated networking, wireless technology, and so on.

Innovative features have benefits to both first-time and repeat PC consumers. They:

- Get users up and running more quickly, reducing the "box-to-boot" time
- Help first-time PC users overcome usability barriers
- Make peripherals and software easier to install
- Make operation quick and quiet
- Reduce user frustration
- Help reduce support costs, including PC-related power costs
- Reduce cable clutter
- Save desk space
- Enable a positive user experience

Many standard PCs rely on existing beige-box configurations to address consumer needs. Intel wants to encourage developers to step outside that beige box and explore ways of making PCs simpler to configure, easier to use, and more visually appealing. To help encourage developers, Intel has created the Innovative PC Recognition Program. This program allows Intel to showcase designs that merge innovation and simplicity to create a compelling PC platform.

Criteria for the Award

The Innovative PC Award is earned by original-equipment manufacturer (OEM) PCs that advance the state-of-the art in three key areas: innovation, simplicity, and style. Manufacturers must qualify in all three categories to receive the award. Winners are announced twice a year, at the Intel® Developer Forum Conference.

Innovation

PCs that score high in innovation are easier to use. They also solve common problems, such as incompatibility issues with outdated connectors. Factors that influence the scoring in this category include:

- Legacy removal—removal of outdated connectors (serial, parallel, game, MIDI, and other outdated ports)
- USB ports on the front of the PC for easy walk-up access
- USB ports on the back of the PC for stationary devices like printers and scanners
- A configuration that allows right- or left-handed mouse use
- Instantly Available PC, or low-power sleep states that keep the PC quiet when not in use, yet ensure that it is quick to respond when needed
- Fast boot and resume times
- Integrated home networking
- Wireless technology (preferably RF connections, rather than laser or infrared technology, because of line-of-sight issues with the latter two technologies).

Simplicity

PCs that score high in simplicity are easier to unpack and set up. Simplicity is judged through the use of a tool called IEP (Initial Experience Predictor). The IEP tool was developed by the PC Quality Roundtable and focuses on consumer desktop PCs. The IEP measures the initial, out-of-box experience that a computer novice would have. For example, scoring in this category is influenced by:

- Packaging—how easy it is to get out of the box? Ease of unpacking is improved by decreasing the size and weight of the PC. Adding a handle also helps users unpack and set up the PC.
- Making setup easy.
- Minimizing the number of external wires that have to be connected.
- Including preloaded software that is easy to use in its default configuration.
- Reducing desktop clutter—limiting the number of icons visible at power-up.
- Including preconfigured Internet access. For example, is there an automatic dialer already configured to a free Internet service?

Style

This category encourages creativity and style. Color, size, weight, shape—PCs that score well in this category are not the old, standard beige boxes.

Winners

Winners are judged on how well they merge innovative features with simplicity, ease of use, and style. Winners are not judged on how successful or unsuccessful they have been in the marketplace. Instead, winning PCs demonstrate innovative concepts that have become reality.

Past winners have included:

- The Dell WebPC*
- The Compaq Presario EZ2700*
- The Packard Bell Z1*

Current winners are:

- IBM NetVista* X40
- Daewoo Qrium* 663X and 663N
- Legend Tian Xi*

IBM NetVista X40

This PC has superior all-in-one design. During unpacking, your first reaction is likely to be “Where's the computer?” The CPU port is on the back of the monitor, and the traditional CPU box is incorporated right into the base of the monitor. The CD-ROM is tucked out of sight in a bay under the monitor. This bay drops down whenever you need to use it; when it's not in use, it's out of sight.

The NetVista has a built-in-handle on top of the monitor/CPU, which makes it easy to remove from the packaging materials. This lift is even easier because the LCD panel is so lightweight. And, since this PC has an integrated design, there are far fewer cables that have to be connected. Consumers can go from the box to the Internet in about 10 minutes.

The IBM PC we tested ships with an Intel® Pentium® III processor 667 MHz, a USB keyboard and mouse, and built-in network software. It includes a total of seven USB ports, which gives users lots of expansion capabilities and allows easy plug-in of new devices without having to reboot—all the wonderful features of USB.

Two of the USB ports are on the keyboard, one on the right side and one on the left. The mouse can connect directly to the keyboard. This helps reduce cable clutter, and allows both left- and right-handed users a comfortable position for the mouse.

In short, this is a very flexible, very expandable machine that takes up a lot less space on the desktop than standard PCs.

Daewoo Qrium 663X and 663N

The Daewoo Qrium has eliminated all old connector ports—PS/2, MIDI/game, serial, parallel, etc. All four available ports are now USB, and the Qrium ships with a USB keyboard and mouse. The 663N model places two of the USB ports on the front panel for easy walk-up connections, while the 663X opts for two USB ports on the side near the front panel. Both the 663N and 663X feature two USB ports on the back panel for static devices. Both systems include integrated Ethernet, which makes it easy to support an external broadband modem with no need to open the chassis. One of the most important features of this PC is its fast boot (through an optimized BIOS) and fast resume time.

Stylistically, both the 663X and the 663N are appealing: small, lightweight, easy to unpack, and easy to set up. The 663N model is cube-shaped, about seven inches square, sloped a bit on the sides, and bright yellow. Even more novel, the 663X has an intriguing asymmetry—like a distorted pyramid—definitely not beige or boxy.

The Qrium we tested ships with an Intel® Pentium® III 600 MHz, integrated networking, and a free online Internet service that is already set up for first-time users.

These PCs are sold in Korea under the Daewoo brand and in the U.S. under the Datus Qrium brand.

Legend Tian Xi

This PC, which sells only on the Chinese market, includes several innovative features. First, the PC ships with voice recognition software for simplified Chinese, a modern technical language. The PC also ships with a handwriting tablet for users to enter ideographs.

As with other winners, the Legend has eliminated many of the legacy ports—PS/2 MIDI/game port, and so on. This PC then adds a total of eight USB ports, seven of which are available on the hub that attaches to the base of the monitor. The Legend PC is preloaded with a Chinese ISP.

Although the Legend is not the smallest PC we tested, there is a built-in, recessed handle in the top of the PC to make it easy to lift the chassis out of the packing box. Consumers also have a choice of several color schemes for the monitor, mouse, keyboard, handwriting tablet, and chassis: hunter green with beige, royal blue with beige, and so on.

The Legend includes a Pentium III processor, but one of its most forward-looking features is the Instantly Available PC S3 Suspend to RAM sleep state. This S3 STR allows the PC to attain a sleep state that draws under 5 watts, while allowing communication software to remain active. The S3 STR also allows the PC to comply with the latest U.S. Environmental Protection Agency (EPA) Energy Star requirements, which went into effect in June 2000. This means that the PC will draw minimal power while inactive, yet be able to return to an active state within seconds in order to answer the phone, receive a fax, download e-mail, and so on.

Summary

A consumer's initial reaction to a PC is an important part of the overall PC experience. Innovation, ease-of-use, and style all contribute to the consumer's first impression. These factors not only help determine—and reduce—the user's frustration level, but later influence the user's willingness to buy another PC.

The Innovative PC Award allows Intel to recognize manufacturers who have advanced the state-of- the-art in computing and, at the same time, have pushed innovation, ease of use, and style beyond the norm. The award lets Intel showcase some of the great features and technologies that have been incorporated into PC designs.

Although the Intel Innovative PC Award is currently focused on consumer/home-use PCs, Intel is looking into expanding the award to include business and mobile platforms.

More Info

You can find more information about the Intel Innovative PC Recognition program in the Ease of Use section of Intel’s Developer Site.

Conclusions from the Ease of Use Roundtable are located on the organization’s site.

If you are interested in submitting a system for consideration for the award, contact your Intel field team. Guidelines for applications and submissions are also found in the Ease of Use section of Intel’s Developer Site.

Author Bios

Matt Dunford has been with Intel for eight years and is currently managing the New Marketing Programs team in the Consumer Desktop Marketing group. He holds a B.S. in Electrical and Computer Engineering from Oklahoma State University, and holds two U.S. patents.

Jason S. Whetstone has spent his three years with Intel in the World Wide OEM Marketing Programs area of Intel’s Consumer Desktop Marketing group. In January 1999 he became responsible for the OEM Marketing for Ease-of-Use initiative. Jason works with OEMs throughout the world and also administers the Innovative PC Recognition program. He holds a B.S. in Computer Engineering from California Polytechnic State University at San Luis Obispo.

Dean Chu is a recent college graduate participating in Intel's Rotation Engineer Program. He holds a B.S. in Electrical Engineering from the University of Wisconsin.

Initiatives and Technologies

Intel® Internet Phone SDK Enhances Net Phone Quality

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Intel Corporation

Ramanan Ganesan
Product Development Manager
Intel Architecture Labs
Intel Corporation

Overview

A growing percentage of calls today are transmitted via the Internet, but the technology has not gained acceptance as rapidly as might be expected. One of the barriers that has slowed wider deployment of Internet telephony has been the lack of interoperability across networks. Another reason is the inferior quality of voice due to the best effort nature of the unpredictable connections carried over the Internet. The end user often experiences echoes, delays in hearing, and audio breakup.

Intel's technology improves the quality of voice communication when making a call from a PC, achieving nearly the same quality as when making a call using the plain old telephone system. It also simplifies IP telephony solution implementation by managing both the voice stream and the placing of the call through the network. Soon to be distributed by Dialogic Corporation, an Intel company, the SDK provides an interoperable solution for developers, offers IP telephony service providers an opportunity for services innovation and market differentiation, and delivers a higher quality experience to end users. Acoustic echo canceling and dynamic jitter buffering enable open audio support and improve sound quality. The software includes audio and configuration wizards that make it easy to install and enabling a fast first call experience. The SDK's ActiveX is easy to develop with and provide a simple way to customize and integrate the software into portals and services that incorporate IP telephony.

Support of Open Standards

Intel is a member of the International Multimedia Teleconferencing Consortium (IMTC), an industry group comprising more than 150 companies that include Cisco Systems, Lucent Technologies, and Nortel Networks. The Intel® SDK is compliant with IMTC iNOW!, a broad-based industry initiative established to quickly provide IP telephony interoperability. Applications developed with the Intel® Internet Phone SDK are automatically compliant with industry-leading iNOW!-compliant equipment, such as gateways and gatekeepers, allowing IP telephony carriers flexibility to choose building blocks from different suppliers when building their networks.

Better Voice Call Experience

One area of concern in PC-initiated IP telephony is the echo that you hear talking to the person on the PC. This is due to acoustic coupling from the PC speaker and microphone. The Intel Internet Phone SDK includes a software-based Acoustic Echo Cancellation engine that is hardware-independent. This technology provides echo-free full-duplex conversation and is built on the new Windows* Audio architecture called WDM (Win32* driver Model) supported on Windows* 98 and Windows* 2000.

Another common problem with current IP telephony offerings is inadequate sound quality—the clicks and pops that interrupt end users during conversations. Intel's patented dynamic jitter buffering technology solves this problem by dynamically adjusting the buffering to compensate for network variability, delivering a smooth audio experience.

Enhanced Web Telephony Services

The SDK makes it easy for Internet telephony service providers, equipment vendors, and Web portals to integrate this software technology into their Web pages and applications to offer expanded capabilities and new services.

Public Switched Telephone Network (PSTN) Bypass

One of the most common uses of Internet telephony is low-cost long-distance phone service, shown in Figure 1. To initiate a call from the PC, the end user starts a desktop application built on the Intel SDK that connects to an IP telephony service provider (ITSP) network responsible for terminating the call. This process saves money because the end user is charged only for the local call to the Internet provider, even if he or she has made a long-distance call. Another attractive application is Internet call waiting, which enables a person to receive a call even when using the phone line to connect to the Internet. Intel's SDK can be integrated into Internet call waiting services to allow the end user to answer the incoming call from the PC, avoiding simply sending the call to voice mail or having to disconnect to answer.

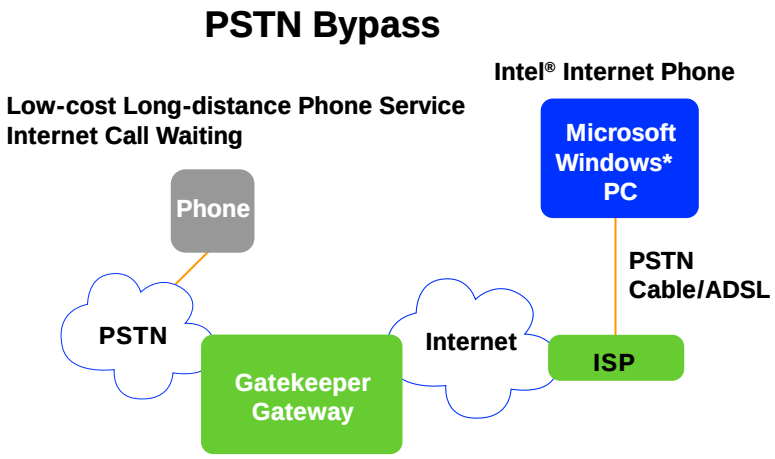

Figure 1

The Intel technology supports open audio, so the end user doesn't need a headset or a stand-alone microphone and can instead use the microphone built into the PC.

e-Commerce Support

Intel's Internet Telephone creates a robust platform to deliver an enhanced e-Commerce experience with richer interaction using both voice and data. The Internet Phone SDK can be embedded into Web pages. The technology takes on the look and feel of the Web page interface. For example, an end user can click a button on a Web page and talk directly to a representative of that company to order a product or obtain more information. As shown in Figure 2, these Web sites act as originators of telephone traffic and keep customers on their sites as they make the phone calls. This allows Web sites to improve the probability of closing transactions, encourage users to spend more time at the site, increase the number of new and returning users, and help drive traffic to different parts of the site. On the call termination side, the Intel SDK is combined with a gatekeeper and gateway to IP telephony-enable call centers to receive calls from the Internet while keeping backward compatibility with existing applications. IP telephony enabled call centers can also use a single network to handle both voice and data and employ a distributed architecture by allowing the call center agents to work at home.

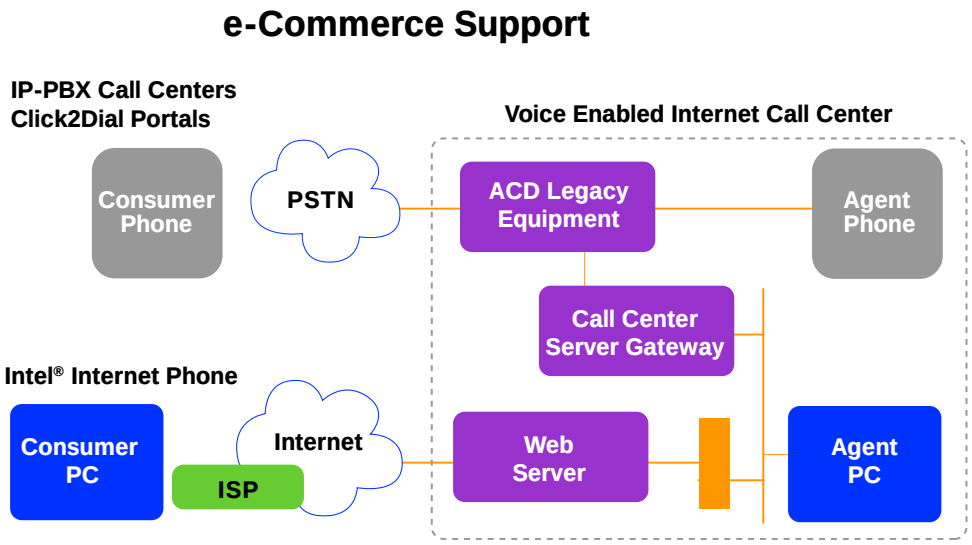

Figure 2

Business Phone

Benefiting from better integration with the PC and better quality calls, business traveler end users will be able to connect to the corporate network via a notebook PC and conveniently gain telephone access as though working at his or her desk. An example is shown in Figure 3. Also, online presence management coupled with a converged voice and data network allows people to be reached where and how they want to.

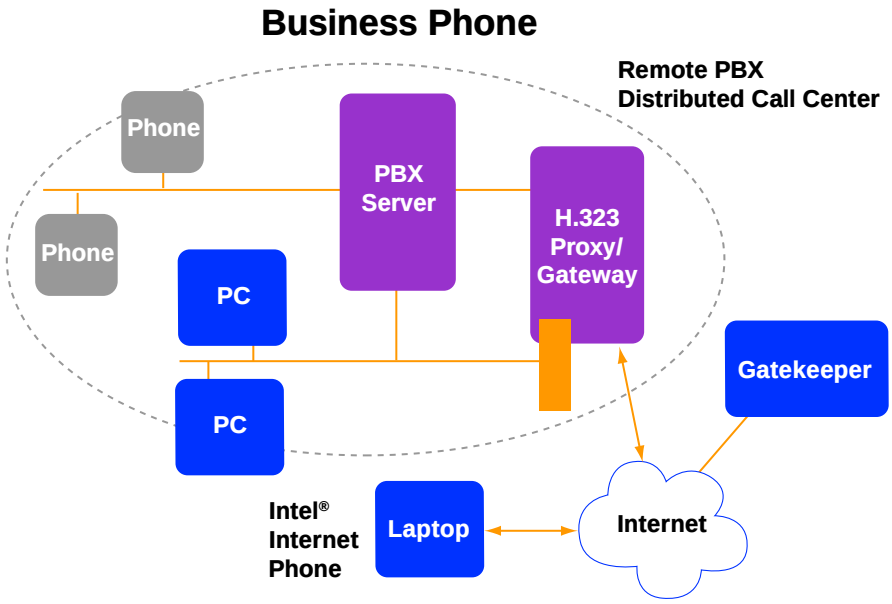

Figure 3

Availability

The Intel Internet Phone SDK and complementary building blocks will be available soon from Dialogic, an Intel Company.

Summary

Intel Internet Phone is a software development kit that provides superior voice quality, includes both voice stream and call control management, interoperability with a broad range of gateways and gatekeepers, flexibility to support proprietary or industry-standard codecs, is light weight for embedding in Web page, allows “easy to create” custom applications. Developers enjoy reduced cost of application customization with easy to program SDK using a simple ActiveX. IP telephony service providers can build out their network based on standard components that are available from multiple vendors. Both can differentiate their solutions by providing superior voice quality with smooth continuous audio.

More Info

For more information on the Intel Internet Phone SDK, send an e-mail to ctcmarketing@dialogic.com.

Author Bios

Max Leite is a marketing manager for Intel Architecture Labs, where he is responsible for business development and strategic directions in the area of Internet telephony.

Previously, Max managed worldwide implementation of Intel’s Internet service provider program. He was also responsible for the successful execution of Intel’s product integrator programs in Latin America.

Before joining Intel, Max helped Advanced Micro Devices establish a presence in the Latin American market. As a co-founder of a network and computer distribution business, he built a corporate infrastructure that allowed negotiations between manufacturer and end user. Max holds a M.B.A. from the University of Texas and a B.S. in Industrial Engineering from the University of Oklahoma.

Ramanan Ganesan manages an Intel Architecture Labs group responsible for development of the Intel Internet Phone SDK. Ramanan's background includes more than 10 years of experience at Intel in designing and developing system software products in the Windows environment. During the course of his career at Intel, Ramanan has been involved in the development of various products including Intel Internet phone, controllerless modems, video phone using Windows WDM technology, security implementation for wireless modems, and PC networking under Multibus II. Ramanan holds a master's degree in Computer Science and Engineering from Indian Institute of Science.

CDSA Now Includes Biometric Authentication, Authorization

Lelia Barlow
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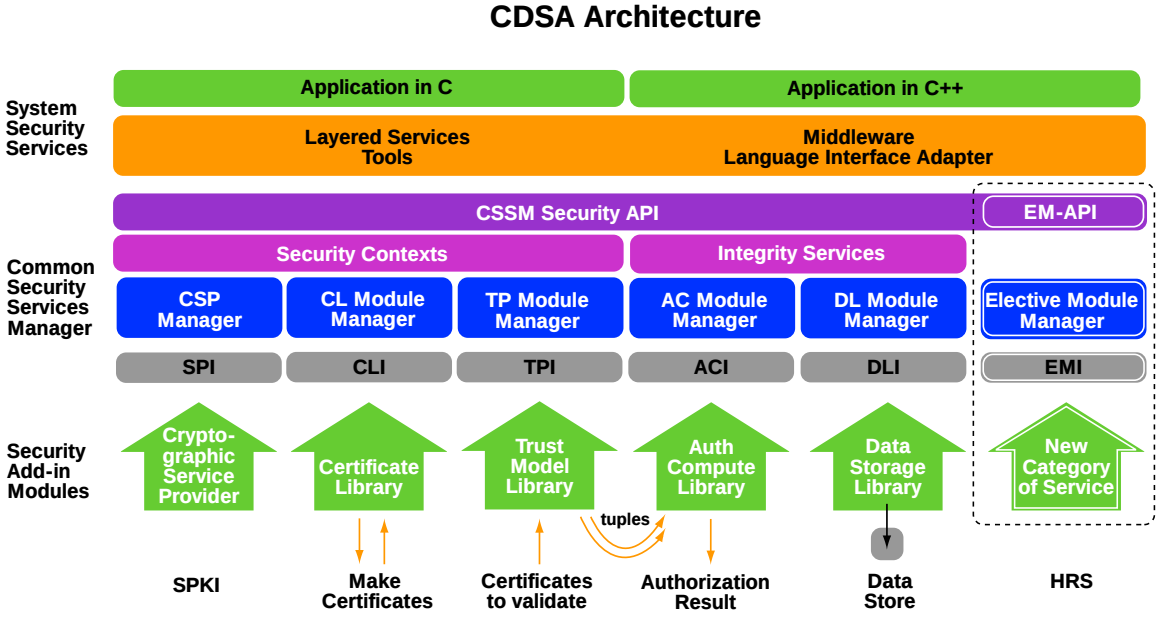
Overview

CDSA (Common Data Security Architecture) provides application developers with an open, cross-platform, extensible, interoperable, and fully exportable security architecture. Created by Intel Architecture Labs a standard an interface to existing and future security technologies, CDSA consists of a unified set of APIs designed to make computer systems more secure for e-commerce, trusted communications, and the consumption of high-value digital content using the Internet. CDSA has been widely adopted by industry, and Intel open sourced the CDSA reference implementation on May 15, 2000.

Now two recently introduced technologies—HRS (Human Recognition Services) and SPKI (Simple Public Key Infrastructure)—offer new security services to application developers. These new modules extend the functionality of CDSA by allowing access to security capabilities such as biometric authentication and authorization certificate processing.

CDSA Architecture

CDSA defines three layers, each building on the more fundamental services of the layer below it. Figure 1 below shows the CDSA architecture in block-diagram form, and shows how HRS and SPKI fit into that architecture. The bottom layer is made up of add-in security modules that start with basic components—cryptographic algorithms, base certificate manipulation facilities, and storage—and build up to secure, digital certificate-based transaction protocols in the uppermost layer (System Security Services). The architecture is designed to be both modular and extensible.



The Common Data Security Architecture (CDSA), including new HRS and SPKI capabilities.

Figure 1

HRS is based on the BioAPI specification for biometric authentication, and is realized in the CDSA framework as an Elective Module Manager (EMM). The EMM allows CDSA to be horizontally extensible to include new categories of security services, and it supports the integrity features of the CDSA stack currently not provided by the BioAPI.

SPKI facilitates the use of multiple certificate formats, including new authorization certificates, to compute authorization. SPKI functionality is included within the CDSA CL, TP, and AC modules. The CL makes certificates. The TP validates certificates, and supplies "tuples," a format that allows different certificate formats to be used together, to the AC. The AC produces the authorization result.

HRS Biometric Authentication

Security experts believe that biometric authentication is a vitally important next step in the creation of security-enhanced applications and solutions. The basic purpose of HRS is to either identify or verify the identity of a person based on some characteristic—typically this is a biometric measurement, though it could also be a password. Access control decisions to such things as smart cards, cryptographic keys, persistent data objects, and Web accounts can be made on the basis of this identification.

Both verification and identification are fully supported by HRS, and they allow the biometric service provider to manage the population database for optimum performance. The API is designed for secure authentication both locally and across a communications channel provided by the application/middleware. Biometric credentials, called biometric identification records or BIRs, make identity theft a practical impossibility; BIRs are both encrypted and signed by the biometric service provider that creates them, and they provide at least the same degree of protection as afforded by digital certificates.

Intel HRS source code is the only biometrics API technology currently available, and biometrics software and hardware vendors are already building products based on HRS.

SPKI Authorization

SPKI—the next step beyond digital certificates—is the simplest way to determine whether a user is authorized to perform an action or use a resource. This mechanism can also allow the authorized user to delegate some of his or her authority to other users, by binding a public key to a set of permissions.

SPKI offers a different kind of certificate format. The original certificate, as designed in 1978, bound names to public keys. SPKI was designed to satisfy a different problem: authorization.

Developers with security needs often must make authorization decisions. If you're running a Web server for medical records and a user asks for a record, you need to decide if the user is authorized to read that record. If you're sending a classified document by e-mail, encrypting the document isn't enough; you need to decide whether the recipient is authorized to read that document. If you are running a Web browser and connecting to an e-commerce page, you need to decide whether the machine at the other end is authorized to handle your payment information (e.g., your credit card number).

When a certificate gives only the name of a keyholder, that's enough information if you know the keyholder and what he or she is authorized to do. SPKI was designed for the more modern case, in which you do not know the keyholder and what he or she is authorized to do.

SPKI certificates bind authorizations directly to public keys. They can also be used to name people you do know and bind authorizations to those names, if you prefer to deal with names for your local community, either way the end result is to communicate an authorization to some code that needs to make a security decision and to allow that decision to be made on the basis of a strongly validated (cryptographically proved) authorization, without requiring that code to know things by some other channel. SPKI certificates simplify the job of making security decisions because they were designed specifically for that purpose, by developers who had that need.

Availability

HRS and SPKI source code for the Windows* 32-bit environment is already publicly available for download from the Intel Architecture Labs area of Intel's Developer site. The 32-bit Linux* version of CDSA will be available by late August, and a 64-bit version, optimized for the Intel® Itanium™ processor, will be available in October 2000.

A demonstration of HRS biometric authentication was presented at the Intel Pavilion and the HRS and SPKI technical sessions at the Intel® Developer Forum Conference, Fall 2000.

Summary

CDSA provides a way to overcome the current challenge of including security services in diverse applications. By establishing an open-source, interoperable, standard infrastructure for accessing security services, CDSA offers access to a variety of security resources, regardless of platform, operating system, or type of security service. CDSA allows application developers to focus on a single API for all security services, instead of a potentially conflicting collection of individual APIs from multiple toolkit vendors. This provides application developers with flexibility, consistency, and portability when implementing security solutions within their products.

More Info

Intel's Developer Site maintains a home page devoted to CDSA technology. From this site, you can download the CDSA source code and technical documentation, join CDSA discussion groups, and locate other technical information such as papers, presentations, and FAQs.

To view the CDSA specification, read "Common Security: CDSA and CSSM, Version 2" in the Publications and Standards area of The Open Group's Web site.

The BioAPI specification (PDF, 323KB), Version 1.0 is available at the organizations site.

To view the SPKI documentation, see IETF RFC2692 (ftp://ftp.isi.edu/in-notes/rfc2692.txt) and IETF RFC2693 (ftp://ftp.isi.edu/in-notes/rfc2693.txt).

For a previous CDSA article by the author, see "CDSA Brings Security into the Open" in the Intel Developer Update Magazine archives, May 2000 issue of IDU.

Author Bio

Lelia Barlow joined Intel in 1997. She works in Distributed Services Architecture Lab (DSAL), part of Intel Architecture Labs, as applications engineer for the Common Data Security Architecture (CDSA) standard. Previously, she worked in the Desktop Motherboard Engineering Group in Intel OEM Platform Solutions Division (OPSD).

Lelia has also been an instructor with Saturday Academy, a community-based pre-college department of the Oregon Graduate Institute of Science and Technology. Her program, "GEEK CHIC," was created to interest middle- and high-school girls in electrical engineering. She holds a B.S.E.E. from Oregon State University.

Intel Press Publishes IA-64 Book

Stuart Goldstein
Intel Press
Intel Architecture Group
Intel Corporation

Overview

At the Intel® Developer Forum Conference, Spring 1999, Intel introduced Intel University Press. Dedicated to providing developers with the highest quality technical publications, its first book was an instant success. *USB Design by Example*, written by John Hyde, became a runaway technical bestseller with an immediate second printing.

To ensure its publishing goals continued to meet the needs of the developer community, Intel University Press sought industry input to guide its growth. As a result of developers' feedback, the term "University" was dropped from its name, making it simply Intel Press. And the Press focused its attention on a topic of intense interest, the 64-bit architecture for the next-generation processor code-named Merced.

At the Intel Developer Conference, Fall 2000, Intel Press announced availability of its latest book. *IA-64 Architecture for Software Developers* by Walt Triebel provides an in-depth look at the architecture that's the foundation of the new 64-bit Intel® Itanium™ processor, formerly known as Merced. The book uses language that makes the technology easy to understand for novices and experts alike.

A Look Inside IA-64

New architectures are rare, and *IA-64 Architecture for Software Developers* by Walt Triebel offers a firsthand look at a design that changes the fundamental "width" of the processor, employing speculation and predication to make explicit parallelism useful.

With an insider's perspective, the foreword by James Reinders tells how this architecture, known as EPIC—Explicitly Parallel Instruction Computing—was developed cooperatively by Intel and Hewlett-Packard. He goes on to show how this innovative technology helps systems run faster and do more at once.

The product of more collaborative engineering than any prior microprocessor architecture, EPIC combines instructions to operate in parallel, using from one instruction to as many instructions as desired. By writing programs using parallel semantics, EPIC makes it possible to build machines with different levels of parallelism, execute the same programs, and get the same results.

EPIC brings a number of new elements to microprocessor technology, but the most significant are instruction-level parallelism, speculation, predication, and a large register file. Each of these makes a computer run faster by doing more things at once. EPIC makes important calculations before they are needed so that when a program calls for information, the answer is already available.

An excerpt from the book, Chapter One, "Introduction," is now online at the Intel Press Web site.

Books Developers Need

To make it easier for developers to acquire important new books, Intel Press now offers them through Shop Intel, the company's online shopping site for books, software, PC products, logo apparel, and gifts.

More Intel-authored, developer-oriented books from Intel Press will be made available throughout 2000. For updates, visit the Intel Press site

Summary

Even as leading vendors were demonstrating readiness for the 64-bit Intel Itanium processor, Intel Press announced *IA-64 Architecture for Software Developers* by Walt Triebel. The latest publication from Intel Press, the book gives an insider's perspective of the new architecture and its development.

Intel is committed to providing developers with the tools they need to be more effective and competitive in this rapidly changing industry. Intel demonstrates this commitment in part through Intel Press and the books it offers through Shop Intel.

More Info

To read the first chapter from *IA-64 Architecture for Software Developers* now, visit the Intel Press Web site.

IA-64 Architecture for Software Developers and USB Design by Example can both be ordered online from the Books & Software section of Shop Intel.

More information about Intel Press is available from its Web site.

Intel Press is a joint publishing agreement between Intel and John Wiley & Sons, Inc. Information on John Wiley & Sons, Inc. Publishing is available on the company's Web site.

Author Bio

Stuart Goldstein is a content manager with Intel Press, part of the Intel Architecture Group. During his three years with Intel, Stuart has worked on integration of PC videophone products and platform compliance testing tools.
Stuart brings with him over 16 years' experience in software development and technology management, in both software and semiconductor design. He has an extensive background in PC audio and interactive multimedia. Stuart holds a B.S. in Computer Science from the University of Kansas.

Get on the Fabric with InfiniBand* Architecture

Jim Pappas
Director of Initiative Marketing
Fabric Component Division
Intel Corporation

Overview

The rapidly changing Internet environment is placing new demands on data centers. Their need to transition to greater flexibility and scalability is driving a renaissance in data center design.

InfiniBand* Architecture provides a platform where ever-increasing processor power converges with a breakthrough in I/O capability. A standards-based architecture developed by a core group of industry leaders, InfiniBand has progressed beyond the concept stage. Today companies like Intel are designing prototypes that closely resemble working systems.

When the InfiniBand Trade Association was introduced in 1999, industry reaction was strong and favorable. The Trade Association has grown from seven founding members to over 170 representatives from every segment of the industry. Final InfiniBand specifications will be available soon, and many companies are already announcing InfiniBand product development. While this architecture promises to be one of the most innovative technologies the industry has seen, the industry is still largely unaware of what the architecture can do.

Moving to Channel-based I/O

Traditionally, server performance has focused on speed and feed. Servers dependent on a shared bus I/O architecture deliver a fixed level of bandwidth that is, in turn, shared among the devices connected to the bus. As connections are added, I/O contentions increase and performance per connection is diminished. This lack of flexibility and scalability is precisely why InfiniBand is such an important new technology.

InfiniBand Architecture provides a standards-based I/O platform that creates a new foundation for greater system scalability, reliability, and performance. At its core, InfiniBand is a new way of attaching servers to each other and to remote storage subsystems and networks.

The shift to channel-based I/O delivers a new perspective on system performance. The ESCON channels that connect many of today's mainframe systems deliver 17-MB/second link performance and are considered to be among the highest performing I/O systems. With InfiniBand architecture, systems that depend on shared bus I/O today can deliver channel-based I/O connectivity operating at more than 15 times that of ESCON systems.

Benefits of the Architecture

InfiniBand Architecture separates the I/O subsystem from the CPU/memory complex by replacing the shared bus with a high-speed serial switched fabric. All nodes attach to the fabric through channel adapters. Host servers attach using components called Host Channel Adapters (HCA), while target devices attach with components called Target Channel Adapters (TCA). One or more switches can connect any number of hosts and target devices to provide a highly reliable fabric. With 2.5-Gbits/second signaling, InfiniBand Architecture promises to achieve the fastest serial interconnect data rate available in the industry.

By offering the flexibility to detach from the CPU/memory complex, InfiniBand Architecture enables a new level of server density. Sharing peripherals across multiple servers reduces the physical space required to connect large volumes of servers with multiple storage and communications devices. With InfiniBand, data centers can be more compact.

Data centers can also be more reliable, thanks to the InfiniBand Architecture's multiple levels of redundancy. Because nodes are connected to multiple links, InfiniBand systems continue to perform even if one link fails due to aggregation of links. Completely redundant fabrics can be configured for the highest level of reliability, and redundant fabrics continue to perform even if an entire fabric fails.

Key Features

The InfiniBand Architecture offers a number of unique features to support these capabilities.

- I/O can be deployed in balance with increased processor performance through independent scalability of server, I/O, and fabric capacity.
- Thermal and packaging density issues associated with physical distance restrictions between devices are greatly reduced.
- Many of the traditional bus architecture-based barriers that limit connectivity are eliminated.
- New form factors will be easier to add, remove, or upgrade than today's shared bus I/O cards.
- Load-and-store-based communications are moved from a shared local bus I/O to a more reliable message passing approach.
- The I/O fabric is designed to scale without encountering the latencies that some shared bus I/O architectures experience as workload increases.
- Thinner server chassis allow a higher number of chassis in a stack, enabling higher processor power.

2001 Roadmaps

With standards-based fabric I/O fast becoming reality, now is the time for hardware, system, and application vendors to develop products that will take advantage of InfiniBand Architecture. The InfiniBand Trade Association is finalizing InfiniBand specifications for publication in October 2000.

In the meantime, Intel will continue to lead the industry in development of InfiniBand fabrics through a number of activities.

- The recently announced industry port logic and product development kit programs will deliver the tools needed for product development to the industry.
- Delivery of Host Channel Adapters (HCA), Target Channel Adapters (TCA), and switch silicon are planned for each primary component of an InfiniBand fabric.
- Intel's InfiniBand World Tour, a seminar series led by Intel InfiniBand architecture experts, will extend the knowledge base to wider audiences around the globe and encourage developers to create products that deliver value to InfiniBand products.

At the same time, Intel will continue working with individual industry members to further validate InfiniBand products and demonstrate this validation at Intel® Developer Forum Conferences and other industry events.

Summary

The InfiniBand Architecture promises to be one of the most significant technologies in development today, and industry leaders believe it has the potential to transform data center I/O and change the way data centers are developed in the future. The top corporations in the industry are working together to define and support the InfiniBand Architecture. Now is the time to develop products based on this innovative architecture.

More Info

For more information on the InfiniBand initiative, visit the What is InfiniBand Architecture? page of Intel's Developer Site.

Information on the InfiniBand World Tour is located in the InfiniBand Architecture area of Intel's Developer Site.

More information on InfiniBand Trade Association events and activities is available from the organization's Web site.

Author Bio

As director of Initiative Marketing in Intel's Fabric Component Division, Enterprise Server Group, Jim Pappas is responsible for working with the industry on the development of products that comply with the InfiniBand Architecture and for the promotion of the standard through the InfiniBand Trade Association.

Formerly the director of Technology Initiatives in Intel's Desktop Products Group, Jim successfully led technologies such as AGP, DVD, IEEE 1394, Instantly Available PC, USB, and other advanced technologies for the Desktop PC.

Jim has 18 years' experience in the computer industry. He has served on the board of directors for a number of technology initiatives, most notably the PCI Special Interest Group as a founding member, and the USB Implementers Forum as the founding chairperson.

Jim holds eight U.S. patents in the areas of computer graphics and microprocessor technologies, and has spoken at major industry events including the Intel Developer Forum (IDF) Conference, WinHEC, Comdex, PC Strategy, Microprocessor Forum, PBX 2000, Consumer Electronics Show, PCI Plus, and the Applied Computing Conference. His B.S.E.E. is from the University of Massachusetts in Amherst.

Solving BIOS Boot Issues with EFI

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Overview

Developers have consistently had to deal with three main issues when thinking about making changes to BIOS: booting an operating system, loading and executing option ROMs, and testing platforms on a manufacturing line. In the past, these issues have been addressed by relying on BIOS interfaces and assuming that certain hardware components are present in the platform. This article describes how EFI solves boot issues with BIOS.

Over time, developers have had to continually extend the functionality of BIOS. However, BIOS presents significant problems for today's computers. For example, when two developers use the same method for extending functionality, collisions can occur. In addition, BIOS is typically implemented in assembly language. What's more, BIOS doesn't have a specification—there is no single document or source that details BIOS interfaces. Without a specification to test against, it is difficult to test a system for compatibility. Finally, the operating systems (OS) not only have to be tied to BIOS, but they must be directly tied to the hardware platforms. This means that OS can only be booted by using BIOS calls, and only if the OS has intimate knowledge about the platform hardware.

Trying to build a legacy-free platform is extremely difficult unless you can decouple or abstract the hardware platform from the OS. Intel has been working with many industry partners to come up with a solution that allows the BIOS interfaces to be replaced. The Extensible Firmware Interface, or EFI, is just that solution.

The EFI Concept

EFI is an OS- and platform-independent boot and preboot interface. It lies between the OS and platform firmware, and addresses many of the limitations of BIOS. Specifically, it allows the OS to boot without having details about the underlying hardware and firmware.

EFI supports a myriad of boot devices: hard disks, removable media devices (CD-ROM, DVD-ROM, floppy drives, zip drives, etc.), and network devices. It also contains an extensibility mechanism that will allow future media devices to be supported. The interface provides run-time services, boot services, console services (such as local-head and remote-head support options), and a collection of GUID-based (Guaranteed Unique Identifier-based) protocol services that are used to access boot devices.

EFI is not restricted by the 640K memory limit that BIOS and DOS currently have. Instead, EFI uses a flat memory model that is limited only by the amount of memory present in a system. It is also implemented in C, not assembly language, so EFI is easier to maintain over a longer period of time and easier to port to new platforms.

With EFI, the OS no longer needs to know which chips are on the motherboard, and no longer needs to know the firmware requirements of individual boot devices. Instead, EFI hides platform and firmware details from the OS. In doing so, EFI presents a consistent interface to the OS, regardless of the CPU, memory configuration, firmware implementation, and so on.

EFI simplifies things from the OS developers' points of view. This lets developers concentrate on innovative OS features instead of methods for making the OS talk to the hardware or firmware. This also means that legacy support is no longer an issue. With EFI, OS developers can drop BIOS constructs, including the compatibility region, run-time INT services, BIOS data area, and the extended BIOS data area.

In short, EFI provides developers with an alternative, flexible, maintainable, extensible, and platform- and OS-independent boot method for embedded systems, desktops, workstations, and servers. EFI meets one of the main goals of providing an interface solution that can handle OS and platform developments for the next 20 years.

What Happens at Boot

EFI gives developers a built-in mechanism for abstracting the OS from the hardware. When the OS boots, the OS needs to know basic details about the hardware and firmware, such as how to read a file from disk, how to interpret a keystroke, how to send messages to the display, and so on. EFI handles these tasks through boot and run-time service, protocol interfaces, and data tables that contain platform-related information to the OS and its loader. The boot services include features like these:

- Events and notifications
- An elegant recovery mechanism through a watchdog timer
- Memory allocation
- Handle management and location
- The ability to load and execute EFI drivers, EFI applications, and OS loaders for EFI-compliant operating systems

The services provided by EFI eliminate the need for the OS to make BIOS calls and the need to contact hardware directly. They allow the OS to boot without having any direct knowledge of the hardware platform or about the internals of the firmware BIOS. Even if BIOS is available, an EFI-aware OS uses only EFI to get information from the boot devices (such as a keyboard). When both the OS and hardware platform are EFI-compatible, EFI will fully initialize the system using only EFI drivers.

Current EFI Use

EFI is already being used in industry. The interface is in every IA-64 platform being designed today—it is the only method allowed for booting IA-64 operating systems. It provides OS vendors with a cleaner, more effective, more easily maintained interface that can handle future developments in both OS and hardware platforms.

AMI and Phoenix are currently implementing EFI, and many original-equipment manufacturer (OEM) platforms also already support EFI. In addition, a variety of operating system vendors are developing IA-64 EFI-compatible operating systems, including IBM/Monterey*, Linux*, Novell*, SCO*, Solaris*, HP/UX*, and Windows NT*.

EFI is not limited to IA-64. It is also being used in some of today's IA-32 systems. Manufacturing and test infrastructures are also already moving to EFI.

Why Convert Now?

Operating-system vendors (OSV) should immediately start converting their operating systems to use EFI. The development of future OS will be even more cost-effective and maintainable under EFI than under BIOS, because EFI is platform-independent. Future EFI-compatible OS will not need to be ported from one platform to the next.

Platform vendors should also begin making the transition to EFI by implementing EFI-compliant firmware. Once the platforms and operating systems are EFI-compliant, platform vendors will be able to make innovative improvements to hardware designs without worrying about issues of OS compatibility.

The EFI specification tells OS developers how to change the OS to work with an EFI-compatible platform. The EFI specification also tells hardware platform developers and firmware developers how to build EFI-compatibility into the platform and firmware implementation. The latest EFI specification is available for free download from Intel’s Developer Site.

A future version of the EFI Specification (EFI 1.1) will provide details on how to implement EFI-compliant option ROMs. Independent Hardware Vendors (IHVs) will need this information to build add-in cards for EFI-compliant platforms.

Add-in Cards

Add-in cards often include a ROM that contains the software required to initialize and access a device. This software currently makes use of BIOS calls, and assumes a PC/AT-like motherboard is present. Add-in card vendors also need to begin converting their products to be EFI-compatible.

The benefits to add-in card developers are similar to those of the OS and hardware-platform vendors. The amount of work required to upgrade, port, or create new EFI-compatible add-in cards will be less than the effort required to make BIOS-compatible cards. In addition, the EFI-compatible add-in cards will be able to work on a wider variety of platforms.

Sample Implementation and Toolkit

Intel has made a sample implementation of EFI freely available to developers. This is a portable implementation of the interfaces of the EFI Specification. The implementation is designed for integration with an existing underlying BIOS or firmware implementation, and this code will work equally well on an IA-32 or IA-64 based system.

The EFI Application Toolkit is a set of tools that support rapid porting and development of EFI applications. These tools promote a uniform preboot environment on IA-32 and IA-64 platforms. The components are available as reference source code, which is free to developers. The toolkit includes a Standard C library with wide character and local support, the EFI Shell and utilities, a TCP/IP networking stack and networking utilities, and so on.

Transition Period

Initially, EFI can be layered on BIOS. This allows industry a transition period to move both operating systems and hardware platforms away from BIOS. However, if the OS supports EFI, the OS may use the more effective and efficient EFI services in place of BIOS services.

Eventually, EFI will likely replace BIOS interfaces completely. This will free OS developers from hardware considerations, and will release hardware/firmware developers from having to design platforms that contain hardware that is assumed to be present by the OS.

Summary

EFI provides a platform-independent boot and preboot interface between an operating system and the platform hardware. In replacing BIOS, EFI allows for continuous improvement and innovation in both hardware platforms and OS. At the same time, EFI maintains basic compatibility by providing the necessary interface for developers.

EFI has significant advantages over BIOS. It:

- Decouples the hardware platform from the OS
- Is useful to OSV because they can write their loaders for the standardized EFI instead of for architecture-specific platforms
- Is useful to platform designers because they can create new, exciting, innovative, or even radically different hardware designs without having to worry about compatibility with existing or future OS
- Is implemented in C, and so is easier to maintain over long periods of time
- Has a detailed specification that makes it easier to test for compliance
- Is the only way to boot IA-64 operating systems

EFI solves current problems with BIOS and presents a standard environment for the booting OS and for running preboot applications. This is a solution that not only can be implemented now, but that will stand up to the next 20 years of OS and hardware-platform development.

More Info

Refer to Intel's EFI Web Site for:

- General EFI Information
- EFI Specification
- Presentations on EFI and the EFI Application Toolkit
- Full source code to the EFI Sample Implementation
- Full source code to the EFI Application Toolkit

Also refer to Microsoft's Web Site for:

- FAT32 File System Specifications
- Portable Executable and Common Object File Format (PE/COFF) Specifications

Author Bio

Michael Kinney joined Intel in early 1999 as a staff engineer in the Microcomputer Software Labs. He is one of the architects of the EFI Specification and has worked extensively on the EFI Sample Implementation. Prior to joining Intel, Mike was a principle software engineer at DeskStation Technology*, where he designed MIPS and ALPHA based workstations for Windows NT and Linux. He received his Bachelor's degree in Computer Engineering and his Masters degree in Electrical Engineering from the University of Kansas.

Servers

ROMB: The Rest of the Story

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Overview

The adoption of Internet-based e-Commerce and e-Business models has made data the most important strategic asset for businesses of every size. As data protection and data availability become top-of-mind issues with business users, RAID (redundant array of independent disks) subsystems are increasingly being added to entry-level and midrange servers. The emergence of affordably priced RAID controller cards based on Intel® I/O processors has helped stimulate the attach rate hardware-based RAID. RAID-on motherboard (ROMB) implementations are now driving costs down even further.

Implementing a hardware-based RAID solution directly on the server board provides decisive advantages for server OEMs as well as their IT customers. Intel's ROMB solutions deliver a combination of storage performance, data protection, availability, server reliability, and ease-of-use. Perhaps the best news for server OEMs, system integrators, and business users is that ROMB makes all of these benefits deliverable at the lowest possible cost. This explains why ROMB is currently shipping in a wide range of server models offered by leading vendors.

The use of I/O building blocks, including Intel I/O processors and Intel® Integrated RAID software, will continue to enable server OEMs to implement ROMB as a key value-added feature in servers spanning all price points, including the emerging category of Network Attached Storage (NAS) server appliances. To compete in this space, OEMs should be prepared to offer RAID capability to their customers, and ROMB will enable them to implement RAID at the lowest possible cost.

RAID Features

While they are available on adapter cards, Ethernet and SCSI I/O technologies have found their way onto the motherboard in implementations that reduce bill-of-materials costs for OEMs, while providing value-added features for server users. Intel Integrated RAID building blocks make it possible to achieve the same advantages with hardware-based RAID. Business users looking for optimal network storage performance, data protection, data availability, network reliability, and ease-of-use can find it all integrated into their next server. Here are some of the ways ROMB can enhance server value:

- Performance—Intel I/O processors combine integrated internal buses, data flow architecture, and support for 64-bit/66-MHz PCI to enhance throughput in single- and dual-channel SCSI RAID applications. By offloading RAID interrupts from the server's host CPU, RAID I/O processors help optimize server performance. Intel makes a variety of I/O processors available to satisfy multiple price and performance requirements.

- Data protection—Intel® RAID controllers and Integrated RAID software support RAID levels 0, 1, 5, and 10, enabling users to select the optimal balance of storage performance and data protection. RAID 5 includes data striping across multiple disks, with parity calculations to enable data recovery in the event of a disk failure. The integrated XOR capability available in Intel I/O processors performs RAID 5 parity calculations, freeing the host processor for application processing.

- Data availability—Intel Integrated RAID software enables online capacity expansion without the need to reboot the server. The software also supports up to 15 drives per RAID channel.

- Reliability—Intel RAID building blocks are validated with Intel® server boards, major operating systems, and new drive technologies to enhance server reliability and reduce support costs. In the event of a drive failure, a "hot spare" can be brought online or a disk can be replaced without disrupting the network.

- Ease of use—Intel Integrated RAID software includes a browser-based RAID management tool that simplifies RAID configuration. This operating system-independent software utility suite supports remote configuration and includes a BIOS configuration utility that creates a RAID array for operating system installation.

ROMB for NAS

Dedicated Network Attached Storage (NAS) appliances are emerging as a simple and affordable mass storage solution for high-availability networks. Because a NAS device is a dedicated appliance used only for storage, it may be a cost-effective alternative to adding a PC-based file server in many network installations. NAS devices typically advertise plug-and-play flexibility in a transportable form factor, and they enable both Windows NT* and UNIX* clients to store files on the same network storage device. By providing these flexible storage options, NAS appliances enable administrators to easily scale their network's storage capacity, without disrupting availability.

Of course, data protection is just as important on a NAS appliance as it is on any other server, and this requirement makes ROMB the ideal solution. With its high level of integration, ROMB is an appropriate solution for "thin" server NAS devices, including rack-mount implementations, that must also support advanced RAID levels in larger disk arrays.

Summary

As e-Business and e-Commerce applications continue to proliferate in all business segments, data availability and server reliability are becoming critical issues. This requirement is making RAID technology a key value-added feature in entry-level and midrange servers. The availability of affordably priced RAID adapter cards has helped support a growing attach rate in this server segment. The next logical step is ROMB, which delivers the data protection and performance of a hardware-based RAID solution at a significantly reduced cost compared to a PCI-based add-in card implementation. In addition to cost advantages, placing the RAID controller on the server board frees a PCI slot for other applications.

ROMB is a perfect solution for Network Attached Storage (NAS) appliances that must support RAID levels 5 and above in a small form factor enclosure where a PCI card might be impractical. The combination of ROMB with a Web-based management software application, such as Intel Integrated RAID software, simplifies RAID configuration and permits easy online array roaming and expansion without taking the server offline. For the growing number of users who are looking for improved network storage performance, data protection, data availability, network reliability, and ease-of-use, ROMB is the next "must-have" feature in servers.

More Info

For additional information on RAID-on motherboard and Intel Integrated RAID building blocks, visit Intel's I/O Building Block Web site.

Author Bio

Logan Henriquez is I/O product marketing manager for Intel's I/O Products Division. Logan's experience includes several years leading the Compaq server storage division product marketing team, which launched Compaq Computer Corporation's first Fibre Channel product, created its entry-level RAID product line, and grew the division into the leading storage supplier. Logan also held positions in software development and planning at Intuit, Inc. and American Express International. He holds a B.S.I.E. from Stanford University and an M.B.A. from the University of Chicago.

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