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U.S. DEPARTMENT OF COMMERCE/National Bureau of Standards

Standard Reference Materials:

Preparation and Certification of SRM's for Calibration of Spreading Resistance Probes

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James R. Ehrstein

Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Gaithersburg, MD 20899



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PREPARATION AND CERTIFICATION OF SRM'S FOR CALIBRATION OF SPREADING RESISTANCE PROBES

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This Special Publication describes the material selection, characterization, data analysis, and measurement process control procedures for four types of Standard Reference Materials (SRMs), available from the National Bureau of Standards, for calibration of spreading resistance measurements on semiconductor silicon. Each of the four comprises a single combination of silicon conductivity-type and crystallographic orientation and contains 16 rectangular silicon chips which are certified for resistivity value based on four-probe resistivity measurements on the slices from which they were cut. The resistivity values of the chips in each set range from about 0.001 $\Omega\cdot\text{cm}$ to about 100 $\Omega\cdot\text{cm}$. The uncertainty of the certified resistivity, as it applies to any individual chip, depends both on the uniformity of the starting slice and on the inherent measurement process uncertainty. The procedure for determining this uncertainty, which is specifically evaluated and tabulated on the certificate for each SRM set, is described.

Key words: resistivity; silicon; spreading resistance measurements; standard reference materials.

1. INTRODUCTION

This Special Publication describes the material selection, characterization, data analysis, and measurement process control procedures for four Standard Reference Materials (SRMs) for spreading resistance measurements on semiconductor silicon.

The four Standard Reference Materials are SRM 2526 for (111) p-type silicon, SRM 2527 for (111) n-type silicon, SRM 2528 for (100) p-type silicon, and SRM 2529 for (100) n-type silicon. These SRMs are sets of single crystal silicon specimens. Each set contains specimens with resistivity values (approximately three per decade) from about 0.001 Ω -cm, to about 100 Ω -cm, with which to generate a spreading resistance-to-resistivity calibration for a spreading resistance probe. The intended application for the calibrations obtained with these SRMs is depth profiling of most common silicon integrated-circuit and discrete-device structures using ASTM Method F 672 [1].* Because the electrical response of a spreading resistance probe is a function of both the conductivity-type and the crystallographic orientation of the silicon being measured, the calibration set (or sets) must be chosen by the user to match the test specimens being profiled or otherwise measured. The silicon specimens in each of these SRM sets are provided in the form of rectangular chips for convenience of use. They are to be polished, lapped, or otherwise prepared in a manner, and with a frequency, established by the user prior to use for calibrating a spreading resistance probe.

The certificate provided with each set gives three certified values for each specimen chip in that set: Resistivity, Range (of measured values), and Uncertainty (of certified resistivity value). The definition of these terms is given in section 4.5 of this report. The values reported for each specimen chip were measured on the slice from which that chip was cut. The certificate also gives additional, non-certified information for each chip: dopant, crystal growth process, an estimate of spatial fine-scale resistivity variation, and, where calculable, an estimate of the macroscopic resistivity variation for the chip.

2. MATERIAL PREPARATION, PRELIMINARY CHARACTERIZATION, AND INGOT SELECTION

Sections of single-crystal silicon ingots 2 to 3 in. in diameter were purchased for these SRMs from a number of commercial silicon suppliers. Below resistivities of about 20 Ω -cm, the crystals were almost exclusively Czochralski (Cz) grown. Above this value, float-zone grown (FZ) p-type crystals and neutron transmutation doped (NTD) n-type crystals were used. The p-type crystals were exclusively boron-doped. Although some arsenic- and antimony-doped ingots were evaluated, all n-type ingots finally selected were phosphorus-doped because of their superior uniformity of resistivity. (Phosphorus-doped crystals will be used exclusively for future n-type sets unless present material supply at a given resistivity is exhausted and replacement crystals are only available with arsenic or antimony doping.)

All ingot sections were verified for crystallographic orientation using either x-ray Laue diffraction or preferential crystallographic etch tests. The conductivity type of each was verified using the hot-probe procedure of ASTM Method F 42 [2]. All ingots were tested for center-point resistivity at both ends by the four-probe technique using ASTM Method F 43 [3]. This procedure was used to allow a tentative selection of those ingots, and the preferred end of each of those ingots, which would give the desired distribution of resistivity values in each of the four SRMs. Each ingot was then screened for resistivity uniformity by measuring the radial resistivity variation on the selected end of the ingot using four-probe measurements and the basic procedures of ASTM Method F 81 [4]. A number of ingots were dropped from consideration at this stage due to excessive radial variation of resistivity.†

Those ingots accepted for use were sliced and the slices lapped on both sides to meet the surface preparation procedure of ASTM Method F 84 [6] and to optimize the thickness uniformity of the slices. Nominal slice thickness after lapping was 625 μ m.

* Individual copies of all ASTM Methods cited in this report are available for a nominal fee from American Society for Testing and Materials, 1916 Race St., Philadelphia, PA 19103. They are available collectively in section 10.05 of the Annual Book of ASTM Standards, available from the same source.

† Macroscopic radial variation of resistivity, as well as fine-scale variation (striations), is a consequence of fluctuations in dopant incorporation during crystal growth. The magnitude and spatial pattern of these fluctuations depend on the segregation coefficient of the dopant as well as thermal variations at the growth interface of the evolving crystal. While it may be possible to minimize these dopant fluctuations (resistivity variations) by optimal control of crystal growth conditions, they cannot be eliminated [5].

Screening for spatial fine-scale resistivity variations was then performed. One slice from each ingot was polished with 0.5- μm grit diamond compound and spreading resistance measurements were made along one diameter to evaluate the fine-scale variations of resistivity (resistivity striations) [7]. A step increment of 100 μm was used for the measurements. Occasionally, auxiliary scans were made at step increments as small as 10 μm , or were made on another diameter. The outermost 2 mm at each end of the diameter were excluded from the scans. It was not known initially what level of fine-scale resistivity uniformity would be obtainable from commercial silicon crystals. Target values for maximum allowable fine-scale resistivity variation were set at 10% for the p-type material and 20% for the n-type material. When measurements exceeded these target values, replacement ingots were sought. In cases where two or more ingots were available with similar resistivity values, the fine-scale resistivity variation was used in conjunction with the coarse-scale resistivity variation, as measured by four probe, to select the best ingot at that resistivity level.

Ingot were selected which were comfortably below the target striation values for all but a few resistivity levels, for which the target was just met, and the highest resistivity level in the (100) p-type SRM, for which the fine-scale variation was found to be about 14%. A replacement ingot for this level was not obtainable.

For all ingots used in these SRMs, the estimate of maximum fine-scale resistivity variation obtained from the spreading-resistance measurements is reported on each SRM certificate. For the test slices from some ingots, resistivity variations of the reported magnitude occurred at only a few isolated places along the diameter tested; for other test slices, such resistivity variations were pervasive along the diameter. Because fine-scale resistivity variations generally change from slice to slice for a given ingot, the values reported on the certificate, measured on a single slice from each ingot, must be considered as representative only; they are not certified. A summary of these fine-scale resistivity estimates for the ingots used for the four spreading resistance SRMs as they are currently being issued is given in table 1.

All slices intended for use were qualified for uniformity of thickness by scanning along three diameters using a contactless thickness gauge. One of the diameters scanned was oriented parallel to the slice-orientation flat and the other two were oriented at ± 60 deg with respect to the first diameter. The scan along each diameter included all points except the outermost 6 mm; see figure 1. For slice acceptance, the measured thickness was required to be constant to 1%, or better; typically, the values for a given slice were constant to better than 0.4%.

3. CERTIFICATION MEASUREMENTS

3.1 Slice Thickness Measurements

The thickness value actually used to compute slice resistivity values from the electrical measurements was the average of five thickness values measured with an electronic contacting micrometer. These five values were taken at the slice center and at four points located at half-radii along each of two perpendicular diameters. The accuracy of these individual measurements, traceable to precision gauge blocks, was better than ± 1 μm . Figure 1 shows a schematic diagram of the thickness measurement locations used for the preliminary uniformity qualification and those used for calculation of the resistivity values.

3.2 The Resistivity Measurement Test Station

The resistivity measurement station employed for certification of all slices used for these SRMs consisted of 1) a precision six-decade dc constant-current supply with regulated current capability from 10^{-8} to 10^{-1} A; 2) a 6-1/2 digit DVM with resolution to 0.1 μV ; 3) a series of standard resistors, with values from 0.01 to 10,000 Ω , each known to better than 10 parts per million, for monitoring the dc current value; 4) a manual stage capable of radial and azimuthal (r, θ) motion sufficient to measure all points on any diameter of a slice up to 4-in. diameter; 5) a copper-block heat sink with an imbedded thermistor calibrated to 0.01°C against an NBS-traceable glass-bulb thermometer and with a centering fixture capable of centering circular slices (up to 3-in. diameter) on the stage to within 0.0015 in.; and 6) a four-point probe with a spacing of 1.59 mm (0.0625 in.) as required by ASTM F 81 [4]. Since the measurement procedure relies on the ratio of voltage measurements (between the silicon slice and the standard resistors), measurement accuracy depends primarily on DVM linearity rather than on DVM accuracy. Tests of this linearity, made by comparing different pairs of standard resistors, show it to run from about 0.0012% when all voltages are 10 mV or above to about 0.1% when the voltages can only be measured to about 3-1/2 digits, as is the case for slices below about 0.001 $\Omega\cdot\text{cm}$.

3.3 Sampling Plan for Resistivity Measurements

It was expected from the nature of silicon crystal growth, and supported by previous experience, that the resistivity variation for most of the slices would be primarily radially dependent with a high degree

SRM 2526 (111) P-type			SRM 2528 (100) P-type			SRM 2529 (100) N-type		
CODE1	RESISTIVITY2 ($\Omega \cdot \text{cm}$)	STRIATION3	CODE1	RESISTIVITY2 ($\Omega \cdot \text{cm}$)	STRIATION3	CODE1	RESISTIVITY2 ($\Omega \cdot \text{cm}$)	STRIATION3
IP01	0.0006	5%	IN01	0.0008	4%	OP01	0.0006	4%
IP02	0.0011	6%	IN02	0.0024	10%	OP02	0.0014	3%
IP03	0.0018	5%	IN03	0.0050	5%	OP03	0.0044	3%
IP04	0.0056	6%	IN04	0.0080	4%	OP04	0.0066	4%
IP05	0.015	5%	IN05	0.027	7%	OP05	0.014	6%
IP06	0.024	6%	IN06	0.055	5%	OP06	0.026	8%
IP07	0.060	8%	IN07	0.15	8%	OP07	0.057	6%
IP08	0.13	8%	IN08	0.30	10%	OP08	0.16	6%
IP09	0.33	5%	IN09	0.53	10%	OP09	0.32	6%
IP10	0.75	6%	IN10	1.4	10%	OP10	0.63	8%
IP11	2.6	6%	IN11	2.8	12%	OP11	1.3	10%
IP12	4.8	6%	IN12	6.5	14%	OP12	3.8	5%
IP13	11.	5%	IN13	11.	14%	OP13	7.9	10%
IP14	22.	6%	IN14	27.	5%	OP14	20.	6%
IP15	70.	6%	IN15	75.	5%	OP15	28.	6%
IP16	220.	10%	IN16	200.	5%	OP16	80.	14% ⁴

Table 1 Estimates of fine-scale resistivity striations for the ingots currently being used for the spreading resistance calibration SRMs.

- 1 A code used to identify chips in a set by resistivity level, see section 6.
- 2 Nominal resistivity value for the ingot currently being used, in $\text{ohm}\cdot\text{cm}$.
- 3 Percent difference between maximum and minimum value of largest amplitude fine-scale feature.
- 4 Above initial target value.

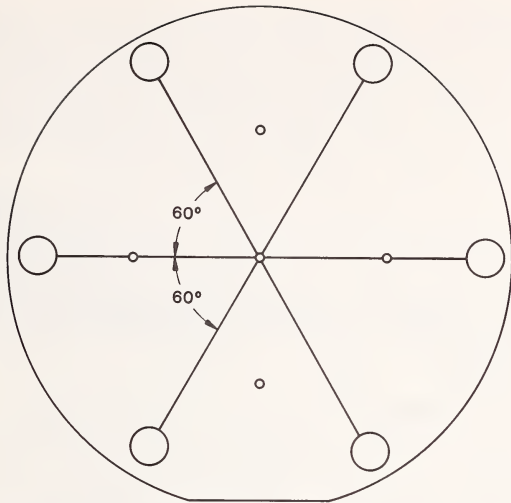


Figure 1. Schematic diagram of thickness measurement locations: 1) three diameters which were scanned for thickness uniformity using a contactless thickness gauge; large circles at the end of each diameter represent the sensing area of the contactless gauge, scaled to a 3-in. diameter slice; 2) five small circles at slice center and four half-radius points show the location of electronic-micrometer (certified) measurements.

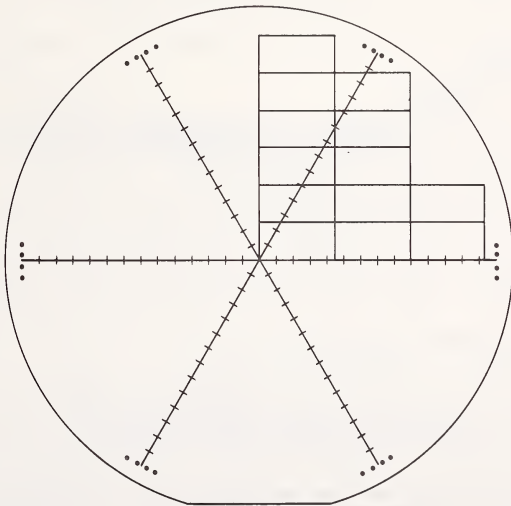


Figure 2. Schematic diagram of a 3-in. diameter slice showing: 1) three measurement diameters used for certification; 2) location of 29 measurement positions on each diameter, shown by short dashes except for outermost positions which show the location of the probe points for the 1.59-mm probe; and 3) all possible final chips of size 0.22 by 0.44 in. (shown in upper right quadrant).

of azimuthal (rotational) symmetry. Based on this expectation, a resistivity measurement sampling plan was designed which emphasized the determination of the radial resistivity variation for each slice. This sampling plan required resistivity measurements at the slice center and at intervals of 0.1 in. along each of the three diameters, 60 deg apart, that were used in the thickness uniformity scan with the contactless thickness gauge.* The measurement procedure of ASTM Method F 81 [4] was used at each location; this required that the probe array be oriented perpendicular to the measurement diameter. For each slice, dc current values were set to obtain a probe voltage of 10 to 12 mV, except for the very lowest resistivity specimens for which it was not possible to supply enough current to obtain 10 mV. For these specimens the probe voltage was that obtainable with a measurement current of 100 mA.

In this manner, a total of 57 measurements (19 along each diameter) was obtained on each 2-in. diameter slice and a total of 81 measurements (29 per diameter) on each 3-in. diameter slice. Three of these, one from each diameter, were located at the slice center. Figure 2 shows the schematic location for these resistivity measurements on a 3-in. diameter slice, together with the arrangement of SRM chips which could be cut from one quadrant of such a slice. The three-diameter profiles obtained on virtually all (111) slices showed a high degree of azimuthal (rotational) symmetry; this azimuthal symmetry was found much less often for the (100) slices. A number of examples of the resistivity data obtained using this procedure are shown in figures 3a, b, and c with the vertical axis scales shown as percent difference from the average resistivity value at the slice center.

Separate tests were run to gauge the effectiveness of the three-diameter plan for evaluating the range of resistivity variation on specimens which had shown a variety of patterns of resistivity variations. These tests used two other sampling plans, each acquiring approximately the same number of total measurements per slice as were taken with the three-diameter plan, but with more emphasis placed on measuring azimuthal variation of resistivity and less on measuring radial variation. Results of this comparison of sampling plans are illustrated in Appendix A. The superior effectiveness of the three-diameter plan in evaluating the range of resistivity variation over a full slice, without extraneous effects due to slice flats, is shown.

After characterization with the three diameter sampling plan, each of the slices was cut into a number of rectangular chips and the chips distributed among a number of sets of the appropriate SRM, according to conductivity type and crystal orientation. Each SRM set in turn contains one chip at each available resistivity level. Figure 4 shows the schematic arrangement of all chips which might potentially be used from a 3-in. diameter slice, together with the chip identification code which is used for record keeping and which appears on the contents list of all spreading resistance SRM sets.

4. ANALYSIS OF RESISTIVITY RADIAL PROFILE DATA TO GENERATE CERTIFIED RESISTIVITY AND RANGE VALUES

4.1 General Considerations

Although the three-diameter sampling plan was found to be effective for characterizing the resistivity variation on each slice as a whole, measurements were not obtained at the location of all chips which could be cut from within the sampled region of that slice. As a result, individual resistivity values for each of the chips were not obtainable with the three-diameter plan. A procedure was designed for calculating a single representative resistivity value for each slice from the array of resistivity values measured; this representative value is the certified Resistivity for the slice as a whole and for all the chips cut from the slice. A "measure of the goodness" with which this single representative resistivity applies to the individual chips from the slice was also derived. This "measure of goodness," called the Uncertainty, is formally defined in section 5.4: "Certification Uncertainty for Individual Calibration Chips in Each Set." The value of the Uncertainty will be related to the resistivity variation (Range of values) measured on each slice and to the underlying random and systematic errors in the measurement process.

4.2 Calculating the Certified Resistivity Value

Three general methods for calculating the certified Resistivity value were considered. In the order of the amount of available data base from each slice, they were: 1) calculation of the average of all measured values, 2) calculation of the mean resistivity at each radial position followed by calculation of the average of the lowest and highest of those mean values, and 3) calculation of the average of the maximum and minimum single individual values measured on the slice. Two requirements were established to evaluate these three methods: 1) the method used had to be compatible with minimizing the worst-case difference between the derived slice Resistivity value and the value likely to be appropriate for any individual chip used from that slice, and 2) the method had to be compatible with a wide variety of profile shapes, magni-

* A four-point probe measures a local average resistivity over a center-weighted area related to the probe spacing. For a probe with the spacing used for these resistivity measurements, little additional information on resistivity variation would be provided by a sampling plan with spatial intervals between measurement locations smaller than 0.1 in.

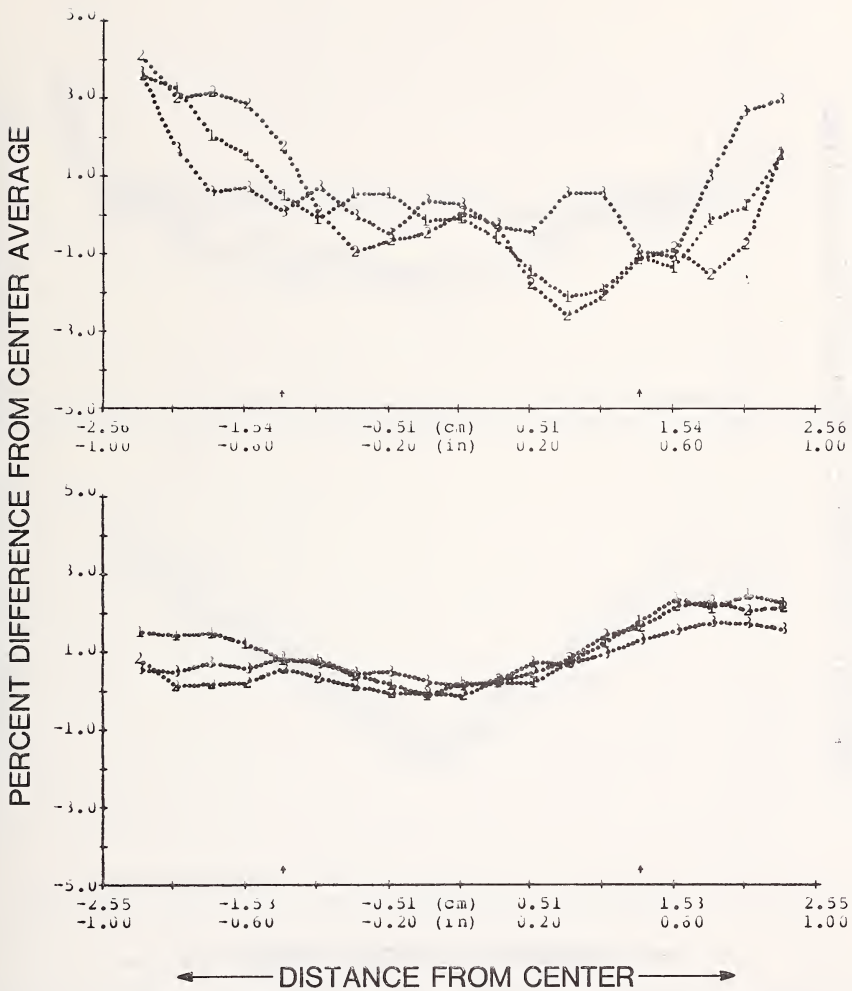


Figure 3a. Examples of nonsymmetric resistivity profiles obtained during the certification procedure.

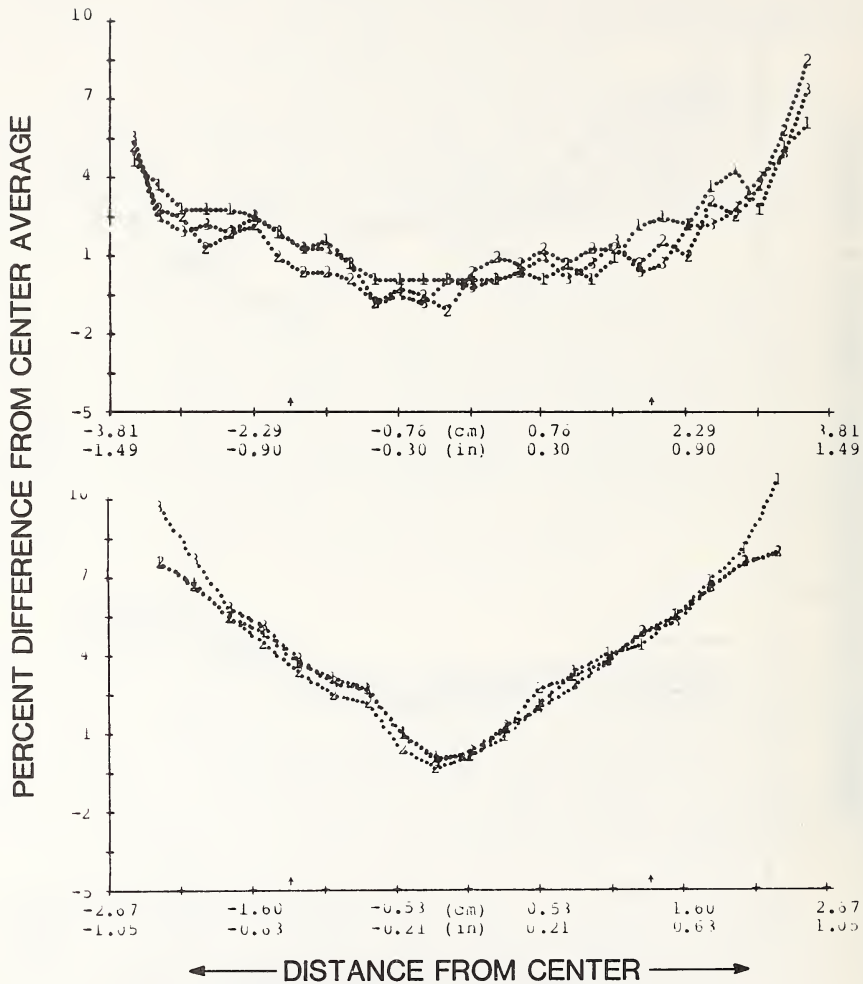


Figure 3b. Examples of nearly symmetric, but off-center, profiles obtained during the certification procedure.

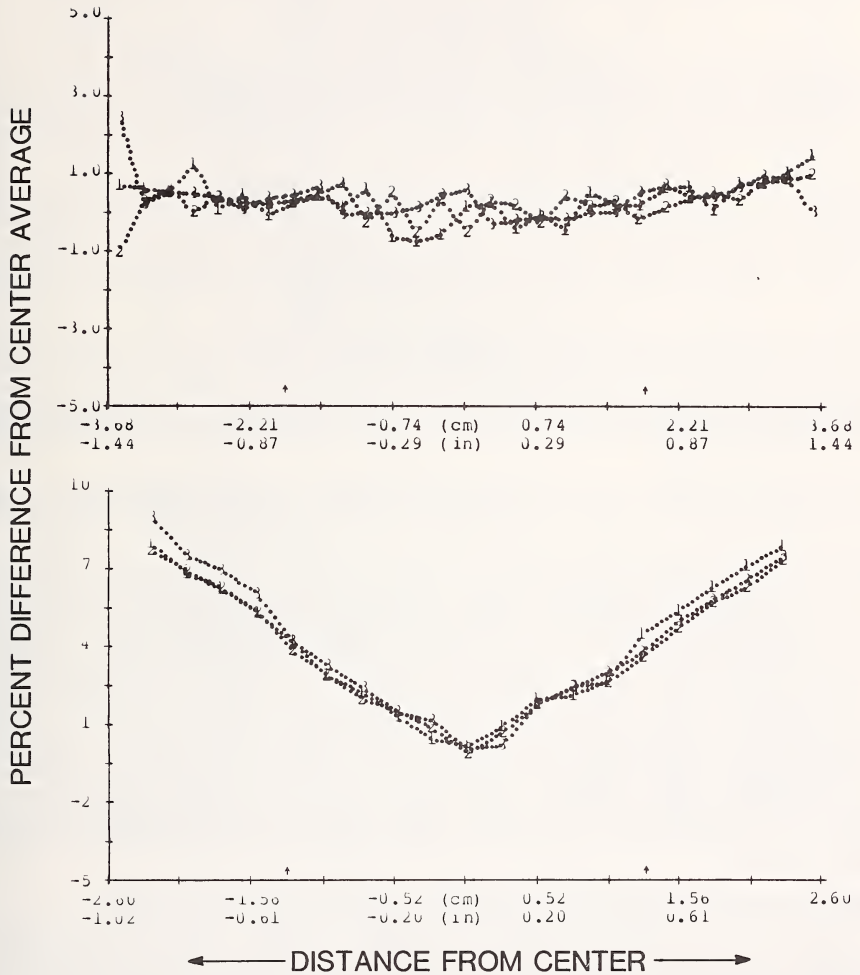


Figure 3c. Examples of symmetric profiles obtained during the certification procedure.

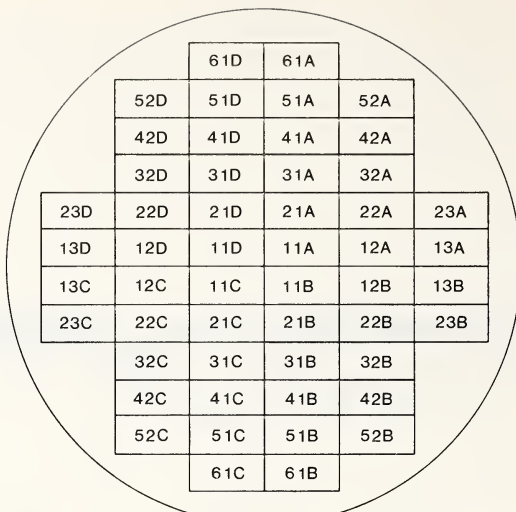


Figure 4. Schematic diagram showing the chip-numbering sequence for a 3-in. diameter slice. (Chips actually used for SRM sets depend on the region selected following analysis of profile data from each slice.)

tudes, and degrees of symmetry. The first requirement suggested some form of mid-range value would be appropriate for minimizing the worst-case difference; the second requirement suggested that any procedure based on averages be carefully examined for applicability to slices with nonsymmetric profiles.

Since use of the average of all measured values would weight the calculated resistivity to the most common values measured on a slice, and therefore increase the error for chips used from other portions of the slice, the averaging of all measured values was discarded as being nonacceptable. The method based on maximum average and minimum average values was also discarded, since, as can be seen in figure 3, for slices with nonsymmetric profiles, such local averages are not meaningful representations of the data. The third method considered, using the average of maximum and minimum individual measured values, satisfied both evaluation requirements. Since this method gives a resistivity value which is a midpoint of the range of all measured values without respect to where those values were measured, it does not bias the result toward the low or high side of the measurement range or to any specific portion of the slice. Consequently, it minimizes the worst-case differences between the "representative" value which would be certified for the entire slice and the "true," but unknown, value for chips taken from the vicinity of either the lowest or highest values measured on the slice. Further, since it avoids use of averages as a function of position, it is applicable both to symmetric and nonsymmetric profiles. As noted, this procedure does not weight the final result to the most common measured value. In this sense the final Resistivity may not be the "most correct" representation of the slice as a whole; nevertheless, it is the "fairest" representation since it balances the error among individual chips, and consequently, it balances the risk of error borne by individual set users.

4.3 Use of the Range of Measured Values to Relate Slice Resistivity to Individual Chips

In conjunction with use of this average of individual measurement extrema as the certified slice Resistivity, the difference, or Range, between these maximum and minimum values was chosen as the basis for calculating the "goodness" with which the certified Resistivity represented the resistivity of the individual chips cut from the slice. Such a procedure does have two identifiable drawbacks, however. The first, applicable to slices with symmetric profiles, is that it may be overly conservative.* The second drawback primarily applies to slices with noticeably nonsymmetric profiles. For such slices, with symmetry absent, it is not possible to correlate data obtained along different diameters and to estimate the extent

* When evaluating measurement error or uncertainty, using a "conservative" value means using a value which is somewhat inflated, i.e., on the high side of the likely values.

to which the maximum and minimum observed values represent real resistivity extrema rather than measurement errors. Consequently, for nonsymmetric profiles, the Range of observed values may understate the true resistivity variation. However, guard factors (as explained in section 5.4 on certification Uncertainty) are used to protect against such underestimation, and where the original maximum or minimum appeared significantly inconsistent with the shape of the profile, complete remeasurement of slices was employed to protect against significant overestimation.

4.4 Auxiliary Procedure to Improve Quality of Certification

The use of the individual maximum and minimum measured values to calculate certified values for each slice left one degree of freedom to improve the quality of certification (i.e., reduce the Uncertainty) for each slice and for the chips used from that slice. This was the choice of the area of the slice from which the final chips would be taken (and consequently the portion of the profile data which was used to extract the certified values).

Before a procedure to select the slice area could be formulated (as described below), it was necessary to determine the size of the chips which would be cut from the slices. Choice of chip size was a compromise between making the chips large enough so that they would last for a reasonable amount of time in use and making them small enough both to obtain a reasonable chip yield from each slice and to assure that the variations in resistivity which occurred on any one chip would be acceptably small. After numerous computational tests on data from a variety of profile types, a chip size of 0.22 in. by 0.44 in. (approx. 5.6 by 11.2 mm) was found to be a reasonable compromise.

The selection of the size and location of the slice area to be used for SRM chips was done in conjunction with target values for the certification Uncertainty and with the development and application of an auxiliary analysis procedure. Target values for maximum Uncertainty were set at 5% for p-type specimens and at 10% for n-type specimens. The auxiliary analysis procedure entailed estimation of the lowest and highest resistivity values likely to be encountered on any chip cut from each starting slice. This chip estimation procedure, which was applied to all slices for which the range of values was judged adequately

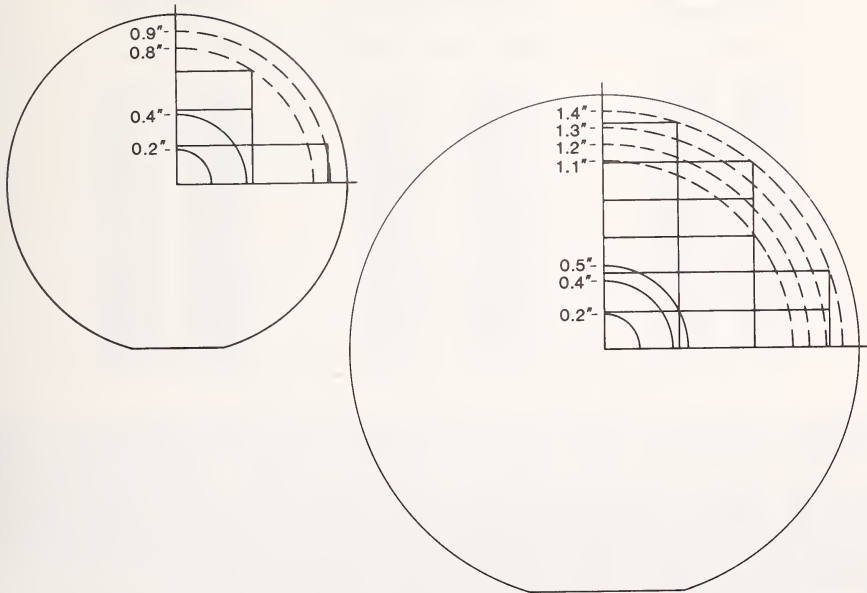


Figure 5. Schematic diagram for 2-in. and 3-in. diameter slices: 1) possible inner starting points for data analysis (solid line arcs), 2) possible outer stopping points for data analysis (dashed line arcs), and 3) layout of chips with respect to these limits; to be usable, no part of a chip may extend more than 0.010 in. beyond the analysis limits chosen.

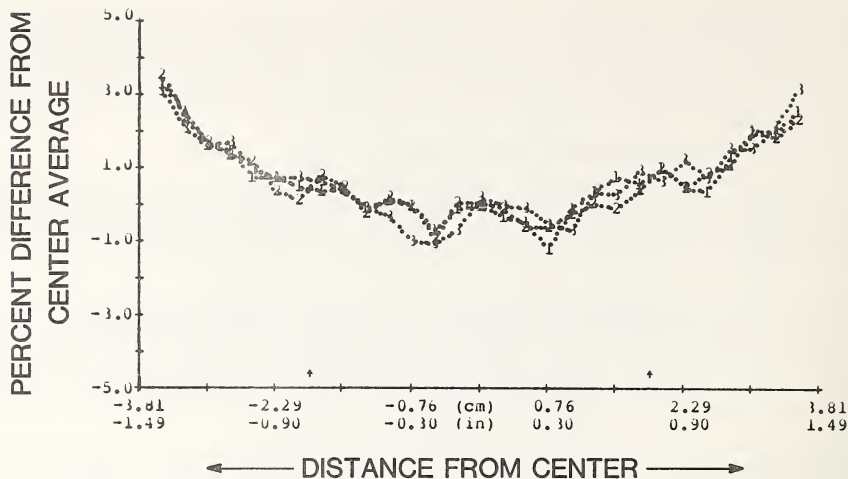


Figure 6a. Resistivity profile and data reduction for a symmetric profile with relatively small range value: 3-in. diameter, (100) p-type slice.

Radial Distance From Center		Average & Standard Deviation (by position)		Extremum Values (by position)	
(cm.)	(inch)	Ave. of all	(1s%)	Min. val.	Max. val.
0.000	(0.00)	0.013653	0.11	0.01364	0.01367
0.254	(0.10)	0.013617	0.27	0.01355	0.01365
0.508	(0.20)	0.013557	0.34	0.01350	0.01363
0.762	(0.30)	0.013567	0.48	0.01348	0.01364
1.016	(0.40)	0.013620	0.32	0.01355	0.01367
1.270	(0.50)	0.013650	0.25	0.01361	0.01369
1.524	(0.60)	0.013693	0.29	0.01363	0.01375
1.778	(0.70)	0.013727	0.22	0.01369	0.01377
2.032	(0.80)	0.013733	0.33	0.01366	0.01378
2.286	(0.90)	0.013733	0.31	0.01369	0.01381
2.540	(1.00)	0.013750	0.27	0.01369	0.01380
2.794	(1.10)	0.013832	0.20	0.01379	0.01387
3.048	(1.20)	0.013878	0.21	0.01385	0.01392
3.302	(1.30)	0.013932	0.24	0.01389	0.01398
3.556	(1.40)	0.014047	0.43	0.01396	0.01412

large compared to the scatter in the data, and for which the resistivity profile symmetry was judged high, was implemented in the following manner. The resistivity values from each of the three diameters (each of six radii) were averaged as a function of distance from the slice center. The radial distances from the slice to the nearest and farthest points of each chip were used as a "window" on the average radial profile to calculate the lowest and highest expected resistivity values for that chip. Where calculated, the estimates of lowest and highest expected resistivity for each chip are reported on the SRM certificates. These estimates are not certified, however, both because portions of the slice from which some chips were cut were not intersected by any measurement diameter and because the assumption of radial symmetry of resistivity, even when apparent in the available data, may not strictly be true.

These estimates of the highest and lowest expected resistivity for each chip, together with the calculated values of Resistivity and Range which resulted from analyzing each of several possible circular or annular regions of each slice, were used to make final decisions on how much of a given slice to use for SRM chips. Figure 5 shows a number of possible inner and outer radial limits for defining the region

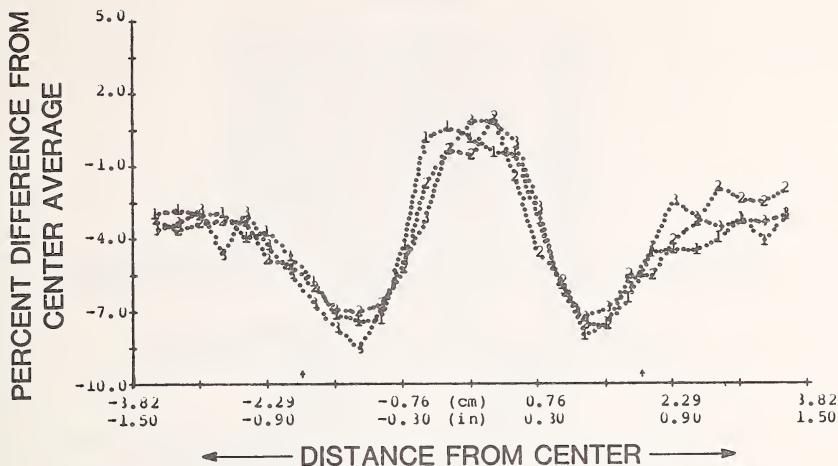


Figure 6b. Resistivity profile and data reduction for a symmetric profile with relatively large range value: 3-in. diameter, (100) p-type slice.

Radial Distance From Center		Average & Standard Deviation (by position)		Extremum Values (by position)	
(cm.)	(inch)	Ave. of all	(1s%)	Min. val.	Max. val.
0.000	(0.00)	80.3450	0.68	79.803	80.895
0.254	(0.10)	80.4110	0.67	79.873	81.045
0.508	(0.20)	79.3333	1.25	77.708	80.361
0.762	(0.30)	76.9457	1.00	76.115	78.063
1.016	(0.40)	75.1402	0.62	74.446	75.681
1.270	(0.50)	74.2007	0.63	73.413	74.748
1.524	(0.60)	74.4767	0.38	74.120	74.804
1.778	(0.70)	75.4172	0.48	74.918	75.922
2.032	(0.80)	76.2908	0.48	75.856	76.705
2.286	(0.90)	77.0875	0.84	76.411	78.265
2.540	(1.00)	77.4457	0.61	76.663	77.946
2.794	(1.10)	77.5387	0.99	76.479	78.713
3.048	(1.20)	77.8550	0.37	77.597	78.339
3.302	(1.30)	77.6107	0.59	76.940	78.211
3.556	(1.40)	77.8692	0.58	77.319	78.692

analyzed on 2-in. and 3-in. slices and the relation of those limits to the chips which would be cut from one quadrant of those slices.

Examples of application of these analysis procedures to slice profiles are shown in the next two figures. Figure 6 shows the resistivity profiles for two 3-in. slices having profiles sufficiently symmetric to estimate resistivity values for individual chips. Figure 7 shows the analysis sheets for these two slices, giving resistivity estimates for individual chips at the top of the sheets followed by the values of resistivity and range that were calculated using the data from various regions of each slice (as shown schematically in fig. 5). For the slice whose profile is shown in fig. 6A (analyses shown in fig. 7A), all chips have an estimated uniformity of 2.2%, or better, and are considered acceptable for use. Since the range values calculated for any of the six slice regions chosen for analysis are considered reasonable, analysis #6 which includes the entire slice is chosen as the appropriate compromise between chip quality, certified Range value, and yield. In contrast with this is the slice whose profile is shown in fig. 6B (analyses shown in fig. 7B). For this slice, the first two chips listed (taken from the center region of

CHIP ANALYSIS

CHIP CODE	ESTIMATED	MIN/MAX	%DIFF
CHIP 11	0.013557	0.013653	0.71
CHIP 21	0.013559	0.013701	1.05
CHIP 31	0.013632	0.013733	0.74
CHIP 41	0.013713	0.013747	0.25
CHIP 51	0.013733	0.013871	1.00
CHIP 61	0.013832	0.014036	1.48
CHIP 12	0.013632	0.013735	0.75
CHIP 22	0.013648	0.013747	0.73
CHIP 32	0.013701	0.013832	0.96
CHIP 42	0.013733	0.013902	1.23
CHIP 52	0.013747	0.014047	2.18
CHIP 13	0.013733	0.013975	1.76
CHIP 23	0.013735	0.014036	2.20

SLICE ANALYSES

1) OUTER RAD. THIS ANAL. 1.2, INNER RADIUS 0.0 in.
 INCLUDES .22x.44 in. CHIP #'s: 11 21 31 41 51 12 22 32

EXTREMA	0.013480
MINIMUM	0.013480
MAXIMUM	0.013920
MEAN =	0.013700
RANGE (%) =	3.21

2) OUTER RAD. THIS ANAL. 1.3, INNER RADIUS 0.0 in.
 INCLUDES .22x.44 in. CHIP #'s: 11 21 31 41 51 12 22 32 42

EXTREMA	0.013480
MINIMUM	0.013480
MAXIMUM	0.013980
MEAN =	0.013730
RANGE (%) =	3.64

3) OUTER RAD. THIS ANAL. 1.3, INNER RADIUS 0.2 in.
 INCLUDES .22x.44 in. CHIP #'s: 21 31 41 51 12 22 32 42

EXTREMA	0.013480
MINIMUM	0.013480
MAXIMUM	0.013980
MEAN =	0.013730
RANGE (%) =	3.64

4) OUTER RAD. THIS ANAL. 1.3, INNER RADIUS 0.4 in.
 INCLUDES .22x.44 in. CHIP #'s: 31 41 51 12 22 32 42

EXTREMA	0.013550
MINIMUM	0.013550
MAXIMUM	0.013980
MEAN =	0.013765
RANGE (%) =	3.12

5) OUTER RAD. THIS ANAL. 1.4, INNER RADIUS 0.5 in.
 INCLUDES .22x.44 in. CHIP #'s: 41 51 61 22 32 42 52 13 23

EXTREMA	0.013610
MINIMUM	0.013610
MAXIMUM	0.014120
MEAN =	0.013865
RANGE (%) =	3.68

6) OUTER RAD. THIS ANAL. 1.4, INNER RADIUS 0.0 in.
 INCLUDES .22x.44 in. CHIP #'s: 11 21 31 41 51 61 12 22 32 42 52

EXTREMA	0.013480
MINIMUM	0.013480
MAXIMUM	0.014120
MEAN =	0.013800
RANGE (%) =	4.64

STRIATION MAGNITUDE (%) 6.

Figure 7a. Individual chip resistivity estimates for the symmetric profile shown in figure 6a, and six analyses of slice data using inner and outer radial limits as represented in figure 5. Since all chips are estimated to be acceptably uniform and since all slice analyses have acceptable range values, analysis #6 is chosen as the best compromise between yield, chip quality and certified range value.

CHIP ANALYSIS

CHIP CODE	ESTIMATED	MIN/MAX	%DIFF
CHIP 11	74.276	80.411	8.26
CHIP 21	74.201	78.856	6.27
CHIP 31	74.201	76.231	2.74
CHIP 41	75.041	77.388	3.13
CHIP 51	76.928	77.808	1.14
CHIP 61	77.539	77.855	0.41
CHIP 12	74.201	77.113	3.92
CHIP 22	74.201	77.388	4.30
CHIP 32	74.686	77.539	3.82
CHIP 42	76.231	77.855	2.13
CHIP 52	77.388	77.869	0.62
CHIP 13	76.928	77.855	1.20
CHIP 23	77.113	77.855	0.96

SLICE ANALYSES

1) OUTER RAD. THIS ANAL. 1.2, INNER RADIUS 0.0 in.
 INCLUDES .22x.44 in. CHIP #'s: 11 21 31 41 51 12 22 32

MINIMUM	EXTREMA
MAXIMUM	73.4130
MEAN =	81.0450
RANGE (%) =	77.2290
	9.88

2) OUTER RAD. THIS ANAL. 1.3, INNER RADIUS 0.0 in.
 INCLUDES .22x.44 in. CHIP #'s: 11 21 31 41 51 12 22 32 42

MINIMUM	EXTREMA
MAXIMUM	73.4130
MEAN =	81.0450
RANGE (%) =	77.2290
	9.88

3) OUTER RAD. THIS ANAL. 1.3, INNER RADIUS 0.2 in.
 INCLUDES .22x.44 in. CHIP #'s: 21 31 41 51 12 22 32 42

MINIMUM	EXTREMA
MAXIMUM	73.4130
MEAN =	80.3610
RANGE (%) =	76.8870
	9.04

4) OUTER RAD. THIS ANAL. 1.3, INNER RADIUS 0.4 in.
 INCLUDES .22x.44 in. CHIP #'s: 31 41 51 12 22 32 42

MINIMUM	EXTREMA
MAXIMUM	73.4130
MEAN =	78.7130
RANGE (%) =	76.0630
	6.97

5) OUTER RAD. THIS ANAL. 1.4, INNER RADIUS 0.5 in.
 INCLUDES .22x.44 in. CHIP #'s: 41 51 61 22 32 42 52 13 23

MINIMUM	EXTREMA
MAXIMUM	73.4130
MEAN =	78.7130
RANGE (%) =	76.0630
	6.97

6) OUTER RAD. THIS ANAL. 1.4, INNER RADIUS 0.4 in.
 INCLUDES .22x.44 in. CHIP #'s: 31 41 51 61 12 22 32 42 52 13 23

MINIMUM	EXTREMA
MAXIMUM	73.4130
MEAN =	78.7130
RANGE (%) =	76.0630
	6.97

STRIATION MAGNITUDE (%) 14.

Figure 7b. Individual chip resistivity estimates for the symmetric profile shown in figure 6b, and six analyses of slice data using inner and outer radial limits as represented in figure 5. Estimates for chips 11 and 21 show unacceptable nonuniformity; analysis #6 which ignores the core of the slice out to a radius of 0.4 in. is chosen as the best compromise.

SRM 2526, Set No. 21

Specimen Code	Certified Measurement Values			Additional Information - Values Not Certified			
	Resistivity (Ωcm)	Range (%)	Uncertainty, Σ (%)	Dopant*	Growth* Process	Estimates of Chip Minimum and Maximum Values**	Fine Scale Resistivity Variation (%)
1P01	0.000595	3.7	3.6	BORON	CZ	0.000589-0.000599	5
1P02	0.00116	4.3	3.9	BORON	CZ	0.00113-0.00114	6
1P03	0.00178	3.4	3.4	BORON	CZ	0.00176-0.00178	5
1P04	0.00565	2.8	3.1	BORON	CZ	0.00558-0.00562	6
1P05	0.0154	4.8	4.2	BORON	CZ	0.0152-0.0153	5
1P06	0.0242	5.0	4.3	BORON	CZ	0.0242-0.0244	6
1P07	0.0603	2.5	2.9	BORON	CZ	N.A.	8
1P08	0.137	9.1	6.6	BORON	FZ	0.133-0.141	8
1P09	0.332	2.6	3.0	BORON	CZ	N.A.	5
1P10	0.756	2.8	3.1	BORON	CZ	0.750-0.754	6
1P11	2.66	4.0	3.8	BORON	CZ	2.66-2.70	6
1P12	4.93	3.3	3.4	BORON	CZ	4.91-4.96	6
1P13	10.8	2.7	3.1	BORON	CZ	N.A.	5
1P14	21.7	4.9	4.3	BORON	CZ	21.6-21.7	6
1P15	72.9	2.2	2.8	BORON	FZ	N.A.	6
1P16	222.	4.2	3.9	BORON	FZ	219-223	10

*As provided by the crystal manufacturer.

**The symbol "n.a." indicates the calculation was "not applicable" to this chip.

Table 2a Data table from the certificate of a set of SRM 2526 for (111) p-type silicon.

Specimen Code	Certified Measurement Values			Additional Information - Values Not Certified			
	Resistivity (Ω .cm)	Range (%)	Uncertainty, Σ (%)	Dopant*	Growth* Process	Estimates of Chip Minimum and Maximum Values**	Fine Scale Resistivity Variation (%)
1N01	0.000778	4.1	3.8	PHOS	CZ	0.000764-0.000786	4
1N02	0.00249	7.6	5.8	PHOS	CZ	0.00250-0.00257	10
1N03	0.00510	7.3	5.6	PHOS	CZ	0.00492-0.00511	5
1N04	0.00862	5.7	4.7	PHOS	CZ	0.00857-0.00876	4
1N05	0.0271	6.6	5.2	PHOS	CZ	0.0268-0.0275	7
1N06	0.0549	5.3	4.5	PHOS	CZ	0.0551-0.0562	5
1N07	0.152	8.2	6.1	PHOS	CZ	0.153-0.158	8
1N08	0.301	10.0	7.1	PHOS	CZ	0.290-0.301	10
1N09	0.535	7.7	5.8	PHOS	CZ	0.529-0.541	10
1N10	1.35	4.6	4.1	PHOS	CZ	N.A.	10
1N11	2.87	9.5	6.8	PHOS	CZ	2.77-2.89	12
1N12	6.62	8.1	6.0	PHOS	CZ	6.43-6.52	14
1N13	11.2	14.4	9.5	PHOS	CZ	11.5-11.9	14
1N14	26.7	2.5	2.9	PHOS	NTD	N.A.	5
1N15	74.8	1.3	2.3	PHOS	NTD	N.A.	5
1N16	195.	2.9	3.2	PHOS	NTD	N.A.	5

*As provided by the crystal manufacturer.

**The symbol "n.a." indicates the calculation was "not applicable" to this chip.

Table 2b Data table from the certificate of a set of SRM 2527 for (111) n-type silicon.

the slice) are estimated to be unacceptably nonuniform. Consequently, this region of the slice is excluded from use, and the first three slice analyses are rejected. The last three modes of slice analysis (all of which omit the center region of the slice but differ in the area and number of chips included) have the same calculated Range value. Of these, analysis #6 which includes the annular area between radial values of 0.4 and 1.4 in. is chosen as the best compromise since it offers the widest choice of chips without inflation of the Range value.

4.5 Examples of Certificate Data Tables Showing Certified and Noncertified Information

Tables 2a and b show certificates for two actual SRM sets, one p-type and one n-type, illustrating the certified and noncertified information specifically evaluated for the components of each SRM set. The certified Resistivity is the average of the minimum and maximum individual measured resistivity values in the region of the slice chosen for use. The certified Range is the difference between these minimum and maximum values expressed as a percent of the certified Resistivity. The exact meaning of the certified Uncertainty will be explained in the following section. Note however, that except for the eighth level of the p-type set (specimen code 1P08), it was always possible to stay within the target values for Uncertainty, 5% for p-type slices and 10% for n-type slices.

5. RELATION BETWEEN VALUES MEASURED ON A STARTING SLICE AND VALUES FOR INDIVIDUAL SPECIMEN CHIPS: CALCULATION OF CERTIFICATION UNCERTAINTY

5.1 Overview

As already described, as a natural consequence of silicon crystal growth, none of the starting silicon slices from which the chips in these SRM sets were cut had uniform resistivity. However, for each slice, the amount of nonuniformity was estimated from an array of resistivity measurements using the three-diameter sampling plan. A single resistivity value, the average of the highest and lowest values measured within the selected region, was then calculated and certified to represent the slice (and all chips from the selected region). That one certified Resistivity value then appears on the certificate for each SRM set which contains a chip from that slice.

The most important question to anyone using such chips to establish a resistivity to spreading resistance calibration is: "How well does each certified Resistivity value on my certificate represent the resistivity value of the corresponding chip in my set?" To put the question another way: "What error in resistivity scale am I likely to experience during spreading resistance calibration when I use the value on the certificate?" In the next three sections, an expression for this "error" in resistivity values will be developed. It will be shown to be composed of two types of measurement system error, or uncertainty, which essentially have a fixed value regardless of resistivity level (sec. 5.2), and an error, or uncertainty, based on the nonuniformity of each slice, the value of which therefore changes from slice to slice (sec. 5.3). Finally, the manner for combining these two contributions will be given and a bound on the combined "error" will be derived to form a parameter termed the certification Uncertainty (sec. 5.4).

5.2 Uncertainty of Resistivity Values Due to Measurement Errors

The short-term random error, or measurement scatter, associated with the four-probe resistivity measurements can be estimated from the standard deviation of a number of measurements taken with different probe orientations at the center of a slice in the manner described in ASTM Method F 84 [6]. Such estimates of the precision have been found in this laboratory to vary from about 0.1% to about 0.4%, depending on specimen resistivity and surface preparation. The value of 0.4% is used as a conservative estimate of the short-term random error (one standard deviation) for the certification of these spreading resistance SRMs.

An estimate of the short-term systematic error between the resistivity scale in effect at the time of any of the certification measurements and the long-term average response of the NBS resistivity measurement facility is obtained from several long-term measurement reproducibility studies at NBS. These studies, primarily based on specimens at approximately 0.1 and 10 Ω .cm, including slices from SRM 1521, indicate that a value of 0.33% is a conservative estimate of the long-term random error, one standard deviation, of the NBS resistivity measurement process due to unknown sources (see Appendix B for examples of these data). This value is supported by less extensive studies of slices from SRM 1522 and SRM 1523 which have resistivity values from 0.01 to 180 Ω .cm. For measurements on any one slice (taken at any given time), or for any one chip in a user's SRM set, this error acts as a short-term systematic error or bias (with a maximum absolute value (3σ) of 1%) compared to the long-term NBS baseline. However, for the full array of chips in a typical SRM set (which come from slices measured over a period of several months), this long-term error is unlikely to act as a systematic bias with constant value. Therefore, insofar as it affects the relation between the Resistivity values (on the certificate) for a complete set of SRM chips and the long-term NBS baseline, this error is best modeled as an additional component of random error.

This long-term random error is taken to be independent of the short-term random error. Because they are considered independent, they can be combined in root-mean-square fashion to give a combined random error of 0.52% (one standard deviation). This total random error, which relates a single measured value such as an observed minimum or maximum resistivity to the NBS baseline, can be stated at the 99% confidence level (three standard deviations) as 1.56%. In other words, there is a 99% confidence that the resistivity value measured at a single location on a slice is within 1.56% of the resistivity scale established by the long-term NBS baseline.*

This is a conservative statement for the error of a single feature from a nonsymmetric profile. It is even more conservative for a maximum or minimum taken from a symmetric profile.

5.3 Uncertainty of Resistivity Values Due to Silicon Slice Nonuniformity

Because the four-probe averages over an area, the effect of thickness nonuniformity on these measurements is expected to be no worse than $\pm 0.2\%$ [8]. The allowances built into the "guard factor" (next section) as well as the conservative estimates of the measurement process error are considered sufficient to implicitly allow for such errors due to thickness fluctuations. Therefore, no explicit term for thickness fluctuations is used. For a typical chip in an SRM set, the primary source of error between the "true," but unknown, resistivity value of the chip and the value given on the certificate is due to the radial nonuniformity of resistivity of the starting slice. As a result of this nonuniformity, only a few chips from each slice have resistivity values which actually fall at the Resistivity certified for that slice. However, the use of maximum and minimum individual measurement values from each slice to calculate the Range values and the use of an additional allowance for unmeasured portions of the slice via the "guard factor" are considered a conservative allowance for all resistivity variations on the region of the slice which was used.

5.4 Certification Uncertainty for Individual Calibration Chips in Each Set

A parameter, called the Uncertainty, Σ , can be expressed based on the combined effects of measurement error and the observed silicon slice nonuniformity. This expression, which is evaluated separately for each chip in any of these SRM sets, is given as a percent of the certified Resistivity by:

$$\Sigma = [K (\text{Range}/2) + 1.56], \%$$

The guard factor, K, which is assigned the value 1.1 for slices with symmetric profile data and the value 1.2 for slices with nonsymmetric profile data, allows for possible additional resistivity excursions on unmeasured diameters as well as for errors caused by thickness variations. The Range value appropriate to each chip in a set is given in table 1 of the certificate for that set. The term 1.56% includes, at the 99% confidence level, the effects of both short-term and long-term random errors, previously discussed. Values of the Uncertainty, Σ , are also given in table 1 of each certificate for each of the chips in that set.

The Uncertainty, Σ , can be used to calculate bounds on the resistivity values of any slice which should include the "true" values of all chips cut from the certified region of that slice relative. These resistivity bounds are given by:

$$\text{Resistivity} (1 \pm \Sigma/100) .$$

A derivation is given in Appendix C for the confidence level of the resistivity bounds. Except where the stated Range value is small, the dominant term in the calculated Uncertainty and the resulting resistivity bounds are due to the resistivity nonuniformity of the starting slice. Because resistivity values are determined by the crystal growth process, the nonuniformity is not random. Therefore, the stated Range values cannot be used to estimate any other statistical parameter, such as a 90% confidence level, for the uncertainty of individual chip resistivity values.

6. CARE AND USE OF SPREADING RESISTANCE SRM SETS

Each silicon chip in these Spreading Resistance SRM sets is waxed to one facet of a dual-angle beveling block. The nominal angles on each block are 0.5 deg and 3 deg. The angles were chosen to be compatible with many common spreading resistance applications. The blocks themselves can be directly mounted on most spreading resistance instruments. The underside of each block is inscribed with a four-character code. The first character is "1" for (111) orientation or "0" for (100) orientation. The second character is "N" or "P" for the conductivity type. The third and fourth characters are a two-digit code for the resistivity level of the particular chip mounted on that block. The resistivity level code for all

* The value printed on the certificate, 1.57%, is slightly different from the value given here which is based on a more refined error model.

four sets currently runs from "01" to "16". This four-digit chip-identifying code is also given in the first column of the certificate and on the SRM set contents list packed with each set.

When establishing a spreading resistance calibration relation, the spreading resistance values obtained on each calibration specimen will have a precision determined by the surface preparation used, by the stability of the probes being used, and by the underlying resistivity striation structure of the specimen. Prior to the first use of these SRM specimens, it is recommended that each chip be polished, preferably with fine grain diamond, 0.5- μ m grain size, or less, across the entire surface area and then checked for striation structure with a spreading resistance probe. The user should then evaluate the need for a sampling plan to minimize possible uncertainty in future spreading resistance calibrations caused by any striations observed. This procedure is particularly recommended for calibration chips which will be used to calibrate measurements on epitaxial structures.

Good spreading resistance practice dictates that the specimen to be tested and the calibration specimens be prepared as similarly as possible. This includes use of the same surface preparation procedure and subsequent thermal or chemical treatment, and in the case of bevel sectioning, trying to keep the beveled area of test and calibration samples of similar size. Where the application of these calibration sets is primarily to depth profiling of beveled specimens, it may be advisable to cut each of the calibration chips in the SRM sets into several smaller chips of the size normally used for the depth-profile test specimens. Any such cutting of the calibration chips should be done with a diamond saw and should not be attempted with a scribe and break technique. This should be done only after the chip has been initially characterized for uniformity, as in the preceding paragraph.

No recommendation is made here regarding the polishing procedure to be used for preparing the calibration chips and test specimens in actual use, since the choice of procedure must often be dictated by the nature of the test specimen [9,10]. No recommendation is made regarding the acceptability of the common expedient of mounting all calibration specimens on a single fixture for simultaneous preparation. All such options regarding the nature of surface preparation of the calibration specimens as well as the required frequency of re-preparation should be established by the user. A statistical summary of intralaboratory short-term repeatability and long-term reproducibility of spreading resistance measurements, derived from a multi-laboratory experiment, for three common surface preparations is contained in ASTM Method F 525-83, Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe [11].

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APPENDIX A

COMPARISON OF RESULTS FROM THREE-, FOUR-, AND SIX-DIAMETER SAMPLING PLANS

Figures A-1 through A-3 compare the amount of detail obtained with the three-diameter measurement plan and with two alternate sampling plans. All three sampling plans acquire approximately the same amount of total data on each slice. These alternate plans utilized 1) measurements at intervals of 0.15 in. along four diameters, 45 deg apart, and 2) measurements at intervals of 0.2 in. along six diameters, 30 deg apart. However, as can generally be seen, the four-diameter and six-diameter sampling plans, while adding more information about azimuthal resistivity variation, generally fail to provide as much information about the range of resistivity variation of a slice as the three-diameter sampling plan. Further, significant measurement error was often encountered at the end of one diameter with both the four-diameter and six-diameter sampling plans due to proximity to the slice-orientation flat. Therefore, the three-diameter sampling plan is seen to be superior to the others for extracting the resistivity structure of a slice while avoiding spurious effects at the slice flat.

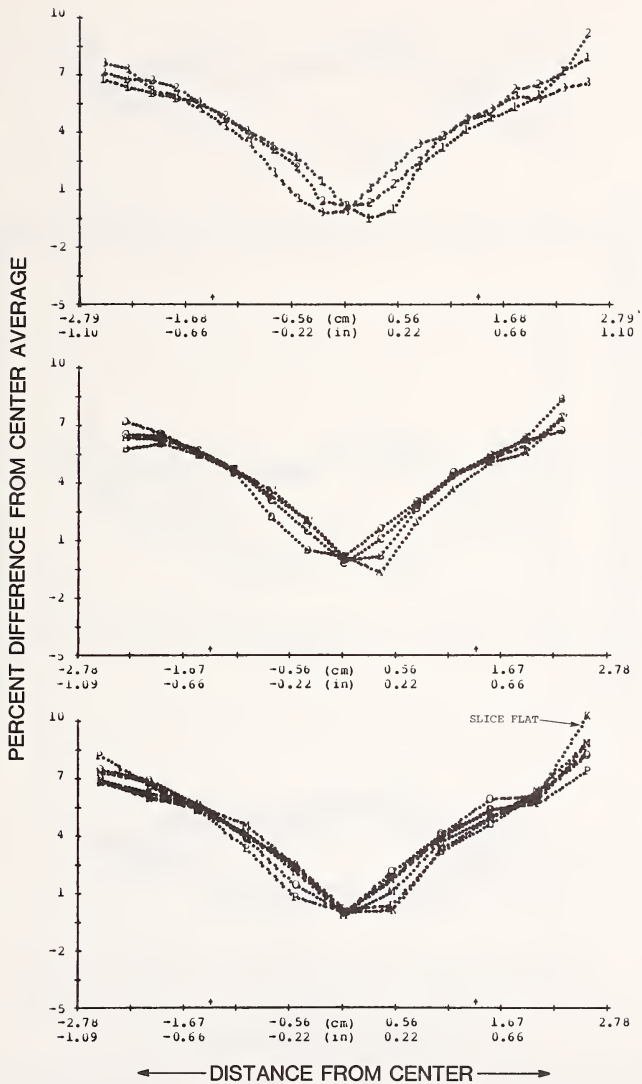


Figure A1. Example of three-, four-, and six-diameter profiles for a (111) n-type slice, approximately $0.002 \Omega \cdot \text{cm}$.

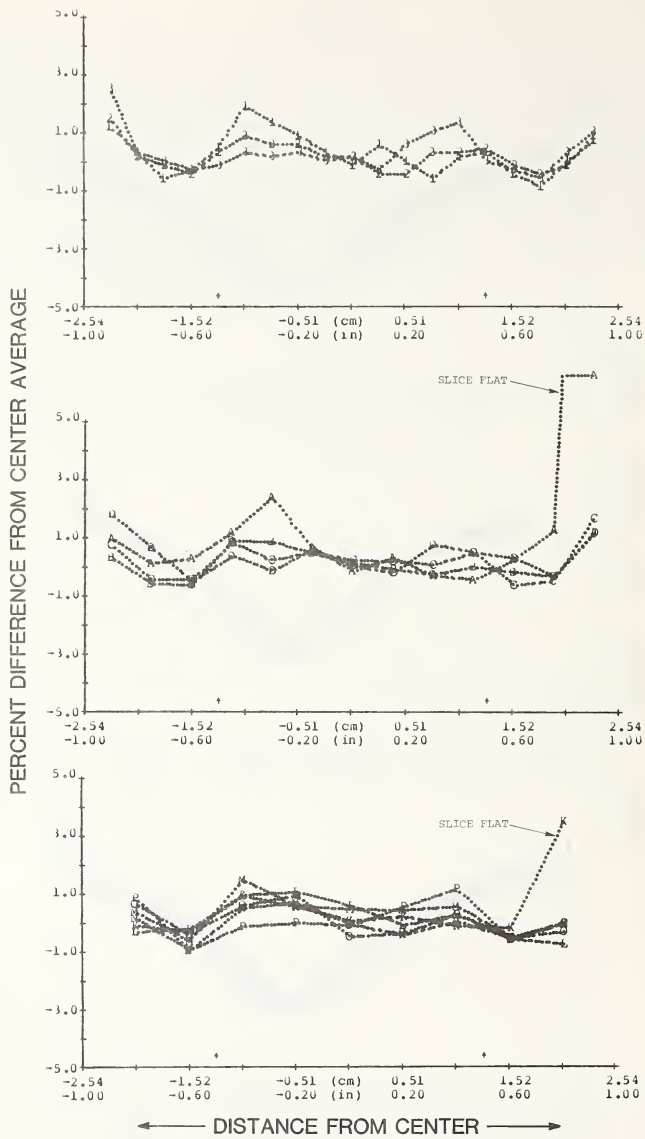


Figure A2. Example of three-, four-, and six-diameter profiles for a (100) n-type slice, approximately 0.007 Ω -cm.

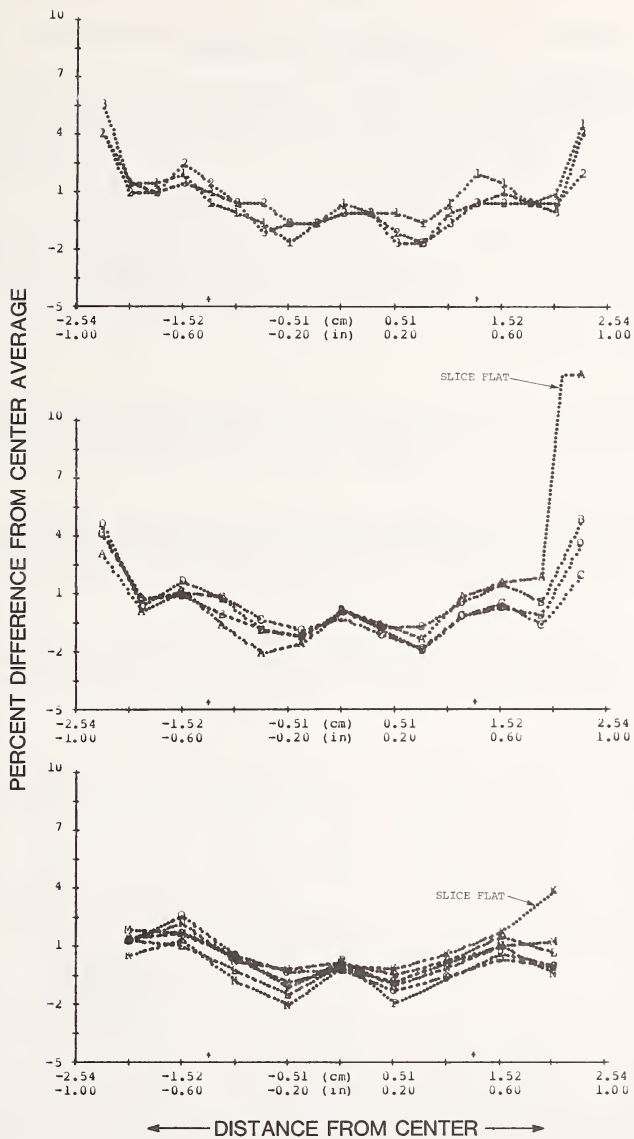


Figure A3. Example of three-, and four-, and six-diameter profiles for a (100) n-type slice approximately $0.002 \Omega \cdot \text{cm}$.

APPENDIX B

PROCEDURES USED TO MONITOR AND EVALUATE THE LONG-TERM STABILITY
OF THE FOUR-PROBE TEST STATION

Two basic types of procedures have been used both to monitor and maintain the long-term stability of the four-probe test station and to estimate measurement uncertainty due to long-term random scatter in system performance. The first is the use of control charts to track the stability of the total measurement system: current supply, DVM, standard resistor bank, and four-probe. The second is the performance of periodic two-operator/two-instrument experiments.

Control chart data were taken rather intensively for a few slices over a period of about two years in conjunction with the issuance of the first silicon resistivity SRMs in 1974. They have also been taken much less intensively, but with a continually evolving collection of slices (now totaling 60) from every crystal ever used to produce SRMs 1521, 1522, and 1523. Four examples of control chart data are shown, in figures B-1 through B-4. The first two show data taken approximately biweekly over slightly more than two years on two slices that were prototypes of SRM 1520. The second two figures show data taken much less frequently, but with four different four-probes, over four years' duration, for two actual slices from SRM 1520. These four figures substantiate the statement in section 5.2 that long-term stability of the measurement is within 1%.

Two-operator, two-instrument tests are periodically employed because of a potential ambiguity in interpreting the control charts reported here. Control charts monitor the stability of the entire measurement process, not only of the equipment used but also of the specimen itself. Hence the data are sensitive not only to probe wear and to drifts in the current supply, standard resistor, and DVM but also to the effects of cumulative probe damage on the silicon slices or to changes in the near-surface conduction process due to relapping or cleaning of a slice.

The two-operator, two-instrument procedure makes no assumptions regarding the long-term stability of a specimen. Rather, by use of two separate measurement systems, each meeting the requirements (in this case) of ASTM F 84, and two different operators to take data on a variety of test specimens, it is possible to evaluate measurement control at any given time, with negligible uncertainty caused by changes in the specimens.

Table B-1 shows data from the two-operator/two-instrument experiment which was done just prior to beginning the certification of spreading resistance SRMs in 1982. Data such as these can be used to estimate systematic biases due to equipment or to operator procedure over a wide range of resistivity values. Instrument system 1, the more automated of the two in table B-1, was the one used for certification of the spreading resistance SRM slices.

SLICE	Op. 1 / Inst. 1		Op. 1 / Inst. 2		Op. 2 / Inst. 1		Op. 2 / Inst. 2	
0.01-6 0.01-36	0.01285 0.01300	(0.19%) (0.17%)	0.01286 0.01303	(0.13%) (0.09%)	0.01283 0.01303	(0.11%) (0.10%)	0.01289 0.01304	(0.11%) (0.15%)
0.1-29 0.1-57	0.09384 0.09346	(0.18%) (0.12%)	0.09399 0.09357	(0.23%) (0.19%)	0.09398 0.09345	(0.12%) (0.17%)	0.09388 0.09338	(0.08%) (0.23%)
1-38 1-64	0.8837 0.8124	(0.11%) (0.16%)	0.8870 0.8095	(0.28%) (0.04%)	0.8857 0.8119	(0.36%) (0.37%)	0.8847 0.8133	(0.20%) (0.16%)
10-35 10-52	8.918 8.637	(0.08%) (0.23%)	8.931 8.662	(0.14%) (0.17%)	8.919 8.618	(0.19%) (0.21%)	8.912 8.644	(0.30%) (0.09%)
25-10 25-20	24.75 24.75	(0.13%) (0.26%)	24.75 24.77	(0.05%) (0.05%)	24.71 24.74	(0.07%) (0.12%)	24.72 24.72	(0.11%) (0.06%)
75-10 75-20	79.42 79.77	(0.19%) (0.17%)	79.54 79.79	(0.10%) (0.12%)	79.40 79.67	(0.14%) (0.17%)	79.42 79.67	(0.09%) (0.10%)
180-10 180-20	188.9 190.1	(0.11%) (0.23%)	189.3 190.2	(0.11%) (0.07%)	188.8 189.9	(0.14%) (0.23%)	189.1 190.0	(0.10%) (0.13%)

Table B1 Data from a two-operator/two-instrument test performed at the inception of calibration of spreading resistance SRMs. Each box shows the average of six readings and the percent standard deviation of those readings.

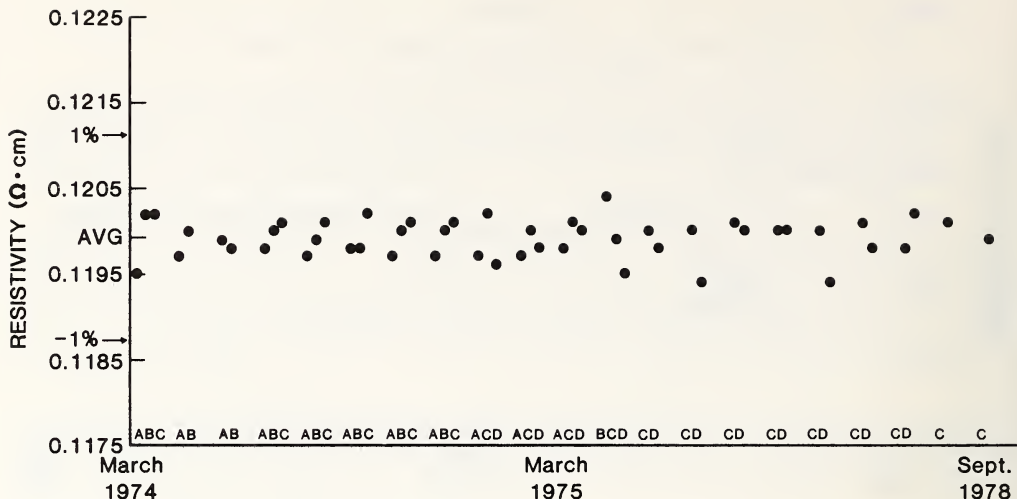


Figure B3. Resistivity measurements taken at irregular intervals over approximately four years on a low-resistivity slice from SRM 1520. Four different four-probes: A, B, C, D were used. Probes A, B, and C met the requirements of ASTM F 84; probe D used intentionally worn pins. Each entry shows the average of six readings taken in the manner of ASTM F 84.

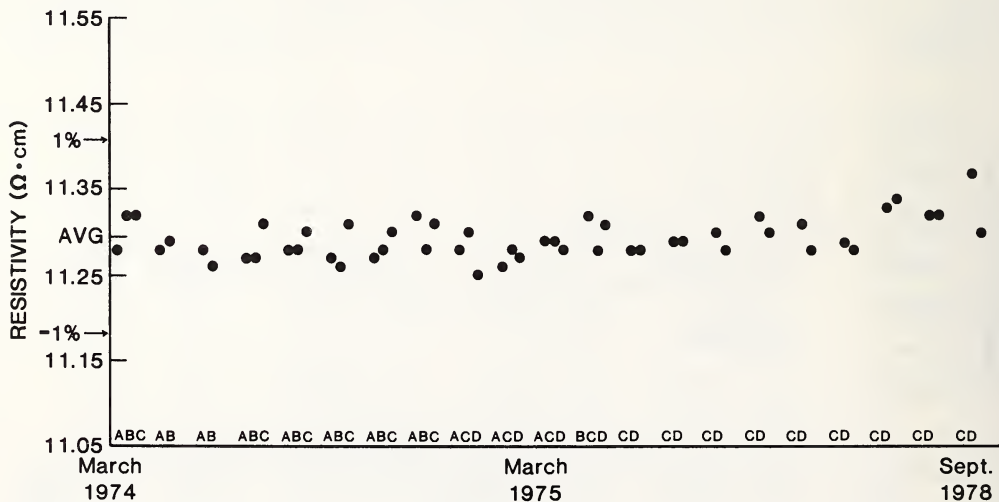


Figure B4. Resistivity measurements as in Figure B3 except at the higher resistivity level from SRM 1520.

APPENDIX C

PROBABILITY THAT THE RESISTIVITY BOUNDS BASED ON THE CERTIFICATION UNCERTAINTY VALUE INCLUDE THE "TRUE" RESISTIVITY VALUES OF ALL CHIPS FROM THE CERTIFIED REGION OF A SLICE

It was shown in section 5.2, based on consideration of random errors in the measurement process, that there is a 99% probability that any single measured value is within 1.56% of its "true" value. That is, it is within 1.56% of the value that would be obtained if measurements were made repeatedly at the same location over an extended period of time with the NBS resistivity measurement system. The question to be answered is how well two such measured values, one a minimum observed value, the other a maximum observed value, taken from the same set of measurements are likely to describe the full range of "true" resistivity values of the slice on which they were obtained.

Considering only the points actually measured on any slice, we can define R_{min} as the "true," but unknown, minimum resistivity and Y_{min} as the measured value corresponding to R_{min} . Corresponding definitions are taken for R_{max} and Y_{max} . We will ignore the guard factor, K , at this point; this is equivalent to assuming that measurements have been taken at the locations of actual minimum and maximum resistivity and that the only difference between measured and "true" values are due to measurement process errors. We will take T to be a "margin of error" and ask the general question, "When we quote Y_{max} and Y_{min} as defining the observed range, what is the probability that the range given by $Y_{max} + T$ and $Y_{min} - T$ covers the range of true values?"

This probability can be symbolically written as the simultaneous probability

$$P (Y_{max} + T > R_{max} \text{ and } Y_{min} - T < R_{min})$$

or

$$P (Y_{max} - R_{max} > - T \text{ and } Y_{min} - R_{min} < T) .$$

At the time we measure the value Y_{max} , it differs from R_{max} because of two types of errors: a short-term random measurement error, e_1 , and a short-term systematic error, β , with a fixed value for any one slice which comes from the distribution of long-term random measurement errors. Similarly, Y_{min} and R_{min} differ by the combination of β and e_2 . Therefore, in the previous probability statement, we can substitute for $Y_{max} - R_{max}$ and $Y_{min} - R_{min}$ to write:

$$P (\beta + e_1 > - T \text{ and } \beta + e_2 < T) .$$

The problem is to evaluate the simultaneous probability that for some margin of error, T , yet unspecified, the allowance made for errors of types β and e is sufficient to cover the value chosen for T . As explained in section 5.2, β and e are assumed to come from random distributions with standard deviations of 0.33% and 0.4%, respectively. Because β occurs in both terms with a common value which comes from the long-term random-error distribution, we must evaluate a convolution of probabilities, for all possible values of β :

$$\sum_b P(\beta = b) \cdot P(\beta + e_2 < T \text{ and } \beta + e_1 > - T |_{\beta = b}) ,$$

where b is any of the allowed values of β . Using the assumed Gaussian distributions for the errors, β and e , and a value for T of 1.56%, this probability can be readily evaluated by numerical integration. The result of integrating over all allowed values for β is a probability of 0.997.

Therefore, having allowed for the effects of random error to be up to 1.56% (three standard deviations) of the measured value, there is a probability of 0.997 that the observed maximum and minimum resistivities will cover the "true" maximum and minimum resistivities, for the set of locations measured. This is an idealized model: it does not account for the effects of thickness fluctuations or of additional excursions of resistivity on nonmeasured diameters. In an effort to account for these possibilities, a guard factor, K , with a value of 1.1 or 1.2 is also used. The probability statement can then be rewritten as:

$$P_r (Y_{max} + \frac{(K-1)}{2} * \text{Range} + T > R'_{max} \text{ and } Y_{min} - \frac{(K-1)}{2} * \text{Range} - T < R'_{min}) ,$$

where R'_{\max} and R'_{\min} do not necessarily occur at the locations of Y_{\max} and Y_{\min} . This probability cannot be directly evaluated since it depends not only on the measurement errors but also on the distribution of "true" values on the slice; this distribution is unknown. Plausibility arguments can be made, however, regarding the applicability of the ideal case probability to three classes of profiles:

- 1) For slices that are truly rotationally symmetric, no additional resistivity excursions exist on nonmeasured diameters, and the guard factor of 1.1 times the measured range is more than adequate to account for the effects of thickness fluctuations [8]. Moreover, since there are three measurements (at the center) or six measurements (at any other location) made of the minimum or maximum value, evaluating the contribution of the short-term error as 0.4% is to noticeably overstate its effect for such profiles. As a result, the appropriate probability for this case should be at least 0.997, as calculated based on a random error contribution of 0.4%.
- 2) For slices that are nearly symmetric, the contribution of the short-term error is still generally overstated, although there may be somewhat less than six chances at each off-center radial position for determining the maximum or minimum value. This overstatement of the short-term error should be sufficient to compensate for unrecognized errors due to thickness fluctuations. Evidence from tests run with three-, four-, and six-diameter profiles on slices with a variety of profile range values, both symmetric and nonsymmetric in shape, indicate that a guard factor of 1.1 is more than adequate to account for additional resistivity excursions. Again, the appropriate probability for these slices should be close to the 0.997 value.
- 3) For slices that are not symmetric, the maximum or minimum value generally occurs at only one measurement point. Hence, there is no safety margin in the short-term error related to having more than one available measurement; there is, however, some safety margin arising from assigning a worst-case value of 0.40% as the short-term standard deviation of the measurement process. In addition, the guard factor is set at 1.2 times the range for increased safety. Finally, the four- and six-diameter measurements, even on nonsymmetric slices, showed no meaningful increase in calculated range above the value determined from the three-diameter measurements. It is therefore expected that the probability of covering the range of true values on a nonsymmetric slice using 1) the observed maximum and minimum values, 2) a guard factor of 1.2, and 3) 1.56% to allow for random errors is near the calculated 0.997.

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