Impact of timestamp accuracy on the error budget of time-aware bridge

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Overview

- It seems that “IEC/IEEE 60802 D1.0 TSN Profile for Industrial Automation” table 15 and 16 specifications are contradicting each other in term of maximum error contribution and timestamp accuracy
- It seems that table 15 is not taking into account the number of timestamps required to compute the residence time and link delay measurement
- The following slides will elaborate on potential error sources as well as the number of timestamps required to compute PTP residence time and link delay measurement.

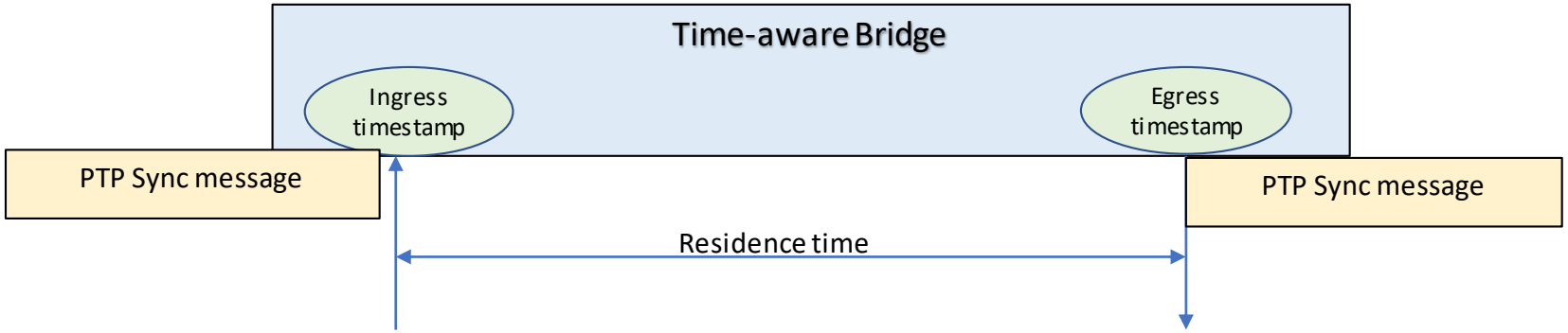
Assumptions:

- Maximum error represents worst case not the mean value

Notes:

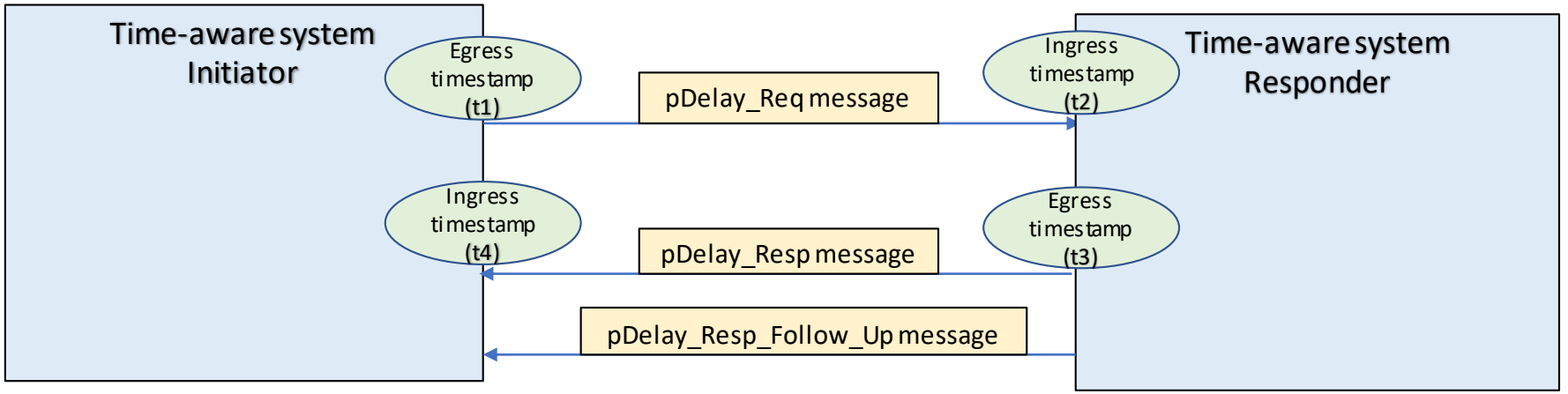
- For simplicity NeighborRateRatio and RateRatio are excluded from the calculations
- Some factors which may amplify link asymmetry effects are:
  - Cable length, link speed, media type, system design (i.e. timestamp point - PHY/MAC/FPGA/CPU) …
- Exclude impact of factors like temperature, components aging …
- Exclude impact of filters [IEEE802.1AS-REV D8.0 Sections 11.1.2, B.1.3.1, B.4]

PTP residence time computation



- The <residenceTime> corresponding to the time interval between the receipt of a Sync message on the ingress PTP Port and the transmission or retransmission of that Sync message on an egress PTP Port … [IEEE1588-2018 D1.4V4_11 Clause 16.10.4.4]
- PTP residence time computation requires 2 timestamps
- Suggestion: Maximum residence time error should be "(2 x timestamp_accuracy_ns) – 2_ns"

Peer-to-peer link delay computation



- The nominal value of the <meanLinkDelay> is computed as <meanLinkDelay> = [(t2 – t1) + (t4 – t3)]/2 = [(t2 – t3) + (t4 – t1)]/2 … [IEEE1588-2018 D1.4V4_11 Clause 11.4.1].
- Peer-to-peer link delay measurement requires 4 timestamps (t1, t2, t3 and t4)
- Suggestion: Maximum link delay error should be "((4 x timestamp_accuracy_ns) – 4_ns)/2"

Link asymmetry

- Logically link asymmetry manifest itself as
  - ingress_timestamp_point != egress_timestamp_point
- Multiple factors contribute to link asymmetry, such as
  - Propagation delay skew in physical media (i.e. media type, speed, length …)
  - Implementation of PHY/MAC layer(s) ingress and egress processing paths
  - System design, such as interaction of PHY/Switch/FPGA/CPU
- Profile should take into account the inaccuracy in the measurement of link asymmetry

Phase and frequency adjustment

- TSN standards such as IEEE802.1Qbv, IEEE802.1Qci (time-based policing) requires common sense of network time for proper operation
- TSN hardware (i.e. MAC layer) requires phase and frequency alignment for compliant operation (i.e. IEEE802.1Qbv)
- Only logical syntonization is not sufficient
- Profile should take into account the HW frequency/phase adjustment error

Conclusions

- Maximum residence time error (max_rt_err) should be “(2 x timestamp_accuracy_ns) – 2_ns”
- Maximum link delay error (max_ld_err) should be “((4 x timestamp_accuracy_ns) – 4_ns)/2”
- Should account for link asymmetry measurement error (link_asym_err)
- Should account for HW adjustment error (hw_adj_err)
- Error budget per time-aware bridge in ns should be
  - MAX { (max_rt_err + max_ld_err + link_asym_err + hw_adj_err), 25 }
- Computation of the number of hops in “IEC/IEEE 60802 D1.0 TSN Profile for Industrial Automation” table 14 should reflects the error budget per time-aware bridge

Thank you

Timestamp accuracy

- The resolution of the clock generating the timestamps required by PTP needs to be consistent with the desired accuracy. Note that this resolution contributes to the PTP variance … [IEEE1588-2018 D1.4V4_11 Annex A.5.4]
- The impact of PTP variance can be reduced and the accuracy improved by applying filters, e.g. an exponential averaging filter. Please see IEEE802.1AS-REV D8.0 Clause 11.1.2 and Annex B.4 for details

References

- IEC/IEEE 60802 D1.0
- Joint ITU-T/IEEE Workshop on The Future of Ethernet Transport. (Geneva, 28 May 2010). IEEE 802 1AS Network Performance - Geoffrey M. Garner
- ISPCS 2011 - Compensation of Asymmetrical Latency for Ethernet Clock Synchronization, Natasa Simanic, Reinhard Exel, Patrick Loschmidt, Thomas Bigler, and Nikolaus Kero
- IEEE1588-2018 D1.4V4_11 draft standard
- IEEE802.1AS-REV D8.0 draft standard
- http://www.ieee802.org/1/files/public/docs2018/60802-Steindl-Synchronization-0718-v02.pdf