DataGeneral

Field Engineer's
Reference Series

NOVA® 4/S AND 4/X

015-000095-02

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NOVA® 4/S AND 4/X

DataGeneral

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PREFACE

This manual is a guide to troubleshooting and repairing NOVA® 4/S and 4/X computers at the field replaceable unit level, commonly referred to as "board swapping".

It is organized around three major sections.

Part I is a product description, which:

- Introduces the major assemblies and explains how they interconnect
- Defines the field replaceable units
- Lists the related documentation
- Explains how to use the consoles.

Part II is devoted to troubleshooting. It explains both how to perform an initial checkout and how to repair a system that failed after normal operation.

The first chapters of Part II describe procedures for finding a failing field replaceable unit using:

- Visual checks
- The CPU's self-test feature
- Reliability and diagnostic test programs
- Simple manual tests.

These procedures, written in a "cookbook" manner, should allow the field engineer to repair most failures in a minimum period of time.

The latter chapters contain reference information about the operation of the major printed circuit boards, which will be useful when troubleshooting with an oscilloscope.

Part III provides detailed mechanical replacement procedures for each field replaceable unit.

WARNING: *The power supplies in these units have hazardous voltages on their printed circuit boards. They should be repaired only by trained service personnel.*

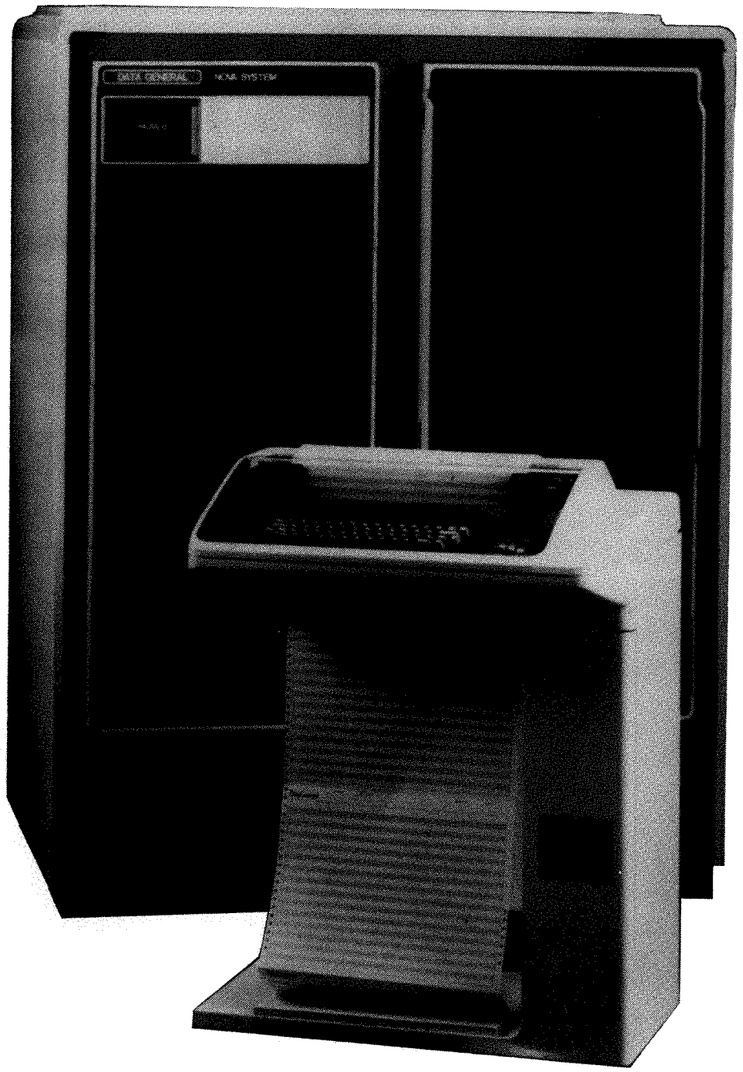

Figure 1.1. NOVA 4 COMPUTER SYSTEM

CONTENTS

PART I
PRODUCT DESCRIPTION

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

POWER SUPPLY

Each chassis has its own power supply, which is available with or without battery backup.

16-Slot Power Supply

The 16-slot power supply and distribution system consists of a VNR (voltage non-regulated) unit that is vertically mounted to the rear of the chassis and a slide-in power supply printed circuit board which plugs into the chassis' backpanel.

The VNR unit converts power from the ac supply line to non-regulated dc power, which it supplies to the power supply board via an internal cable. The internal cable also:

- Carries ac power from the VNR unit to the fan module
- Connects the front console switches and indicators to the backpanel
- Connects the power switch to the VNR unit.

When the battery backup option is present, the VNR unit contains a battery that supplies power to the battery backup circuits in the power supply board.

The power supply board regulates the dc voltages from the VNR unit and supplies the required voltages to the remainder of the system via the etch on the backpanel. It also generates the system clocks and supplies them to the system printed circuit boards via the backpanel.

As an added feature, the 16-slot power supply has a diagnostic test plug (located on the backpanel) that allows voltage margining under diagnostic program control. Use of this plug is described in Chapter 7. In normal operation, the diagnostic test plug must be inserted in the Run position.

CAUTION *The diagnostic test plug should be used only by authorized Data General field service representatives. Other use of this test plug may significantly degrade the system.*

For more information about the operation of the 16-slot power supply, refer to Part II, Chapters 6 and 9.

5-Slot Power Supply

The 5-slot distribution system and power supply resides on a single slide-in power supply printed circuit board. It converts power from the ac supply line to regulated dc voltages. When the battery backup option is present, the battery also resides on the power supply board.

The 5-slot power supply supplies the required dc voltages to the system printed circuit boards via the etch on the backpanel while it supplies ac power to the fan modules via the internal cable. The internal cable also:

- Connects the front console switches and indicators to the backpanel
- Connects the power switch to the power supply.

The 5-slot power supply also generates the system clocks and supplies them to the system printed circuit boards via the backpanel.

For more information about the operation of the 5-slot power supply, refer to Part II, Chapters 6 and 10.

FAN MODULES

Both the 16 and 5-slot fan modules reside on the left side of their respective chassis. They draw air from outside the cabinet and force it through the chassis. On the 16-slot chassis, the fan module, containing four fans, slides into the chassis from the front of the unit. On the 5-slot chassis, two fans mount on the inside of the chassis cover.

FRONT CONSOLE

The front console assembly mounts on the fan module in the 16-slot chassis and on the cover in the 5-slot chassis. It consists of three switches and three indicator lights. The switches allow the user to control basic functions such as power up/down, program load and reset while the indicator lights provide information concerning power status and the CPU's operating mode.

The remaining operator control functions are implemented by a virtual console which is described under the "CPU Board" below. Operator information for both consoles appears in Part I, Chapter 2.

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CHAPTER 1
INTRODUCTION TO NOVA® 4/S AND 4/X COMPUTERS

NOVA 4/S (standard) and NOVA 4/X (extended memory) computers incorporate a modular design plus self-diagnostic capabilities that facilitate maintenance and provide high reliability. In most cases, the user can identify the failing field replaceable unit by running simple tests, thus minimizing repair time.

Both computers are identical with the exception of their memory support capability. The NOVA 4/S computer supports up to 64K bytes of dynamic RAM (random access memory) while the 4/X computer contains a CPU-resident Memory Management and Protection Unit (MMPU) that allows it to support up to 256K bytes of dynamic RAM.

NOVA 4 computers are rack-mounted in NEMA-standard equipment cabinets. These cabinets also provide housing for NOVA line peripheral equipment, such as magnetic tape drives and rack-mounted disc drives.

Both computers consist of the following basic modules, which are tailored to the user's selected configuration.

- Computer chassis
- Power supply
- Fan module
- Front console
- Printed circuit boards
  - CPU
  - Dynamic RAM
  - Floating point unit (optional in 16-slot chassis)

CHASSIS

Two computer chassis are available to NOVA 4 users: 5 and 16-slot. Each has its own backpanel printed circuit board with connectors for the system printed circuit boards. These boards, including a slide-in power supply board (5 or 16-slot version), are inserted from the front of the chassis, which is easily accessed by removing the NOVA 4 front panel attached to the equipment cabinet. Access to the backpanel is via the rear door of the equipment cabinet (and the VNR unit, described below, under "16-Slot Power Supply").

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16-Slot Chassis

This chassis holds up to sixteen 15-inch by 15-inch printed circuit boards plus the 16-slot power supply and fan module.

Bus termination for the backpanel is provided by a resistor fence, which is soldered into the backpanel below slot 1, and two bus terminator cards, one for the A side and one for the B side. The bus terminator cards push onto the backpanel pins of the highest slot containing a memory board.

The 16-slot chassis supports up to twenty I/O paddleboards, which are vertically mounted at the rear of the unit.

Figures 1.2 and 1.3 illustrate the 16-slot chassis.

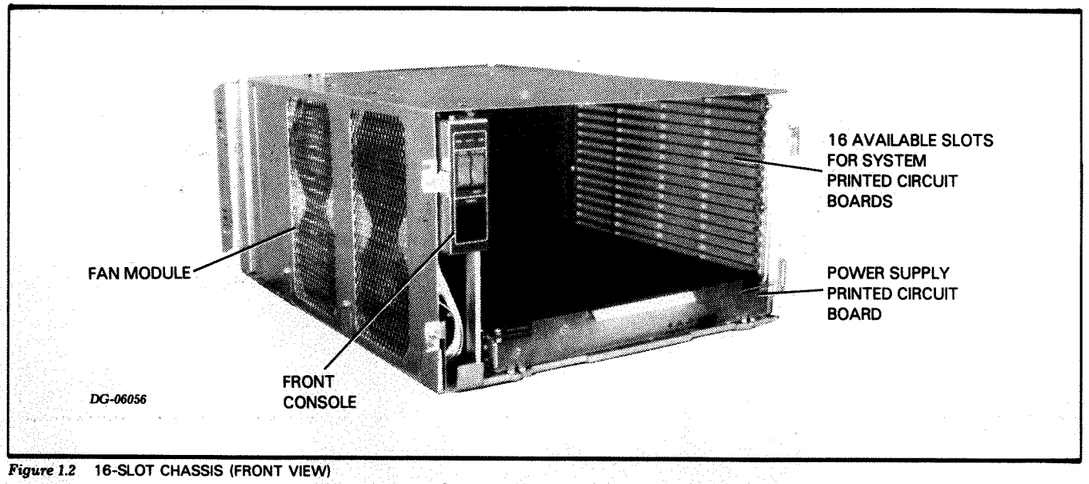

Figure 1.2 16-SLOT CHASSIS (FRONT VIEW)

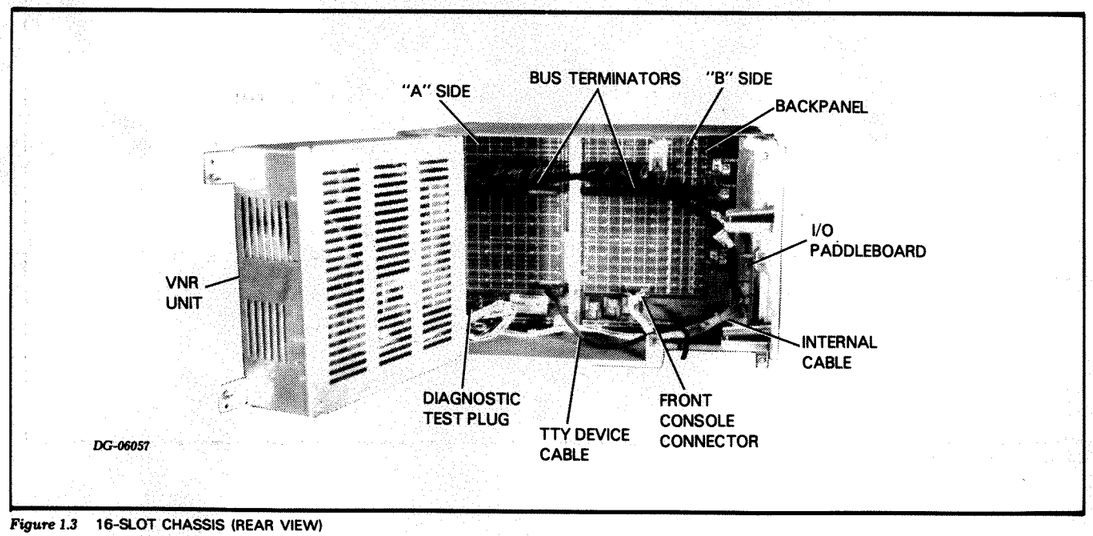

Figure 1.3 16-SLOT CHASSIS (REAR VIEW)

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5-Slot Chassis

This chassis holds up to five 15-inch by 15-inch printed circuit boards plus the 5-slot power supply and fan modules.

Bus termination for the backpanel is provided by a resistor fence (soldered into the backpanel above slot 5) and two bus terminator cards, one for the A side and one for the B side. The bus terminator cards push onto the backpanel pins of slot 2.

The 5-slot chassis supports up to ten I/O paddleboards. Like the 16-slot chassis, the paddleboards are vertically mounted at the rear of the unit.

Figures 1.4 and 1.5 illustrate the 5-slot chassis.

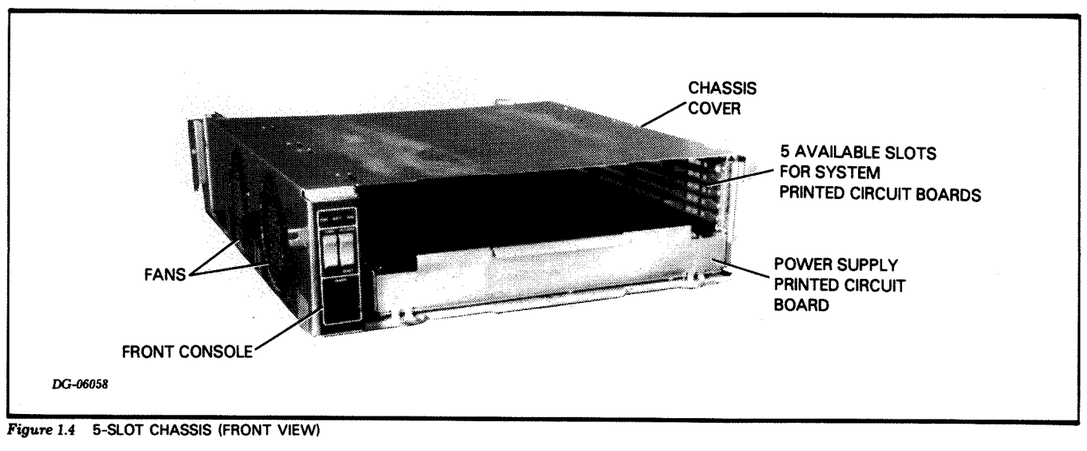

Figure 1.4 5-SLOT CHASSIS (FRONT VIEW)

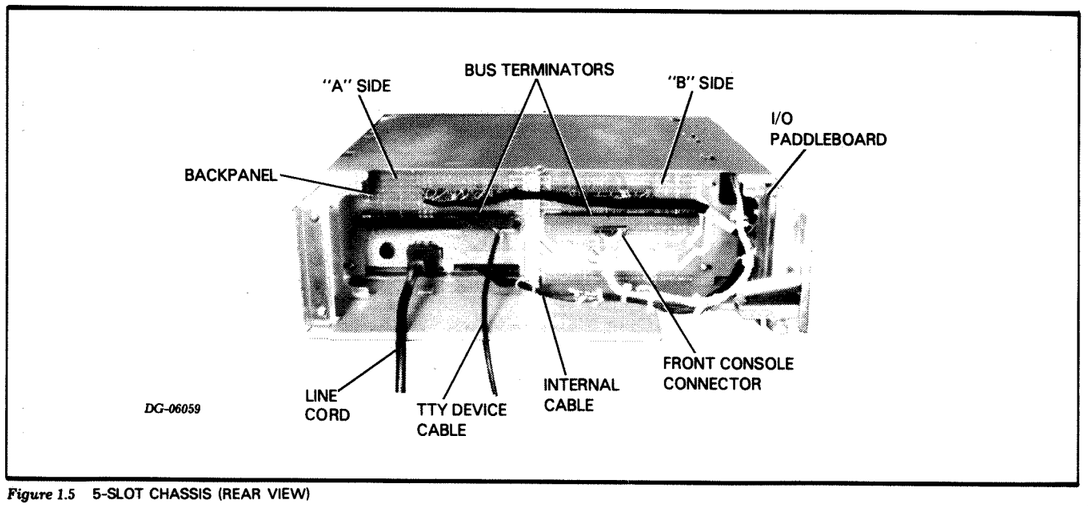

Figure 1.5 5-SLOT CHASSIS (REAR VIEW)

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FIELD REPLACEABLE UNITS

Figures 1.9 and 1.10 show the field replaceable units and their interconnections. Tables 1.1 and 1.2 list their Data General assembly numbers.

Table 1.1
16-SLOT FIELD REPLACEABLE UNITS

Assembly	Description
005-12067	NOVA 4/X CPU with Multiply/Divide option
005-12785	NOVA 4/X CPU without Multiply/Divide option
005-12786	NOVA 4/S CPU with Multiply/Divide option
005-12787	NOVA 4/S CPU without Multiply/Divide option
005-12128	32K byte (16K word) dynamic RAM board
005-12132	64K byte (32K word) dynamic RAM board
005-12136	128K byte (64K word) dynamic RAM board
005-12140	256K byte (128K word) dynamic RAM board
005-12373	Floating point unit board
005-12073	Backpanel board
005-14135	Console PCB assembly
005-12429	VNR unit
005-12064	Power supply board with battery backup
005-12061	Power supply board without battery backup
005-12076	Fan module
115-00163	Fan assembly
005-12438 or 005-15361	Bus terminator, "A" side
005-12439	Bus terminator, "B" side
005-12489	Internal cable
005-07093	12V battery

Table 1.2
5-SLOT FIELD REPLACEABLE UNITS

Assembly No.	Description
005-12067	NOVA 4/X CPU with Multiply/Divide option
005-12785	NOVA 4/X CPU without Multiply/Divide option
005-12786	NOVA 4/S CPU with Multiply/Divide option
005-12787	NOVA 4/S CPU without Multiply/Divide option
005-12128	32K byte (16K word) dynamic RAM board
005-12132	64K byte (32K word) dynamic RAM board
005-12136	128K byte (64K word) dynamic RAM board
005-12140	256K byte (128K word) dynamic RAM board
005-12402	Backpanel board
005-14135	Console PCB assembly
005-12406	Power supply board with battery backup
005-12404	Power supply board without battery backup
005-12398	Fan assembly
005-13932	Bus terminator, "A" side
005-13933	Bus terminator, "B" side
005-13470	Internal cable
005-12873	6V battery

RELATED DOCUMENTATION

A list of documentation for NOVA 4/S and 4/X computers appears in Table 1.3.

Table 1.3
DOCUMENTATION SUMMARY

Affected Assemblies	DGC No.	Description
NOVA 4/S AND 4/X COMPUTERS	014-000617	NOVA 4 Programmer's Reference Manual
	015-000031	Interface Designer's Reference, NOVA and ECLIPSE Line Computers
	015-000056	Diagnostic Operating System Technical Manual
	015-000082	DTOS Summary
16-Slot NOVA 4/S or NOVA 4/X	010-000213	Installation Data Sheets, NOVA 4 16-Slot
5-Slot NOVA 4/S or NOVA 4/X	010-000212	Installation Data Sheets, NOVA 4 5-Slot
CPU	001-001624	CPU Schematic
	016-000677	CPU Illustrated Parts
Dynamic RAM	001-001229	BBU Memory Schematic (All Sizes)
	016-000671	32/128K Word BBU Memory Illustrated Parts
	016-000674	16/64K Word BBU Memory Illustrated Parts
Floating Point Unit	001-001573	FPU Schematic
	016-000865	FPU Illustrated Parts
Power Supply PCB 16-Slot	001-001524	Power Supply Schematic
	016-000688	Power Supply Illustrated Parts (Including Battery Backup)
VNR Unit 16-Slot	001-001523	Power Supply VNR Card Schematic
	016-000670	Power Supply VNR Card Illustrated Parts
Power Supply PCB 5-Slot	001-001616	Power Supply Schematic
	016-000861	Power Supply Illustrated Parts
Backpanel 16-Slot	001-001563	Backpanel Schematic
	016-000675	Backpanel Illustrated Parts
Backpanel 5-Slot	001-001619	Backpanel Schematic
	016-000696	Backpanel Illustrated Parts
Front Console PCB	001-001585	Front Panel Schematic
	016-000661	Front Panel Illustrated Parts
Internal Cable 16-Slot	001-001607	DGC System Wiring Diagram
Internal Cable 5-Slot	001-001637	DGC JR Wiring Diagram
I/O Paddleboards		
005-012472	008-003294	Wire List (General Purpose I/O)
005-012751	008-002599	Wire List (External I/O Bus)
005-012765	008-002570	Wire List (For ULM Models 4241, 4241A, 4242, 4243)
005-012476	008-003287	Wire List (Model 8315 Bus Repeater)
005-012590	008-003301	Wire List (DCU 50, Models 4250, 4254)
005-012473	008-003288	Wire List (Asynchronous Interfaces, Models 4007, 4010, 4023, 4075, 4077, 4078)
005-012585	008-003300	Wire List (MCA, Model 4206)

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PRINTED CIRCUIT BOARDS

While most NOVA 4/S and 4/X computers consist of a variety of printed circuit boards, two basic types of boards comprise the core of NOVA 4/S and 4/X computers: the CPU and memory (dynamic RAM). An optional floating point unit board is available with 16-slot configurations.

Figures 1.6 and 1.7 show the slot assignments for each board in the 16-slot chassis and the 5-slot chassis, respectively.

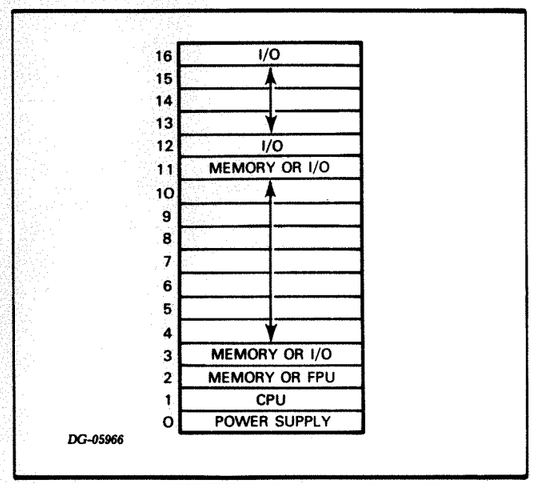

Figure 1.6 SLOT ASSIGNMENT DIAGRAM, 16-SLOT CHASSIS

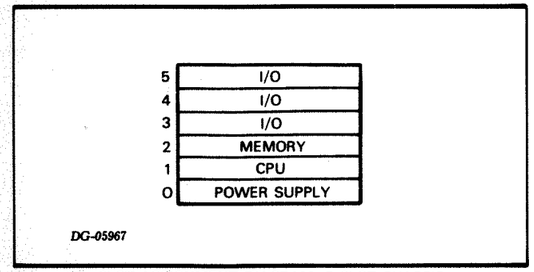

Figure 1.7 SLOT ASSIGNMENT DIAGRAM, 5-SLOT CHASSIS

CPU Board

The basic CPU board of both computers is the same with the exception of the Memory Management and Protection Unit which resides on the NOVA 4/X CPU board only. Both boards may contain the multiply and divide option.

The basic CPU board contains:

- Central processing unit (CPU)
- Full-duplex, asynchronous communications interface
- Programmable real-time clock
- Virtual console, residing in 512 words of ROM (read only memory) with 32 words of scratchpad RAM.

CPU

The CPU is a 16-bit microprogrammed processor, which means its data paths are controlled by microinstructions stored in internal ROM. It incorporates the full NOVA 16-bit architecture, including four 16-bit accumulators and hardware stack and frame pointers. NOVA 4 CPUs execute an extended NOVA 3 instruction set, augmented with load and store byte instructions and, optionally, signed multiply and divide instructions.

It operates in two modes: run and console.

In run mode, the CPU executes instructions stored in main memory (dynamic RAM). To increase throughput and minimize response time, it uses an integral prefetching processor in this mode to fetch and store up to 11 instructions ahead of the instruction currently being executed.

In console mode, the CPU executes instructions stored in the resident virtual console ROM.

On power up or after a power fail when battery backup is not present, the CPU runs a self-test. This test:

- Exercises basic CPU functions
- Checks the first 32K bytes (16K words) of main memory
- Checks the operation of the device connected to the resident asynchronous interface.

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On completion of the self-test, the CPU enters console mode and is ready to accept user commands. For more information about the self-test, refer to Part II, Chapter 5.

As shown in Figure 1.8, the CPU communicates with the dynamic RAM board(s) via memory control lines and two major system buses, **MEMIN** <19, 0-15> and **MEMOUT** <0-15>. The **MEMIN** bus is a 17-bit wide memory address/data bus. It carries 17-bit addresses and 16-bit data words from the CPU to memory. The **MEMOUT** bus is a 16-bit wide data bus. It carries 16-bit data words from memory to the CPU.

The CPU communicates with I/O controllers, other than the CPU-resident asynchronous interface and real-time clock, using the standard 48-line NOVA I/O bus.

It communicates with the optional floating point unit via both the I/O and memory buses as well as dedicated floating point control and status lines.

Asynchronous Interface

This is a programmed I/O controller containing both a transmitter and receiver. It allows full-duplex communications between a serial, asynchronous terminal and the CPU via either a 20mA current loop or an EIA RS-232C communications line connected to the CPU via the backpanel.

In addition to standard send/receive terminals, the asynchronous interface supports both an automatic send/receive terminal (i.e., a terminal equipped with a paper tape reader) as well as a 60cps DASHER terminal printer.

When the CPU is in run mode and unlocked (as indicated by the position of the front console Lock switch), a Break character received by the interface interrupts the executing program and places the CPU in console mode.

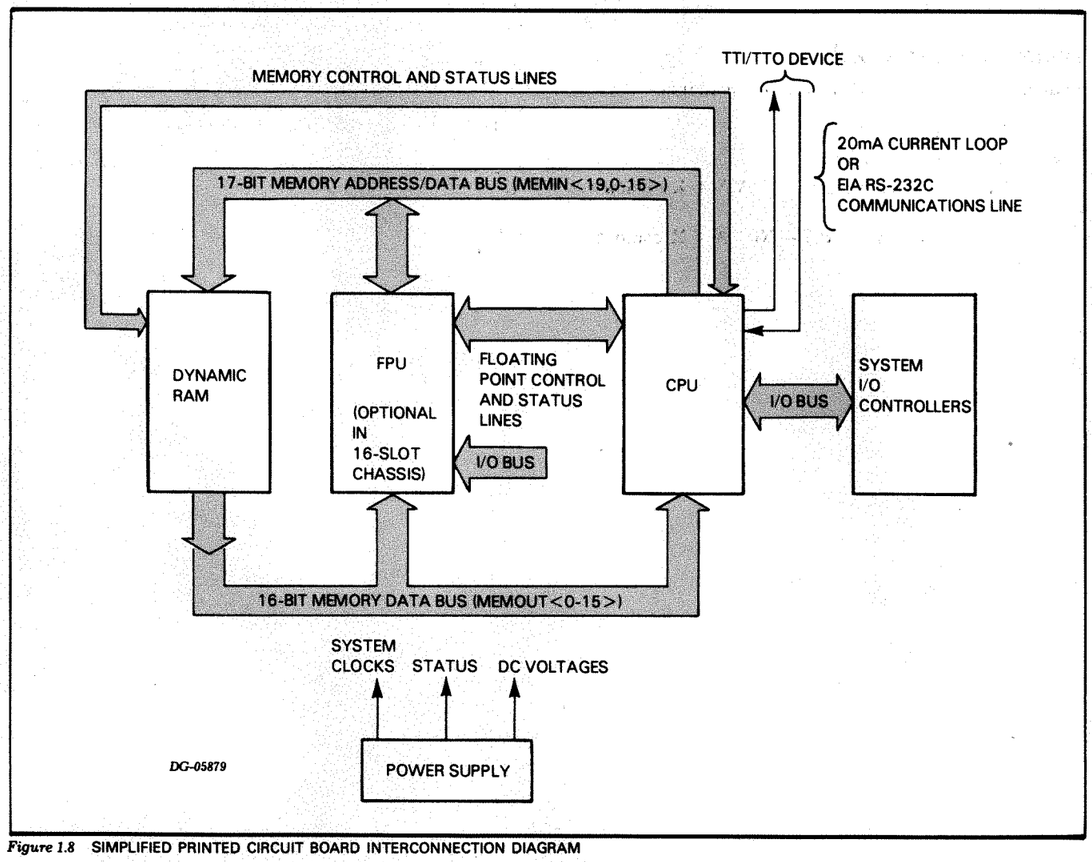

Figure 1.8 SIMPLIFIED PRINTED CIRCUIT BOARD INTERCONNECTION DIAGRAM

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Real-Time Clock

The real-time clock interface can supply program interrupt requests at one of four program-selectable frequencies: 10Hz, 100Hz, 1000Hz or power line frequency.

Virtual Console

The virtual console allows a user whose terminal is connected to the resident asynchronous interface to inspect and modify the system's state and aid program debugging.

It provides the user with the ability to:

- Stop, start and continue program execution
- Examine and/or alter CPU registers and memory locations
- Initiate program load sequences.

For more information concerning the CPU board, refer to Part II, Chapter 11.

Dynamic RAM Boards

Four sizes of dynamic RAM boards are available:

- 32K bytes (16K words)
- 64K bytes (32K words)
- 128K bytes (64K words) -- NOVA 4/X computers only
- 256K bytes (128K words) -- NOVA 4/X computers only

Each board contains integral refresh logic and each is organized around four modules of memory elements which are 4-way interleaved. The 32K byte and 64K byte boards contain 4,096 by 1 bit, N-channel MOS memory elements while the 128K byte and 256K byte boards contain 16,384 by 1 bit memory elements.

Memory read/write cycle time is 400ns. However, due to the modular organization of the memory elements and the presence of four timing generators, each dedicated to a particular module, memory operations can be initiated every 100ns, providing the same memory module is not addressed within the 400ns cycle time.

For more information concerning the operation of the dynamic RAM boards, refer to Part II, Chapter 12.

Floating Point Unit Board

This optional board is available with 16-slot NOVA 4/S and 4/X computers only. It executes the NOVA 3 floating point instruction set with the exception of the diagnostic instructions, which are replaced by microdiagnostics stored in internal ROM.

As shown in Figure 1.8, the floating point unit (FPU) is governed by information provided by the CPU and carried to the FPU by dedicated control lines and the NOVA I/O bus. All data transfers take place between the CPU, the floating point unit and the dynamic RAM board(s) via the two memory buses, **MEMIN** and **MEMOUT.**

For more information concerning the operation of the floating point unit, refer to Part II, Chapter 13.

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VIRTUAL CONSOLE

The virtual console (VC) allows you to interact with the computer through the system terminal connected to the CPU's on-board asynchronous communications interface. Simple commands which you enter on the terminal keyboard allow you to examine and/or modify processor registers or memory locations, start, stop, and continue program execution, and initiate a program load from a selected device.

On power up, the computer performs a self-test. After a successful completion of the self-test, the following information is typed on the terminal:

```
OK
!000000
!
```

"OK" followed by "!" indicates that the self-test ran successfully. This, in turn, is followed by the contents of the program counter, which is all zeroes on power-up. The next "!" is the VC prompt; it tells you that VC is ready and at your service.

In addition to power-up, VC is entered when:

- A HALT instruction is executed,
- The RESET switch on the front console is pressed and the front console is unlocked; or
- The Break key on the system terminal is pressed and the front console is unlocked.

Under these conditions, the contents of the program counter when VC was entered is typed. This is followed by the "!" VC prompt. For example, if the program counter was at location 2077 when VC was entered, the following would be typed:

```
002077
!
```

Cells

VC operates on *cells*. A cell is either a memory location (memory cell) or an internal register (internal cell) such as an accumulator. Each internal register that is accessible by VC is assigned an internal cell number. These are listed in Table 2.1.

Table 2.1
INTERNAL CELLS

Internal Cell #	Internal Register
0-3	The contents of the accumulators AC0 through AC3 respectively.
4	Return address (the contents of the program counter when VC was entered).
5	Stack pointer
6	Frame pointer
7	Interrupt enable flag status bit: 0 = interrupts off 1 = interrupts on
10	MMPU status bits before VC was entered (NOVA 4/X only): BIT — MEANING WHEN 1 0 — Program mapping enabled 1 — Data channel mapping enabled 2 — Program map inhibited 3-8 — Reserved for future use 9 — Single cycle write protect enable 10 — Single cycle select (0 = A, 1 = B) 11 — Auto increment/decrement protect enable 12 — Defer protect enable 13 — I/O protect enable 14 — Write protect enable 15 — Program map select (0 = A, 1 = B)
11	Data switch register: Replaces the conventional console data switches. When the system is in run mode (i.e., not in VC mode) and a READS instruction is executed, the 16-bit contents of this register are read by the CPU.
12	Value of the carry bit

In order to examine or modify any cell, you must *open* it. Opening a cell causes its contents to be printed, in octal, on the terminal.

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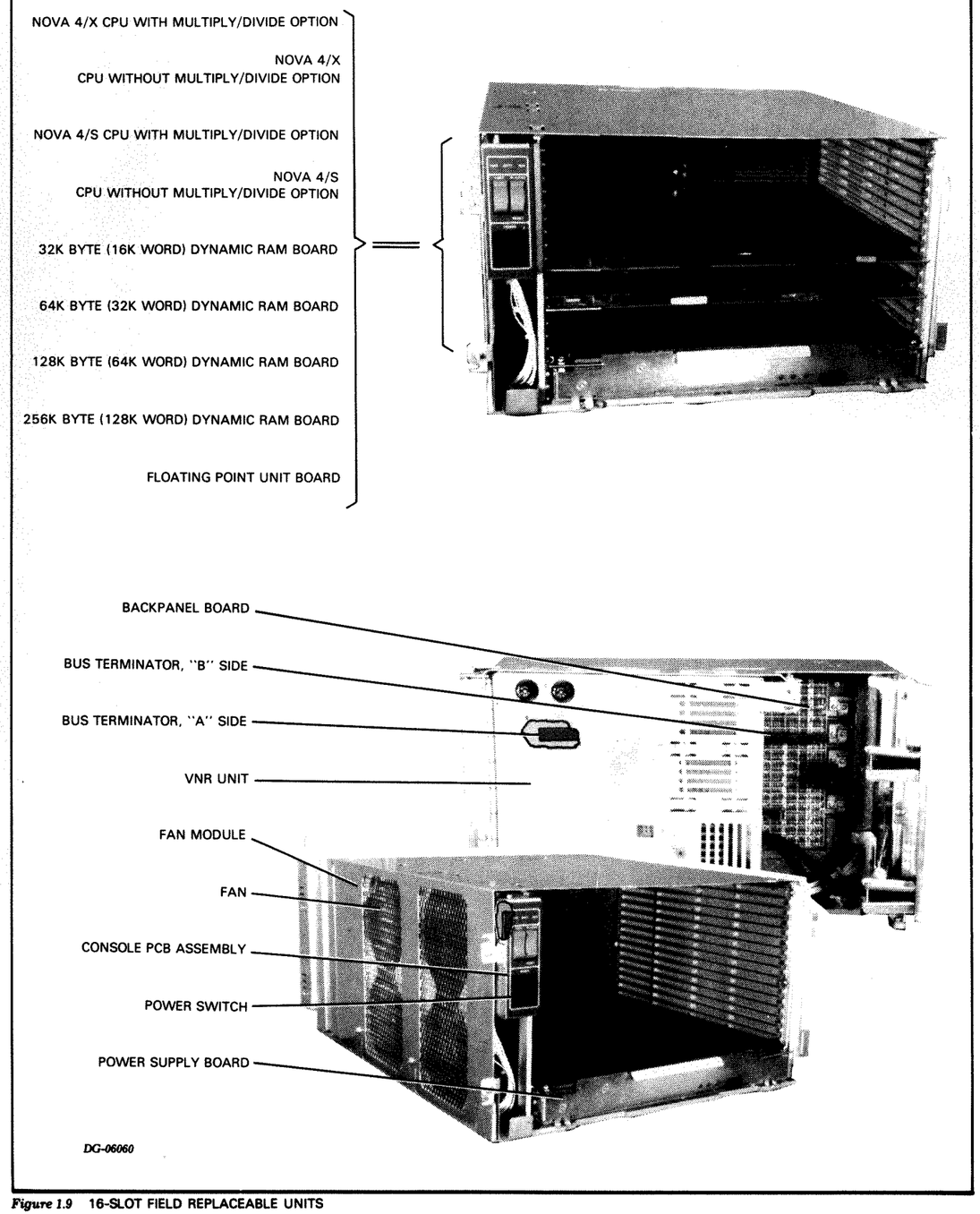

Figure 1.9 16-SLOT FIELD REPLACEABLE UNITS

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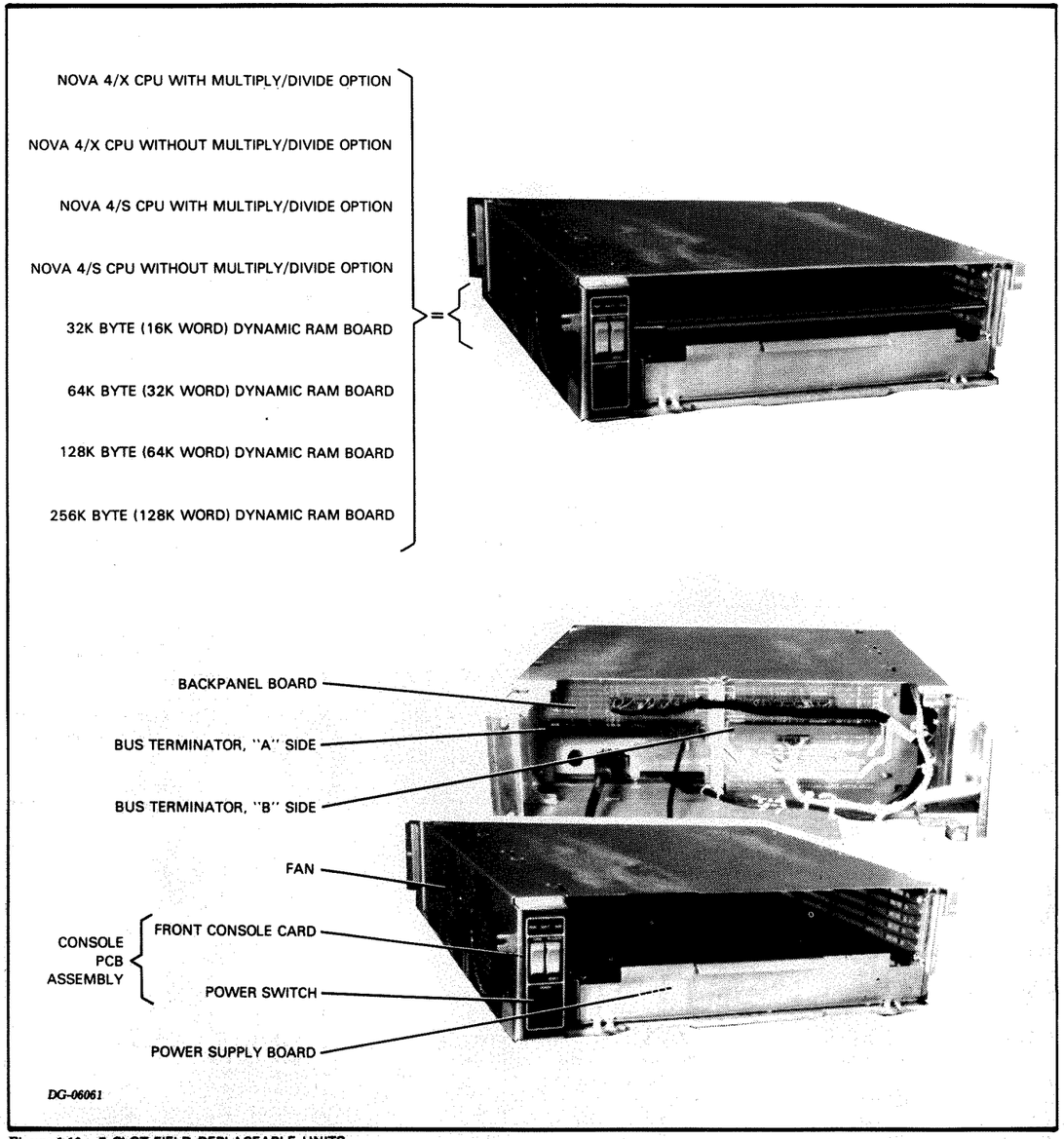

Figure 1.10 **5-SLOT FIELD REPLACEABLE UNITS**

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CHAPTER 2
HOW TO USE THE CONSOLES

The NOVA 4 computers contain two consoles: a *front* console and a *virtual* console. These are described below.

FRONT CONSOLE

The front console is located on the upper-left corner of the front panel. It consists of three switches and three lights, defined below.

Switches

POWER - Powers up and powers down the system.

PL/LOAD-RESET - When this switch is pushed to the PL/LOAD position, the CPU performs a program load from the device whose device code is jumpered on the CPU board. (For jumpering information, see Installation Data Sheets or Part III, Chapter 14, "CPU Board Replacement".)

When this switch is pushed to the RESET position, the CPU performs a system reset and enters virtual console mode, described below.

LOCK - When this switch is in the LOCK position, the other two switches, described above, are disabled. Additionally, the LOCK switch enables auto restart after a power fail when the battery backup is present, while inhibiting access to the virtual console via a Break character transmitted by the system terminal.

On a 16-slot system, if this switch is in the LOCK position, the system cannot be powered down (i.e., the power switch is disabled). On a 5-slot system, if this switch is in the LOCK position and the power switch is placed in the OFF position, the system will go into battery backup mode if that option is present. If the 5-slot system does not contain the battery backup option, the system will be powered down.

Lights

PWR - When illuminated, it indicates that the system is powered up and the voltages are within operating specifications.

BATT - When illuminated, it indicates that the system is running on battery-backup power. This is usually the result of a power failure.

RUN - When illuminated, it indicates that the system is in run mode. This light is out when the system is in virtual console mode.

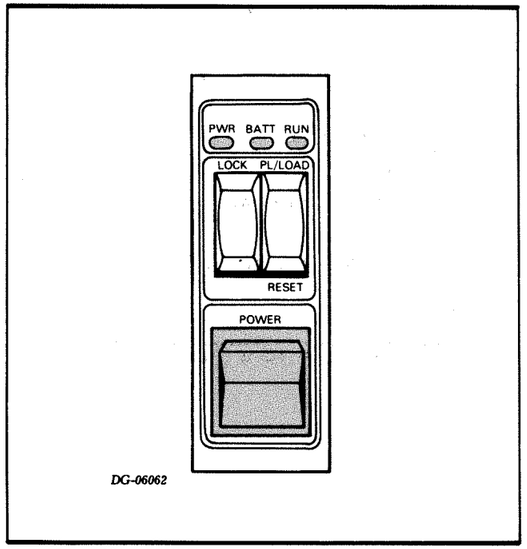

Figure 2.1 FRONT CONSOLE

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Cell Commands

To open a cell, use one of the commands listed in Table 2.2. VC will respond only to octal numbers and upper case letters. In the table, the term *current cell* means the last cell that you opened.

When you open a memory cell, VC interprets the address as a 17-bit physical address. You do not have to type leading zeroes. All you have to type is the physical address in octal representation. For example, if you want to open location 5, type 5/. If you want to examine the top location of a NOVA 4/X system which contains 256K bytes of memory, type 377777/.

Table 2.2
CELL COMMANDS

Command	Function
*n*A	Open the internal cell whose internal cell number is equal to *n*. (Refer to Table 2.1 for the internal cell numbers.)
n/	Open the memory location whose address is equal to the octal number *n*: *n* is a 17-bit address.
(Carriage Return)	Close the current cell, and open the next consecutive cell.
(Line Feed or New Line)	Close the current cell, but do not open another.
/	Close the current cell and open the memory cell whose address is equal to the contents of the current memory or internal cell.

Once you have opened a cell, you may change its contents by simply typing (in octal) the number whose value is to be placed in the cell. Terminate the expression with a Carriage Return, Line Feed or New Line. Note that if you type Carriage Return the next cell will also be opened. This is convenient when you need to enter data into several consecutive locations.

Function Commands

Table 2.3 below lists the VC function commands. All commands must be typed in octal numbers and upper case letters.

VC has two commands to start program execution. Typing **P** starts program execution at the location specified by internal cell number 4 (the return address). You can also start program execution by typing *n***R.** In this case, the CPU issues an I/O Reset command, clears the MMPU, and starts program execution at the location specified by the octal number *n*.

Typing **I** causes the CPU to issue an I/O Reset command and clear the MMPU.

Table 2.3
FUNCTION COMMANDS

Command	Function
P	Starts program execution at the memory location specified by the contents of internal cell number 4 (See Table 2.1).
*n***R**	Issues an I/O Reset; clears the MMPU (NOVA 4/X only), and starts program execution at the memory location specified by the octal number *n*.
I	Issues an I/O Reset, and clears the MMPU (NOVA 4/X only).
*n***L**	Performs a program load from the device whose device code is equal to *n*. Bit 0 of *n* is a 0 for a low-speed device, and is a 1 for a high-speed device.
F	Performs a DG field service cassette bootstrap load (for DGC use only).
K	Cancels the entire line just typed, and prints a question mark (?).

You can program load from an I/O device by typing *n***L** where *n* is the device code, in octal, of the I/O device to be used. Bit 0 of *n* should be a 1 if the I/O device is high-speed, and a 0 if the I/O device is low-speed. For example, if the program load device is a high-speed 6060 disc drive whose device code is 27, you would type the following:

100027L

You can perform a Data General field service cassette bootstrap load by typing **F.**

Virtual Console Errors

If you type a character that VC does not recognize, it will print a **?** followed by a New Line. If you wish to cancel an entire line you just entered, type a **K.** In this case VC will respond with a **?** followed by a New Line.

If you attempt to open a non-existent memory cell, the 16-bit contents of the cell printed in octal on the terminal will be all 1's. You can verify that this location does not exist by entering a new value containing 0's in the cell and then re-opening it. If it still contains all 1's, the location is non-existent.

If you attempt to open a non-existent internal cell, the contents of the cell printed on the terminal will be random and meaningless data.

PART II
TROUBLESHOOTING

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CHAPTER 3
INTRODUCTION TO TROUBLESHOOTING

Part II of this manual consists of 11 chapters (Chapters 3 through 13), which contain two types of information: troubleshooting procedures and reference information. Both are intended for use during:

- Initial checkout of a new installation or addition to an existing system
- Repair of an existing system

While these situations are different, many of the procedures required to perform both initial checkout and repair are the same, as shown in the troubleshooting flowchart, Figure 3.1. This flowchart leads you through a logical sequence of fault isolation, referencing Chapters 4 through 8. These chapters contain step-by-step procedures for detecting faulty assemblies and checking the reliability of the system. (Actual replacement procedures are outlined in Part III, Chapter 14.)

Chapters 9 through 13 provide an operational overview of the major system printed circuit boards. These chapters will better acquaint you with NOVA 4/S and NOVA 4/X computers and will be useful when you are required to troubleshoot using an oscilloscope.

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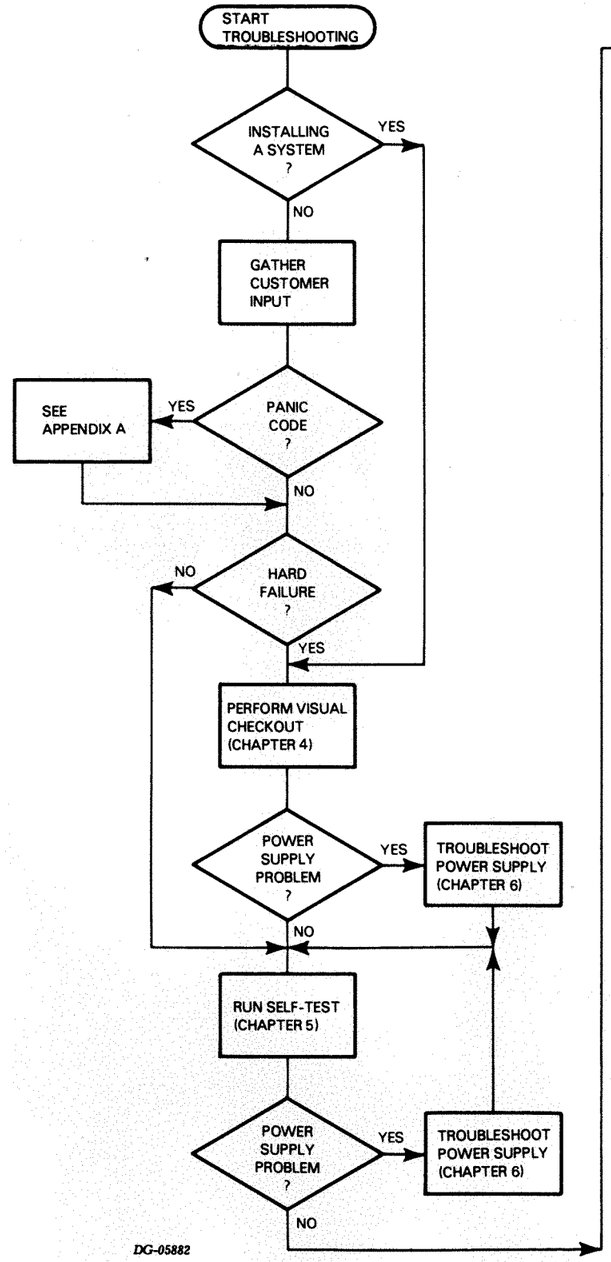

Figure 3.1 TROUBLESHOOTING FLOWCHART

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PRE-SITE INFORMATION

Before going to the customer's site, check the list below and learn the customer's configuration, if possible. This will help to ensure that you have the appropriate field replaceable units (FRUs) with you on arrival.

- Chassis: 16 or 5-slot
- CPU type
- Memory: number and size
- Battery backup option
- Floating point unit
- Terminal used as system console
- Other peripherals

Also, if you are going to repair a failing unit, try to get information from the customer that may give you a clue to the failing FRU.

CONFIGURATION CHART

Each system is shipped with a configuration chart which should reflect its configuration. Attach the chart to the rear door (outside) of the cabinet. Whenever you or anyone else reconfigures or retailors the system, update the chart to reflect the changes.

INITIAL CHECKOUT

If you are performing an initial checkout of a new installation, start with Chapter 4 and follow the steps outlined in the troubleshooting flowchart.

REPAIR

If you are servicing a failing system, the type of failure determines the procedures you will use to troubleshoot it. Thus, it is important to ask the customer the following questions:

1. Was the computer operating properly before the failure?
2. Is the failure a hard or intermittent one?
3. Did the operating system generate any panic codes?
4. Can the computer successfully complete the self-test?
5. Was the failure detected by reliability and/or diagnostic testing?
6. Was the failure detected while running user programs?

With the answers to these questions, you are now ready to follow the steps indicated in the troubleshooting flowchart.

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CHAPTER 4
VISUAL CHECKOUT

You should perform the visual checkout whenever you initially check out a system (or add to a system) or repair an existing system.

WARNING: *The VNR unit (16-slot only) and the slide-in power supply board (both chassis) carry dangerously high voltages. Turn the power off before removing any unit.*

Visually check out the system using the following procedure. Try to correct any simple problems you find.

1. Turn power off.
2. Check the configuration chart on the rear door (outside) of the cabinet to find out what the system contains and how it is tailored.
3. Open the rear cabinet door and unplug the ac line cord from the cabinet.
4. If you are repairing a system, check the ac line fuses and replace them if they are blown. The 16-slot power supply has two 15 Amp line fuses which screw into the rear of the VNR unit (see Figure 4.1). The 5-slot power supply has one 7 AMP line fuse which screws into the rear of the power supply board and extends through a cutout in the backpanel (see Figure 4.2).

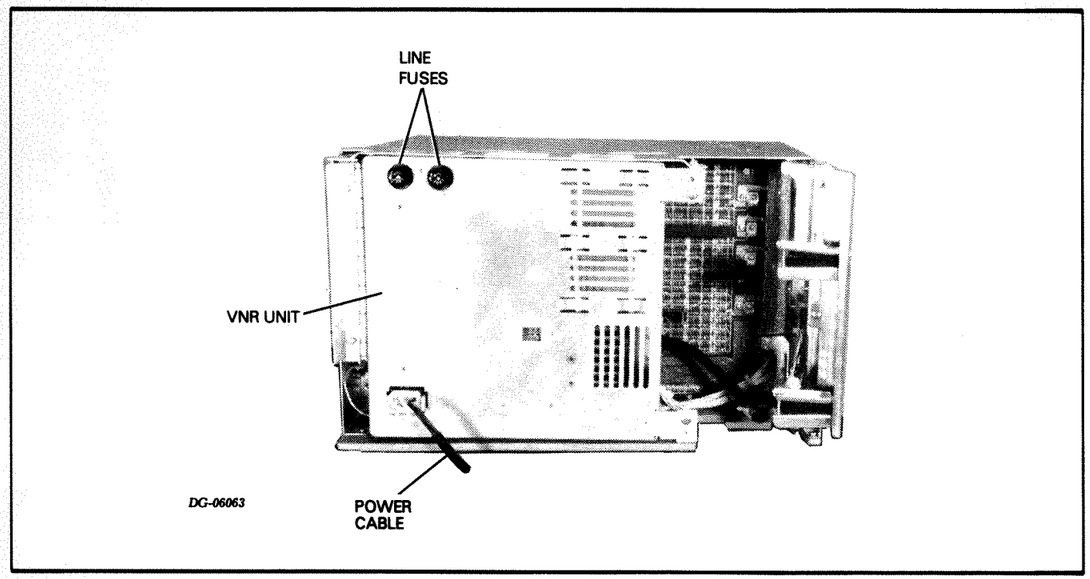

Figure 4.1 LINE FUSES FOR 16-SLOT POWER SUPPLY

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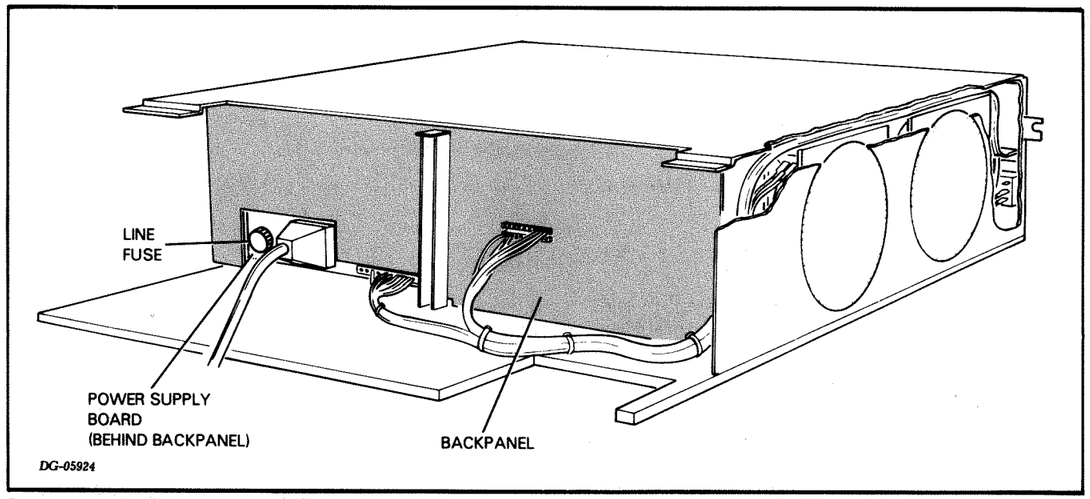

Figure 4.2 LINE FUSE FOR 5-SLOT POWER SUPPLY

5. On a 16-slot chassis:

   a. Swing the VNR unit away from the backpanel (see "VNR Unit Replacement," Chapter 14).

   b. Check for bent pins which cause shorts. Straighten any bent pins.

   c. Make sure the diagnostic test plug is inserted with the RUN label up (see Figure 4.3). If it is not, remove the plug, turn it over, and reinsert it with the RUN side up.

   d. Make sure none of the connectors to the backpanel or to the paddleboards are hanging loose.

   e. If you are repairing a system which you suspect has had an I/O problem since installation:

      - Make sure the priority jumpers are inserted as described in the installation data sheets.
      - Make sure the correct paddleboards are used and connected to the proper backpanel slots (see installation data sheets).

   f. Reposition the VNR unit (see "VNR Unit Replacement," Chapter 14).

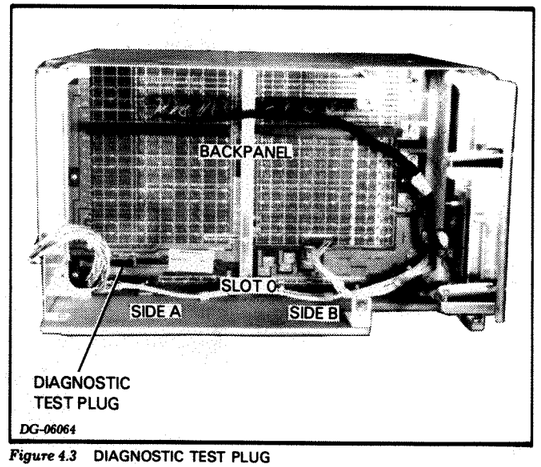

Figure 4.3 DIAGNOSTIC TEST PLUG

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6. On a 5-slot chassis:

   a. Check for bent pins which cause shorts. Straighten any bent pins.

   b. Make sure none of the connectors to the backpanel or to the paddleboards are hanging loose.

   c. If you are repairing a system which you suspect has had an I/O problem since installation:

      - Make sure the priority jumpers are inserted as described in the installation data sheets.
      - Make sure the correct paddleboards are used and connected to the proper backpanel slots (see installation data sheets).

7. Plug the ac line cord back into cabinet and close the rear cabinet door.

8. Remove the front panel (see "Front Panel Replacement," Chapter 14).

9. If you are installing a system or repairing a system which has never operated normally:

   a. Remove each printed circuit board, except the power supply board, and make sure it is tailored properly (see "CPU Board Replacement" or "Memory Board Replacement," Chapter 14, or the appropriate I/O device documentation).

   b. If necessary, update the configuration chart on the rear (outside) of the cabinet door to reflect the proper tailoring.

10. Check the fans as follows:

    a. If you are servicing a 16-slot chassis with boards in slots 6 and 15, remove them. If you are servicing a 5-slot chassis with a board in slot 4, remove it.

    b. Turn the power on.

    c. Look at the left side of the chassis through the open slots and see if all the fans are running. You may need to use a flashlight. If all the fans are running, continue the visual checkout; otherwise, proceed as follows:

       - If some, but not all, of the fans are running, replace the faulty fans and, make sure the cable connectors to the fans and the console PCB assembly are seated securely. (See "Fan and Fan Module Replacement for 16-Slot Chassis" or "Fan Replacement for 5-Slot Chassis," Chapter 14.)
       - If none of the fans are running, go to Chapter 6, "Troubleshooting the Power Supplies."
       - After correcting the problem, continue the visual checkout.

    d. Turn the power off and reinsert any boards you removed.

11. Replace the front panel (see "Front Panel Replacement," Chapter 14).

12. Turn the power on and check the Power-On light on the front console. If this light is on, you can assume that the voltages are within operating margins. In this case, go to Chapter 5, "Computer Self-Test"; otherwise, go to Chapter 6, "Troubleshooting the Power Supplies." After correcting the power supply problem, go to Chapter 5.

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CHAPTER 5
COMPUTER SELF-TEST

Whenever the computer is powered up, the CPU automatically runs a 4-second self-test to ensure that the computer can load and run diagnostic programs. (The CPU also runs this test after a power failure when battery backup is not present.) The self-test consists of several ROM-resident diagnostic tests which check the operation of the power supply, the system terminal, the basic CPU functions, and the first 32K bytes of memory. As the CPU completes portions of the self-test it prints (displays) part of the following message on the system terminal:

```
OK
!000000
!
```

The last exclamation point (!) is the VC prompt.

If the entire message is printed, all the diagnostic tests have run and the self-test is successfully completed. If only part of the message is printed, the self-test found a bad unit. The indicator lights on the front console together with the printed part of the message indicate the probable faulty unit, as shown in Table 5.1.

Table 5.1
FAULT INDICATORS

Power Light	Run Light	Message Printed on System Console	Fault Indicated
Off	On or off		Power supply
On	On for 1 sec then off		Basic CPU
On	Flashes on once*		System terminal
On	Off	0	Memory
On	Off	OK	CPU(PFP)

** The run light flashes on and off so quickly you may miss it and assume you have a faulty basic CPU instead of a faulty system terminal. To make sure you do not make this mistake, you should watch the run light and run the self-test again whenever you think the self-test indicates a basic CPU fault or a system terminal fault. If the run light does not flash on, you have a faulty basic CPU indication.*

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TROUBLESHOOTING WITH THE SELF-TEST

Check out the computer with the self-test as follows:

1. Switch the power on.
2. If the self-test is completed (the entire message is printed out) and any problems found during the visual check are corrected, go to Chapter 7, "Diagnostic Testing."
3. If the self-test is not successfully completed, follow the procedure given below for the fault indicated. If you replace a board and the self-test still indicates the same fault, replace the original board before continuing, unless otherwise indicated. Procedures for replacing FRUs are given in Chapter 14.

NOTE *Each time you replace an FRU, repeat steps 1 through 3 until the self-test is successfully completed.*

Power Supply Fault

Go to Chapter 6, "Troubleshooting the Power Supplies."

Basic CPU Fault

1. Replace the CPU board.
2. If the self-test still indicates a CPU fault with the board, do the following:
   a. Enter the virtual console (VC) by pressing the RESET switch on the front console.
   b. Read the contents of accumulators AC0, AC1, and AC2 using the VC (see Chapter 2).
   c. Replace the new CPU board with the original CPU board and repeat steps a and b.
   d. If the contents of the accumulators are NOT identical in both cases, both CPU boards are probably faulty. Try another CPU board, if you have one.
   e. If the contents of the accumulators are identical in both cases, remove all the printed circuit boards from the chassis except the power supply board, the CPU board, and the memory board which contains the first 16K physical addresses (see "Memory Board Replacement," Chapter 14 to identify this board). If the self-test still indicates a CPU fault, replace the power supply board.
3. If you have already replaced the CPU and power supply boards, replace the bus terminators.

System Terminal Fault

1. Visually check out the terminal as follows, and then repeat steps 1 through 3, "Troubleshooting with the Self-Test," above.
   a. Make sure the connectors on the device cable for the system terminal are securely plugged into the backpanel and the terminal.
   b. Make sure the terminal is connected to the ac line source, turned on, and on-line. Also make sure the correct interface type and baud rate are selected (see the CPU tailoring section of the appropriate installation data sheets).
2. If you have already visually checked the system terminal but have NOT replaced the CPU board, replace the CPU board. If the self-test still indicates a system terminal fault with the new CPU board, check the contents of the accumulators as described in step 2, "Basic CPU Fault," using both the new and original CPU boards. If the contents of the accumulators are identical for both boards, continue to step 3; otherwise, try another CPU board, if you have one.
3. See if the system terminal works in local mode. If it does, replace the device cable; otherwise, troubleshoot the system terminal (see the documentation for the appropriate terminal).
4. If the terminal uses an EIA interface and you have already done steps 1 through 3, replace the power supply board.

Memory Fault

1. Remove the memory board which contains the first 16K physical memory addresses and check the board select jumpers (see "Memory Board Replacement," Chapter 14).
2. If the correct board select jumpers are inserted, replace the memory board.
3. If the self-test still indicates a memory fault with the new memory board, check the contents of the accumulators as described in step 2, "Basic CPU Fault," using both the new and original memory boards. If the contents of the accumulators are identical for both boards, replace the CPU board and continue to step 4; otherwise, try another memory board, if you have one.
4. If you have already replaced the CPU board and the self-test still indicates a memory fault, check the contents of the accumulators as decribed in step 2, "Basic CPU Fault," using both the new and original CPU boards. If the contents of the accumulators are identical for both boards, continue to step 5; otherwise, try another CPU board, if you have one.
5. In a 16-slot chassis if you have already done steps 1 through 4, see if the memory board will work in any available memory slot. If it does, move the bus terminators, if required.
6. If you have already done steps 1 through 5, first replace the bus terminators. If this does not correct the problem, replace the power supply.

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CPU (PFP) Fault

1. Replace the CPU board.
2. If the self-test still indicates a CPU (PFP) fault with the the new CPU board, check the contents of the accumulators as described in step 2, "Basic CPU Fault," using both the new and original CPU boards. If the contents of the accculumators are identical for both boards; continue to step 3; otherwise, try another CPU board, if you have one.
3. Remove the memory board which contains the first 16K physical memory addresses, and check the board select jumpers (see "Memory Board Replacement," Chapter 14) for jumpering.
4. If the correct board select jumpers are inserted, replace the memory board.
5. If the self-test still indicates a CPU (PFP) fault with the new memory board, check the contents of the accumulators as described in step 2, "Basic CPU Fault," using both the new and original memory boards. If the contents of the accumulators are identical for both boards, continue to step 6; otherwise, try another memory board, if you have one.
6. In a 16-slot chassis if you have already done steps 1 through 5, see if the memory board will work in any available memory slot. If it does, move the bus terminators, if required.
7. If you have already done steps 1 through 6, replace the bus terminators.

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TROUBLESHOOTING THE 16-SLOT POWER SUPPLY

WARNING: *The VNR unit and power supply board generate dangerously high voltages. DO NOT ATTEMPT TO MEASURE VOLTAGES INSIDE THEM. Before you remove the cover on the VNR unit or the power supply board, WAIT AT LEAST 5 MINUTES AFTER POWERING DOWN THE SYSTEM to allow the high voltages to dissipate.*

To troubleshoot the 16-slot power supply, carry out the following steps:

1. Initial checkout
2. Indicator light checkout
3. Voltage checkout
4. Final checkout
5. Battery backup checkout

Complete all steps in the order in which they are presented. (Step 5 is only for systems with battery backup.) Failure to do so may result in longer system down time and unnecessary assistance from DGC Field Service.

Whenever you replace a unit, repeat the check that indicated a unit was faulty. If the check still indicates the unit is faulty, replace the original unit before continuing. Procedures for replacing field replaceable units are given in Chapter 14.

IMPORTANT: The steps for troubleshooting the power supply assume the following conditions:

- The CPU board is in the chassis. (An unloaded power supply will not produce regulated outputs so do not troubleshoot the power supply without at least the CPU board in the chassis.)
- The load on the power supply is balanced. (You may upset this balance if you remove or add boards while troubleshooting. See the installation data sheets, DGC No. 010-000213, for the load balancing rules.)
- All the electrical connections between units are good.
- The lock switch on the front console is in the UNLOCK position.

If you have any reason to think that these conditions are not met, check them before proceeding.

Initial Checkout

1. Turn power off and unplug the chassis ac line cord from the cabinet.
2. Make sure the cabinet is supplying the proper ac line voltage.
3. Plug the line cord back into the cabinet.
4. Swing VNR unit away from backpanel (see "VNR Unit Replacement," Chapter 14).

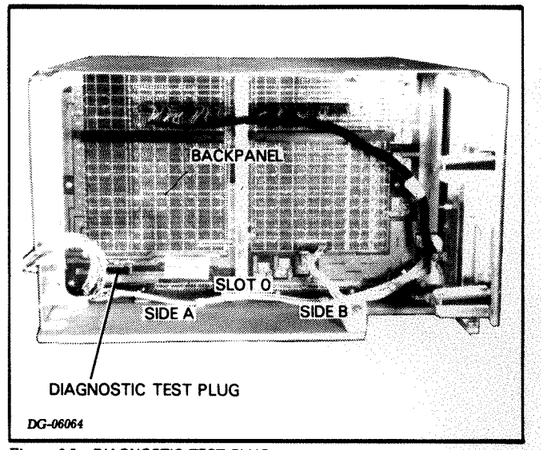

Figure 6.5 **DIAGNOSTIC TEST PLUG**

5. Make sure the diagnostic test plug is inserted in the correct location with the RUN label up (see Figure 6.5).
6. Swing the VNR unit back into position (see "VNR Unit Replacement," Chapter 14).
7. Remove front panel (see "Front Panel Replacement," Chapter 14).
8. Turn the power on.
9. Look at the left side of the chassis through the open slots and see if all the fans are running. You may need to remove boards from slots 6 and 15 and use a flashlight to see the fans.
   a. If all four fans are running, reinsert any boards you removed, and proceed to "Indicator Light Checkout."
   b. If some, but not all, of the fans are running, replace the faulty fans and make sure the cable connectors to the fans and the console PCB assembly are seated securely. (See "Fan and Fan Module Replacement for 16-Slot Chassis," Chapter 14).
   c. If none of the fans are running, continue checkout.
10. If you have NOT already replaced a fan,
    a. Remove the fan module and make sure the cable connectors to the console PCB boards are seated securely (see "Fan and Fan Module Replacement for 16-Slot Chassis," Chapter 14).
    b. Reinstall the fan module.
11. Make sure the internal cable (wiring harness) connectors to the backpanel, the power supply board, and the VNR unit are seated securely (see "VNR Unit Replacement," Chapter 14).
12. Turn the power off.
13. Check the two 15 Amp ac line fuses which screw into the upper left rear corner of the VNR unit (see Figure 6.6).

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CHAPTER 6
TROUBLESHOOTING THE POWER SUPPLIES

This chapter will help you find the failing field replaceable units in the power supply and power distribution system. When you find a failing unit, replace it following the replacement procedure given in Chapter 14. For a detailed description of how the power supply operates, see Chapter 9 (16-slot) or Chapter 10 (5-slot).

OVERVIEW

Before you try to troubleshoot the power supply, it is helpful to know what the power supply does and how its indicator lights function.

Major Functions

The power supplies for both the 16-slot and the 5-slot chassis perform the following functions:

- Supply regulated dc operating voltages for the chassis
- Supply ac voltages for the fans
- Generate clocks for the CPU, memory, and floating point unit (FPU)
- Generate a time base for the CPU's real time clock
- Change the dc operating voltages in response to commands from the CPU (voltage margining - 16-slot power supply only)
- Detect and respond to emergency conditions (power loss, excessive voltage or current, etc.)
- Provide power status indicators for the CPU (power fail, power ok, etc.)
- Provide emergency battery backup for the memory voltages (optional).

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Indicator Lights

Two indicator lights on the front console of both chassis display the status of the power supply (see Figure 6.1).

Power-on Light - Indicates that the dc voltages are stable. If the power switch is on and the light is out, one of the following may have occurred:

- AC power brownout or blackout
- Power supply failure
- Excessive load or short circuit on backpanel
- Diagnostic test plug not in RUN position (16-slot chassis only).

Battery Backup Light - Indicates that the battery is supplying the dc operating voltages for the memories because either a power line failure, a power supply failure, or a shutdown (due to external shorts) occurred.

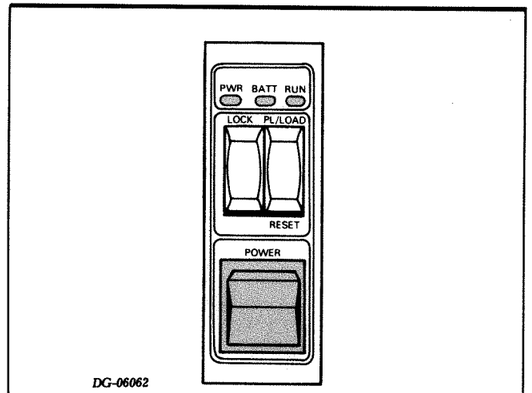

Figure 6.1 FRONT CONSOLE INDICATOR LIGHTS

The 16-slot chassis has three additional indicator lights which give further status information. These lights are located on the front of the power supply board as shown in Figure 6.2.

Over-Current - Indicates that an over-current condition appeared in the supply or on the backpanel. The supply automatically tries to recover from an over-current condition. As a result, you may see this light blink up to 6 times before it finally stays on. Once it stays on you must power the supply down to clear the fault light (this probably will not correct the fault).

Over-Voltage Light - Indicates that an over-voltage condition appeared in the supply. You must power the supply down to clear the fault light (this probably will not correct the fault).

Memory Disaster Light - Indicates that a memory module detected a dc power failure on **-5 MEM.** You must power the supply down to clear the fault light (this probably will not correct the fault).

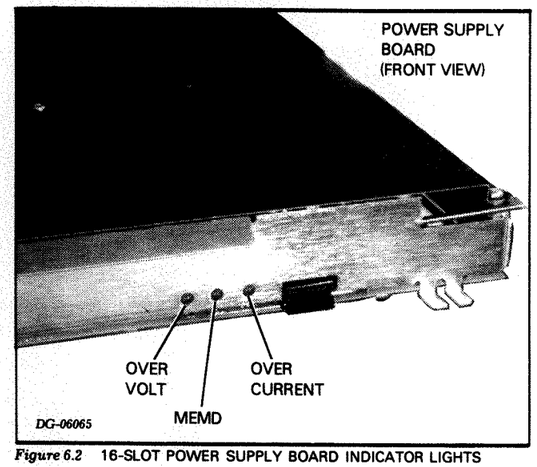

Figure 6.2 16-SLOT POWER SUPPLY BOARD INDICATOR LIGHTS

Functional Description

16-Slot Power Supply

The power supply and distribution system for the 16-slot chassis consists of a VNR unit, a power supply printed circuit board, a fan module, and a backpanel circuit board. These four modules are interconnected by an internal cable (wiring harness) and by etch on the backpanel, as shown in Figure 6.3.

The VNR unit converts power from the ac line to unregulated dc voltages for the power supply board. It also routes ac power to the fans in the fan module. In a system with battery backup, the VNR unit contains a battery charger along with a small battery that supplies power for the battery backup circuits in the power supply board. A plug on the back of the unit lets you connect an external battery when longer backup times are required.

The power supply board is a printed circuit board which regulates the dc voltages from the VNR unit and in turn powers the chassis. It also provides clock and status signals for the CPU, memory, and FPU. Fault detection circuits automatically shut down the power supply if an emergency condition occurs. In addition, a voltage margining feature lets the CPU change the memory voltages under program control to test memory integrity.

The backpanel routes power, control, and status signals between the power supply board and the printed circuit boards. It includes several reed switches that detect excessive current flow in the printed circuit boards. (These switches replace the fuses commonly found on other backpanels.)

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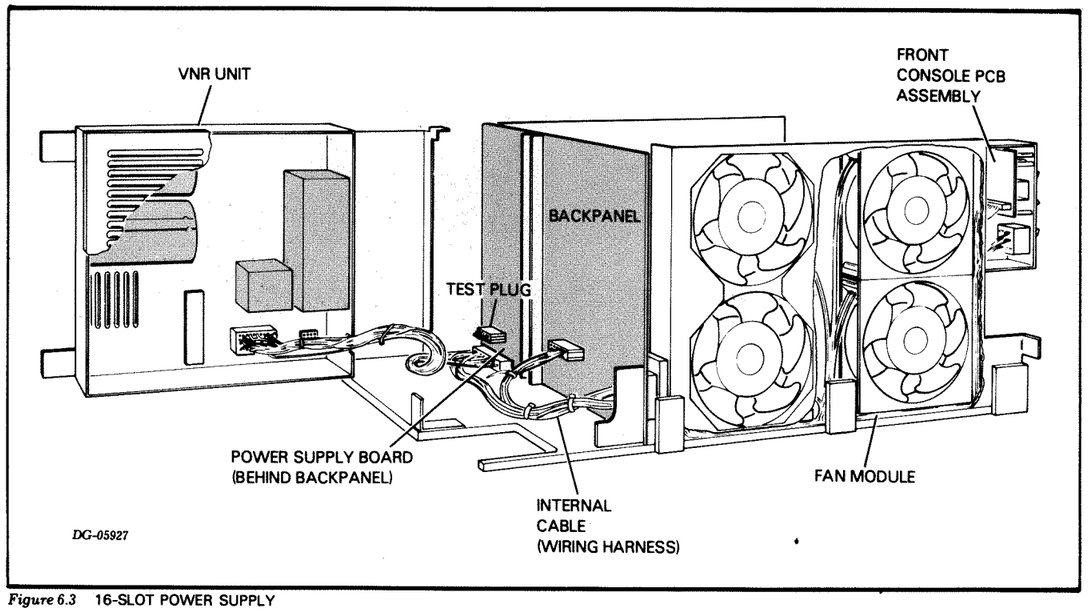

Figure 6.3 16-SLOT POWER SUPPLY

5-Slot Power Supply

The power supply and distribution system for the 5-slot chassis consist of a power supply board, a fan module, a console PCB assembly, and a backpanel circuit board. These modules are interconnected by an internal cable (wiring harness) and by etch on the backpanel, as shown in Figure 6.4.

The power supply board converts the power from the ac line to regulated dc voltages and in turn powers the chassis. It also provides clock and status signals for the CPU and memory. Fault detection circuits automatically shut down the supply if an emergency condition occurs. In a system with battery backup, the power supply board contains a battery charger along with a small battery that supplies power for the battery backup circuits.

The backpanel routes power, control, and status signals between the power supply circuit board and the printed circuit boards.

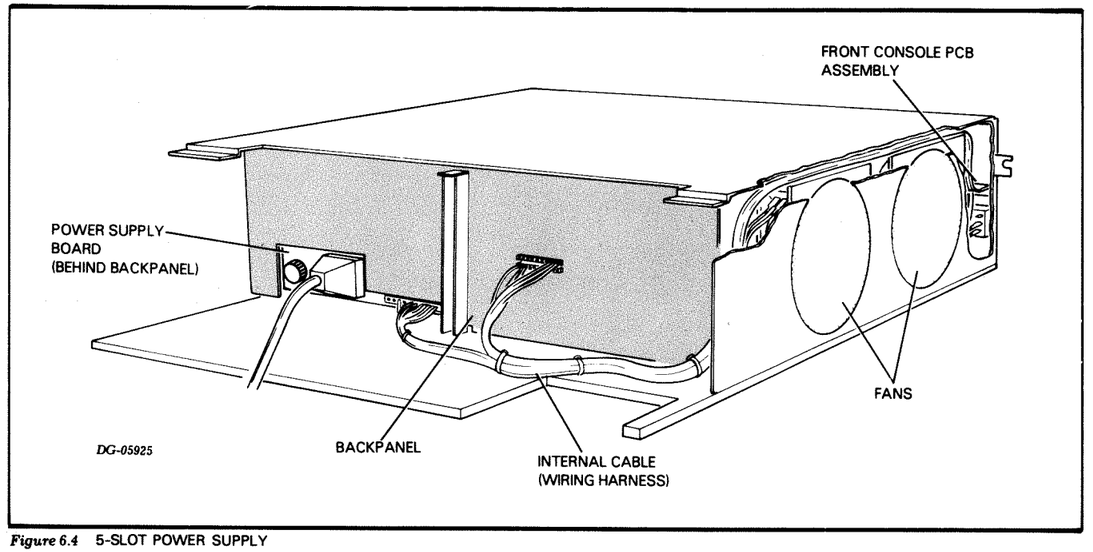

Figure 6.4 5-SLOT POWER SUPPLY

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Battery Backup Checkout

Only carry out this checkout if the system has battery backup. This procedure will not discharge the battery a significant amount. Note that it takes 16 hours for the battery to fully recharge.

1. Turn the power on and unplug the chassis ac line cord from the cabinet.
2. Check the **+12 MEM** voltage at location J35-3 (see Figure 6.7).
   a. If this voltage is GREATER THAN 11.0 volts and remains CONSTANT for MORE THAN 1 MINUTE, continue to step 3 of this checkout; otherwise,
   b. Check the **BAT+** voltage at jack J3-1 (see Figure 6.9).
      - If **BAT+** is greater than 12V, replace the power supply board.
      - If **BAT+** is NOT greater than 12V, then measure the voltage DIFFERENCE between J3-5 and J3-6 (see Figure 6.9). If it is greater than one volt, replace the battery; otherwise, replace the VNR unit.

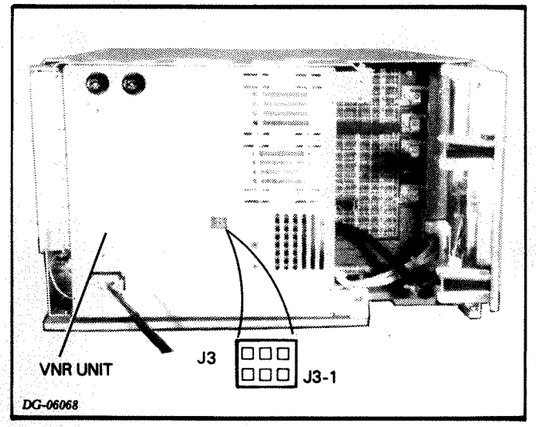

Figure 6.9 JACK3

3. Check the battery backup light on the front console,
   a. If this light is on, plug the power cord into the ac source and then go to Chapter 5, "Computer Self-Test."
   b. If the light is NOT on, replace the power supply board, and if the light still does not turn on, replace the console PCB assembly.
4. Plug the ac line cord back into the cabinet.

TROUBLESHOOTING 5-SLOT POWER SUPPLY

WARNING: *The power supply board generates dangerously high voltages. DO NOT ATTEMPT TO MEASURE VOLTAGES INSIDE. Before you remove the cover on the power supply board WAIT AT LEAST 5 MINUTES AFTER POWERING DOWN THE SYSTEM to allow the high voltages to dissipate.*

To troubleshoot the 5-slot power supply, carry out the following steps:

1. Initial checkout
2. Final checkout
3. Battery backup checkout

Complete all steps in the order in which they are presented. (Step 3 is only for systems with battery backup.) Failure to do so may result in a longer system down time and unnecessary assistance from DGC Field Service.

Whenever you replace a unit, repeat the check which indicated that unit was faulty. If the check still indicates the unit is faulty, replace the orginal unit before continuing. Procedures for replacing field replaceable units are given in Chapter 14.

IMPORTANT: The steps for troubleshooting the power supply assume the following conditions:

- The CPU board is in the chassis. (An unloaded power supply will not produce regulated outputs so do not troubleshoot the system without at least the CPU board in the chassis.)
- All the electrical conections between units are good.
- The lock switch on the front console is in the UNLOCK position.

If you have any reason to think that these conditions are not met, check them before proceeding.

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   a. If the fuses are all right, replace the fan module.
   b. If the fuses are blown:
      - Replace them if you have NOT already replaced them; otherwise,
      - If the fans still do not run, replace the VNR unit.
14. If you cannot get the fans to run after carrying out steps 9 through 13, replace the internal cable (wiring harness).

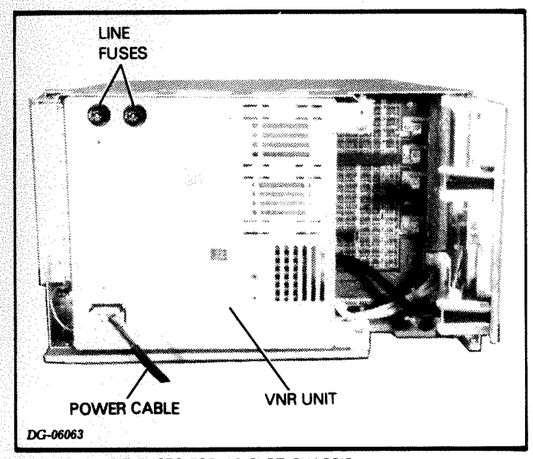

Figure 6.6 LINE FUSES FOR 16-SLOT CHASSIS

Indicator Light Checkout

1. Turn the power on.
2. Check the indicator lights on the front end of the power supply board (see Figure 6.2). If they are all out, go to step 3, "Voltage Checkout"; otherwise, turn the power off and then on again. If any of the lights turn on again, follow the procedure below for the lights which are on. Whenever you replace a unit, repeat this step.
3. If any light still turns on after you have tried the procedure below, replace the internal cable (wiring harness).

Memory Disaster Light

1. Turn the power off.
2. Check that the diagnostic test plug is in the correct location with the RUN label up (see Figure 6.5). If it is, continue to step 3; otherwise:
   a. Reposition the plug.
   b. Turn the power on.
   c. Check the memory disaster light. If it is on, continue to step 3.
3. If the system contains MORE THAN ONE memory board continue to step 4; otherwise, replace the power supply. If the memory disaster light is still on, replace the memory board.
4. Turn the power off.
5. Remove a memory board.
6. Turn the power on.
7. Check the memory disaster light.
   a. If the light is NOT on, replace the memory board (see "Memory Board Replacement," Chapter 14).
   b. If the light is ON, reinsert the original board, and repeat steps 3 through 7 with any other memory board you have not already tried removing.
   c. If the light is still on after you have tried removing all the memory boards, replace the power supply board.

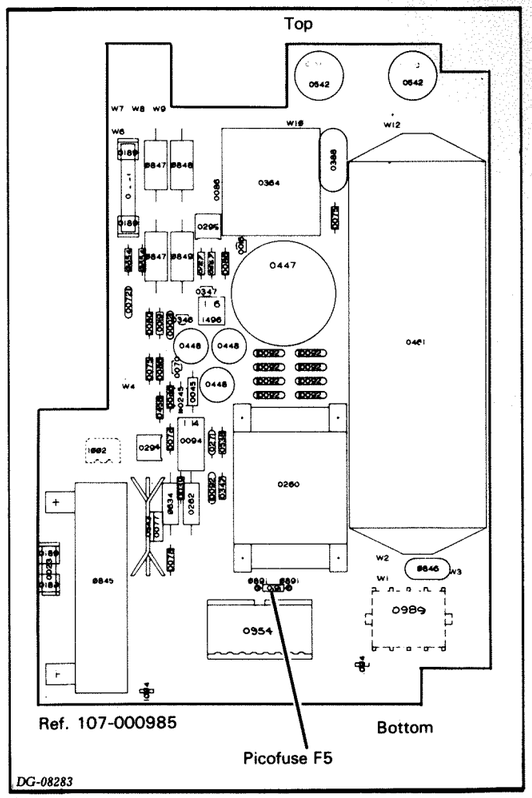

Figure 6.6A LOCATION OF PICO FUSE ON PC BOARD INSIDE VNR UNIT

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Over-Current Light

1. Turn the power off.
2. Replace the power supply board.
3. Turn the power on.
4. Check the over-current light. If the light is on, turn the power off and remove any printed circuit board, other than the power supply board.
5. Turn the power on.
6. Check the over-current light.
   a. If the light is NOT on, replace the board being sure to insert the correct jumpers (see "Memory Board Replacement," Chapter 14, or the appropriate I/O device documentation).
   b. If the light is on, reinsert the removed board, and repeat steps 4 through 6 with any other printed circuit board you have not already tried removing.
   c. If you have already done steps a and b and the overcurrent light is still on, check that the load on the power supply is balanced (see the installation data sheets, DGC No. 010-000213, for the load balancing rules).

Over-Voltage Light

1. Turn the power off.
2. Replace the power supply board.
3. Turn the power on.
4. If the light is still on, replace the CPU board.

Voltage Checkout

1. Turn the power on.
2. Check the +5V voltage at test plug J1-15 (see Figure 6.8). If +5V is between 5.10V and 5.20V, go to "Final Checkout"; otherwise, continue the checkout.
3. Turn the power off and wait 5 minutes.
4. Check the 1.5A, 125V pico fuse F5 (DGC No. 113-000191) on the PC board in the VNR unit (See Figure 6.6A). If it is blown, replace it.
5. Short **MEMD** at J35-21 to **GND** at J35-1 (see Figure 6.7).
6. Turn the power on and check the memory disaster light.
   a. If the light is NOT on, turn the power off, remove the short, and replace the VNR unit.
   b. If the light is on, turn the power off, remove the short, and then turn the power on.

- Check the -11V voltage at J35-25 (see Figure 6.7)
- If -11V is NOT between -11.0V and -12.5V (-30VNR not ok), check the **VREF** at test plug J1-14 (see Figure 6.8). If **VREF** is 5.8V, replace the VNR unit; otherwise, replace the power supply board.
- If -11V is between -11.0V and -12.5 (-30VNR ok), check the **HVS** voltage at test plug J1-4 (see Figure 6.8). If **HVS** is greater then 2.9V, replace the power supply board; otherwise, replace the VNR unit.

7. Recheck the +5V voltage at test plug J1-15 (see Figure 6.8). If it is between 5.10V and 5.20V, go to "Final Checkout"; otherwise, try replacing the internal cable (wiring harness). If this does not work, get help from DGC Field Service.

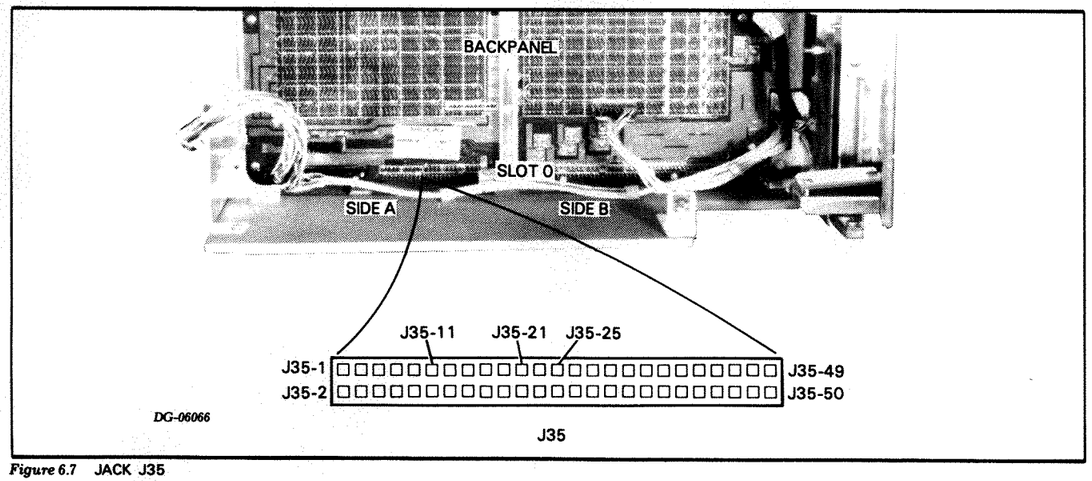

Figure 6.7 JACK J35

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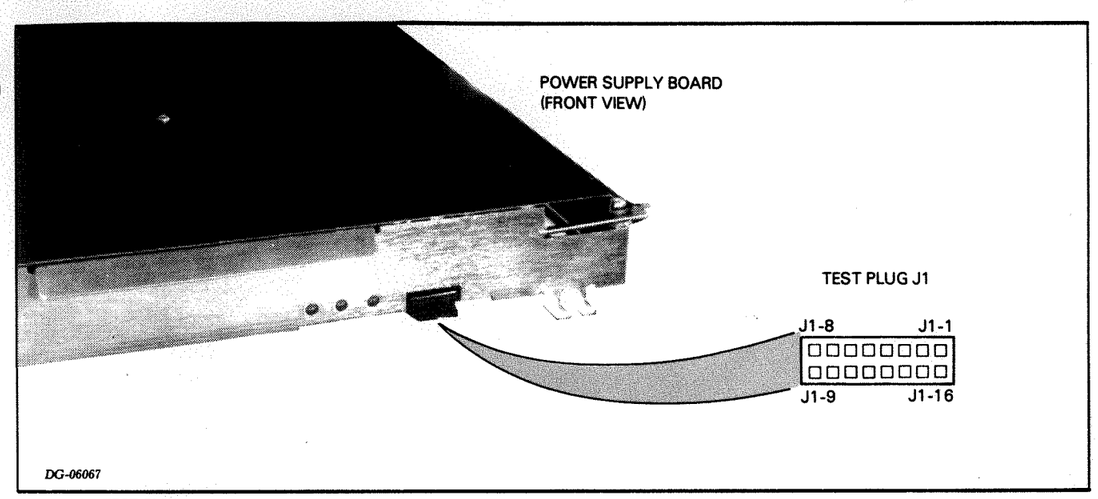

Figure 6.8 TEST PLUG

Final Checkout

1. Turn power on.
2. Check the power on light on the front console.
   a. If the light is on, continue to step 3 of this checkout.
   b. If the light is NOT on, check the $\overline{\text{ONLED-P}}$ voltage at J35-11 (see Figure 6.7).
      - If $\overline{\text{ONLED-P}}$ is 3V or GREATER, replace the power supply board; otherwise, replace the console PCB assembly.
      - If the light still is not on, replace the fan module, and if this does not correct the problem, replace the internal cable (wiring harness).
3. Turn the power off and see if the fans stop.
   a. If the fans stop:
      - Go to step 5, "Battery Backup Checkout" if the system has battery backup.
      - Go to Chapter 5, "Computer Self-Test," if the system does not have battery backup.
   b. If the fans do NOT stop:
      - Make sure the LOCK switch is in the UNLOCK position. If the fans still do not stop, check the $\overline{\text{PWR FAIL}}$ voltage at test plug J1-3 (see Figure 6.8).
      - If $\overline{\text{PWR FAIL}}$ is NOT less than 0.4V, replace the fan module.
      - If $\overline{\text{PWR FAIL}}$ is less than 0.4V, check PON at test plug J1-11 (see Figure 6.8). If PON is less than 0.4V, replace the VNR unit; otherwise, replace the power supply board.

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TROUBLESHOOTING FLOWCHART

The troubleshooting flowchart that appears on the following pages leads you through sequences of reliability and diagnostic tests that will both isolate faulty field replaceable units and verify the proper operation of either the NOVA 4/S or 4/X computer. It assumes that the programs are loaded and run under the control of DTOS and specifies the DTOS commands to be used.

NOTE: *Detailed information concerning DTOS and DTOS commands appears in* How to Use DTOS *(DGC No. 015-000103) and* DTOS Summary *(DGC No. 015-000082).*

If a DTOS loading device (i.e., magnetic tape unit or disc drive) is not present in the system or is inoperable, the flowchart can still be used by running the programs in the sequences indicated, using the field engineering cassette.

Throughout the flowchart, action recommendations following each program test are made solely on a pass/fail basis. To determine if a test passed, refer to the sample program run summary for that test at the end of this chapter. Each summary describes both the operator input and the program output, i.e., the information that will be printed (displayed) by the system terminal when the specified test passes. Additionally, the summaries associated with the memory diagnostics explain how to interpret error messages to identify a failing memory board.

When the flowchart specifies the replacement of a field replaceable unit (FRU), proceed as follows:

- Power down the system
- Replace the specified FRU (see Part III for replacement procedures)
- Power up the system
- Reload DTOS
- Rerun the failing test. If it passes, verify the systems's operation by restarting at the beginning of the flowchart.

Memory Diagnostics

The diagnostic testing sequences outlined in the first part of the troubleshooting flowchart are run in DTOS auto mode. If this testing fails to detect suspected, intermittent memory errors, more vigorous testing of memory can be accomplished by running the appropriate memory diagnostic tests in DTOS manual mode. Operating procedures for running memory diagnostics in both modes are outlined in the appropriate sample program run summaries.

Voltage Margining

When running memory diagnostic tests in manual mode, the Data General field service engineer can adjust the system's operating voltages in computers equipped with a diagnostic test plug (16-slot chassis). It is important to note that this diagnostic tool is intended to be used solely to detect intermittent memory errors, since other use of voltage margining may significantly degrade the system.

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Initial Checkout

1. Turn the power off and unplug the chassis ac line cord from the cabinet.
2. Make sure the ac line source in the cabinet is supplying the proper ac line voltage.
3. Plug the line cord back into the cabinet.
4. Turn the power on.
5. Look at the left side of the chassis through the open slot and see if both fans are running. You may need to remove the board from slot 4 and use a flashlight to see the fans.
   a. If both fans are running, reinsert the board you removed, and go to "Final Checkout".
   b. If only one fan is running, replace the fan which is not running and go to "Final Checkout." While you replace the fan, make sure the cable connectors to the fans and the console PCB assembly are seated securely.
   c. If neither fan is running, continue with this checkout.
6. If you have NOT already replaced a fan, make sure the internal cable (wiring harness) connectors to the console PCB assembly are seated securely (see "Internal Cable Replacement," Chapter 14).
7. Make sure the internal cable (wiring harness) connectors to the backpanel and the power supply board are seated securely.
8. Switch the power off.
9. Check the 7 Amp ac line fuse which screws into the left rear corner of the power supply board and extends through a cutout in the backpanel (see Figure 6.10).
   a. If the fuse is all right, replace the power supply board.
   b. If the fuse is blown:
      - Replace it if you have NOT already replaced it; otherwise,
      - Replace the power supply board.
10. If you cannot get the fans to run after carrying out steps 1 through 9, replace the internal cable.

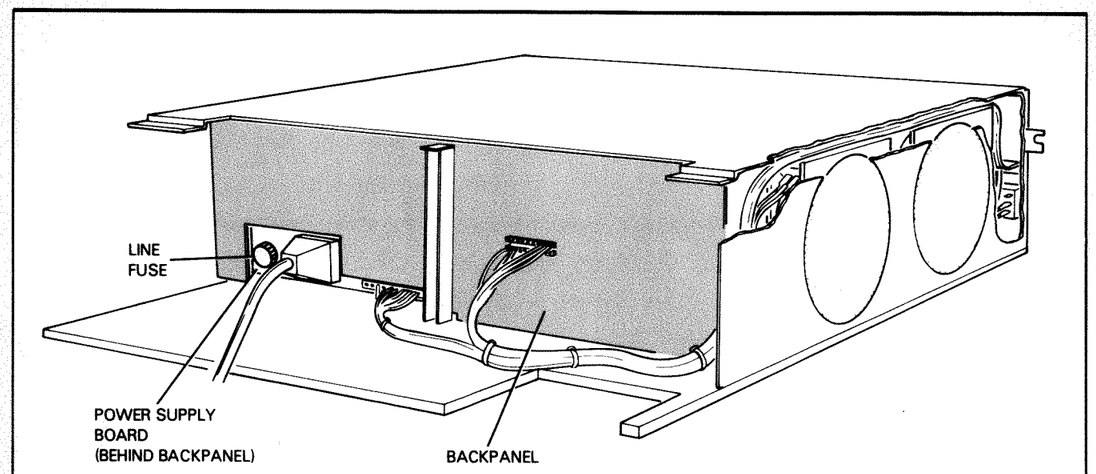

Figure 6.10 LINE FUSE FOR 5-SLOT POWER SUPPLY

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Final Checkout

1. Turn power on.
2. Check the power on light on the front console.
   a. If the light is on, continue to step 3 of this checkout.
   b. If light is NOT on:
      - Replace the power supply board.
      - If the light still does not go on, reseat the internal cable (wiring harness) connectors to the the console PCB assembly. If this does not correct the problem, first replace the console PCB assembly, and then the internal cable (wiring harness).
3. Turn the power off and see if the fans stop.
   a. If the fans stop:
      - Go to "Battery Backup Checkout" if the system has battery backup.
      - Go to Chapter 5, "Computer Self-Test", if the system does not have battery backup.
   b. If the fans do NOT stop, replace the power supply board. If this does not correct the problem, first try reseating the internal cable (wiring harness) connectors, and then replace the internal cable.

Battery Backup Checkout

Only carry out this checkout if the system has battery backup. This procedure will not discharge the battery a significant amount. Note that it takes 24 hours to fully recharge the battery.

1. Turn the power on and unplug the chassis ac line cord from the cabinet.
2. Check the +12 MEM voltage at backpanel pin B47.
   a. If this voltage is GREATER than 11.3 volts and REMAINS CONSTANT FOR MORE THAN 5 MINUTES, go to step 3 of this checkout; otherwise, continue with step b.
   b. Most likely the battery is bad or the battery charger on the power supply board is not operating properly. If you have reason to suspect the battery is bad, replace it; otherwise, replace the power supply board. Note that an unused battery lasts about 3 1/2 years at 23 deg.C and its life expectancy decreases greatly with increases in operating temperature. A battery can be used for about 200 cycles.
3. Check the battery backup light on the front console,
   a. If this light is on, plug the line cord back into the cabinet and go to Chapter 5, "Computer Self-Test".
   b. If the light is NOT on, replace the power supply board, and if the light still does not turn on, replace the console PCB assembly.
4. Plug the ac line cord back into the cabinet.

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Chapter 7
DIAGNOSTIC TESTING

Successful completion of the self-test indicates that the main portion of the NOVA 4/S or 4/X computer is operating properly. This means that the reliability and diagnostic test programs summarized in Table 7.1 can be loaded into main memory and used to:

- Detect faulty replaceable units during troubleshooting
- Verify that the computer is operating properly during initial checkout or after repair

The programs listed in Table 7.1 are available on the media listed in Table 7.2. Loading procedures for the diagnostic operating system (DTOS) appear in Appendix B. Procedures for using the field service cassette appear in Appendix C. Detailed information about DTOS and DTOS commands appears in *How to Use DTOS* (DGC No. 015-000103) and in *DTOS Summary* (DGC No. 015-000082).

Program Name	DTOS Mnemonic and Listing No.	Program Description
NOVA 3, NOVA 4 Multi-programming Reliability Test, Short	N3MORTS 096-000347	Test CPU and memory subsystems with multiply/divide, FPU, real-time clock, and TTY output. Uses I/O tester board to exercise data channel.
NOVA 3, NOVA 4 Multi-programming Reliability Test, Long	N3MORTL 096-000348	Incorporates all tests made in short version Instead of I/O tester, uses peripherals with primary device codes on the system to exercise data channel and interrupt facilities.
NOVA 3, NOVA 4 Multi-programming Reliability Test, Peripheral	N3MORTP 096-000508	Exercises memory, and the CPU's data channel and interrupt facilities plus all primary and secondary peripheral devices in the system.
NOVA and ECLIPSE Logical Memory Verifier	NELMEMV 096-2393	Verifies basic integrity of logical memory address space of up to 64 Kbytes.
NOVA 4 Memory Diagnostic, Unmapped, Parts 1 and 2	N4SMMD1 096-001134 N4SMMD2 096-001135	Used on NOVA 4/S only. Checks up to 64 Kbytes of memory. May be run under nominal or marginal power supply voltage.
NOVA 4/X Mapped Memory Diagnostic	N4XNND 096-001132	Checks up to 256 Kbytes of memory.
NOVA 4 Memory Allocation and Protection Diagnostic	N4MAPD 096-00113	Tests map instructions, two user maps and two data channel maps.
NOVA 4 Floating Point Test Program	N4FPD 096-001130	Tests all operations performed by the floating point arithmetic unit.
NOVA 4 I/O Diagnostic Test	N4IOD 096-002523	Exercises NOVA 4 I/O system, real-time clock and TTY outputs.
Interrupt Priority Test	PRIORX 096-002500	Checks interrupt priority of all devices on line and ready.
NOVA Effective Address Instruction Exerciser	NEFADRX 096-001738	Exercises effective address calculation logic for all NOVA memory reference instructions.
NOVA Instruction Set Diagnostic, Parts 1 and 2	NESISV1 096-001733 NESISV2 096-001734	Checks out basic NOVA instruction set (Part 1) and tests auto-increment and auto-decrement functions (Part 2).
NOVA Instruction Verification Test, Parts 3 and 4	N34SISV 096-002352 N4SISV 096-002353	Checks out stack, trap, and multiply/divide instructions (Part 3) and byte, other stack instructions and signed multiply/divide instructions, (Part 4).

Table 7.1 Reliability and diagnostic test program summary

Table 7.1 Reliability and diagnostic test program summary (continued)

Media	Description	Part No.
Magnetic tape	Model 3802M (800 BPI) Model 3802H (1600 BPI)	074-000119
Diskette	Single density	075-000071 075-000072 075-000073 075-000074
Diskette	Dual density (quad floppy)	065-000002
Cassette	Field Engineering Cassette	Depends on revision

Table 7.2 DTOS media

NOTE: *The four single-density diskettes, collectively, contain the NOVA 4 test programs referred to in this chapter.*

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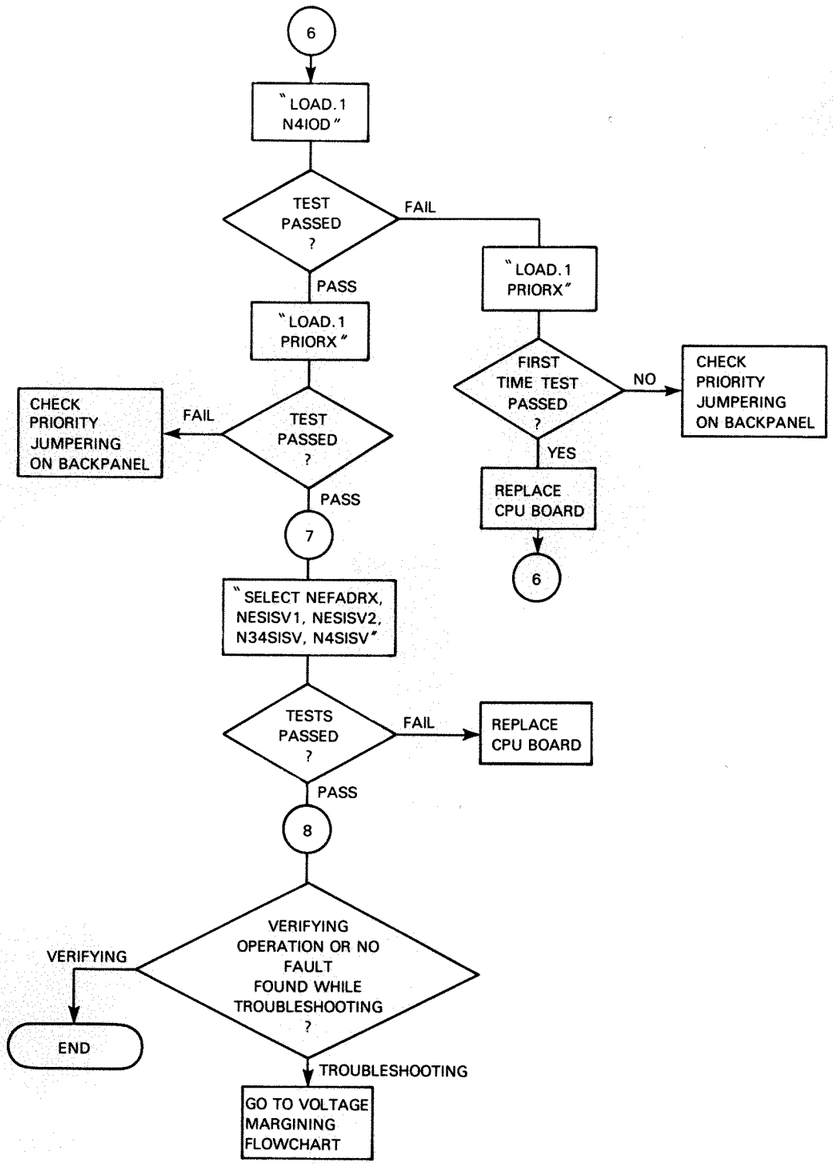

DG-08287

Figure 7.1 TROUBLESHOOTING FLOWCHART (CONTINUED)

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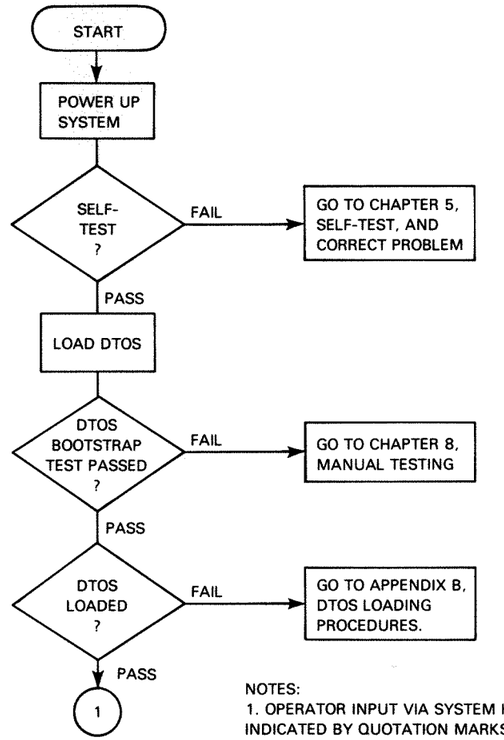

NOTES:
1. OPERATOR INPUT VIA SYSTEM KEYBOARD INDICATED BY QUOTATION MARKS, E.G., "LOAD.3 N3 MORT S"
2. SEE APPROPRIATE SAMPLE PROGRAM RUN SUMMARY FOR PROGRAM OPERATING PROCEDURES.
3. SEE APPROPRIATE MEMORY DIAGNOSTIC SAMPLE PROGRAM RUN TO IDENTIFY FAILING MEMORY BOARD.
4. WHENEVER THE LOAD COMMAND IS USED TO RUN THE SPECIFIED PROGRAM, DTOS MUST BE RELOADED BEFORE THE TESTING SEQUENCE CAN BE CONTINUED.

DG-08284

Figure 7.1 TROUBLESHOOTING FLOWCHART

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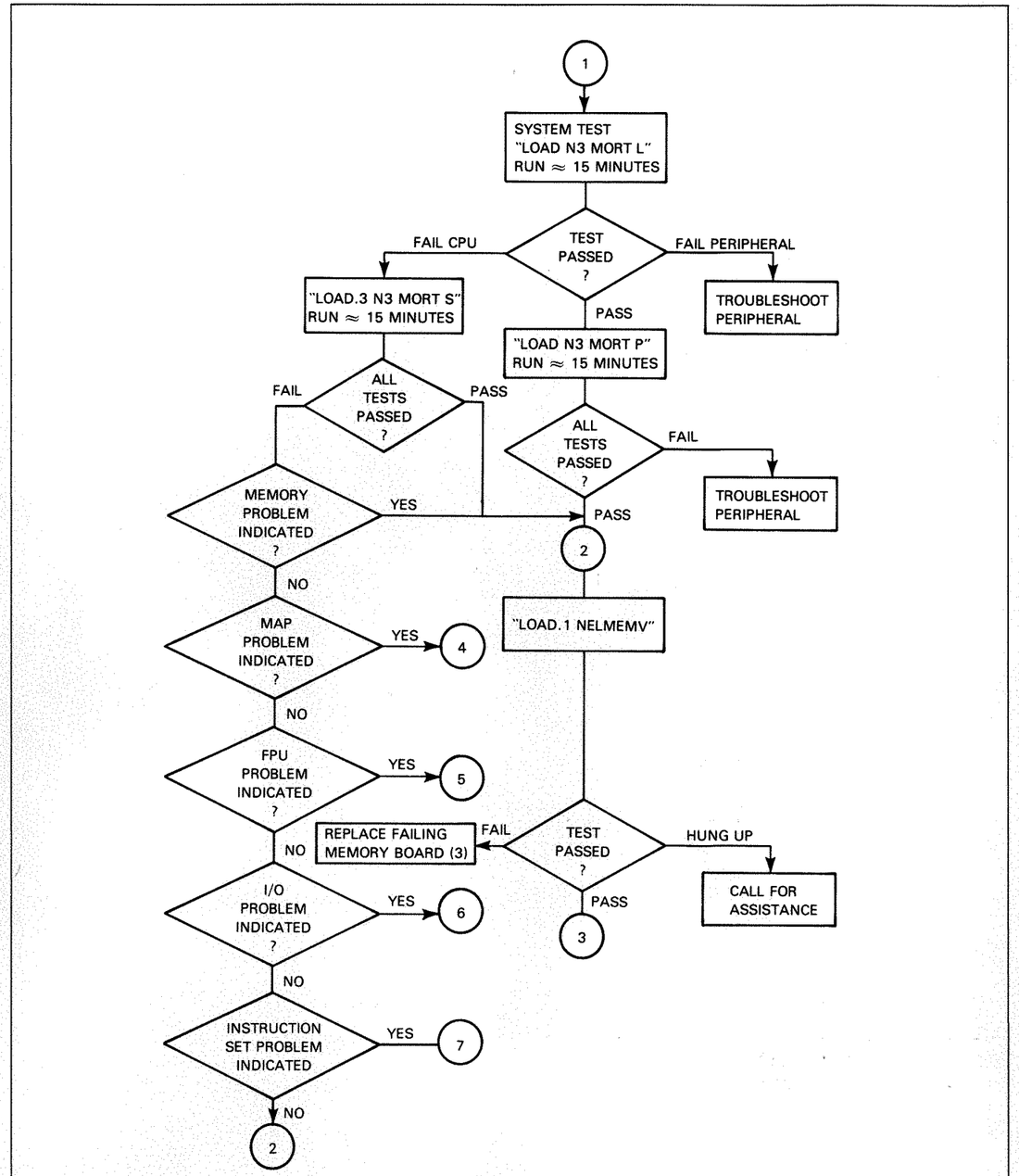

Figure 7.1 TROUBLESHOOTING FLOWCHART (CONTINUED)

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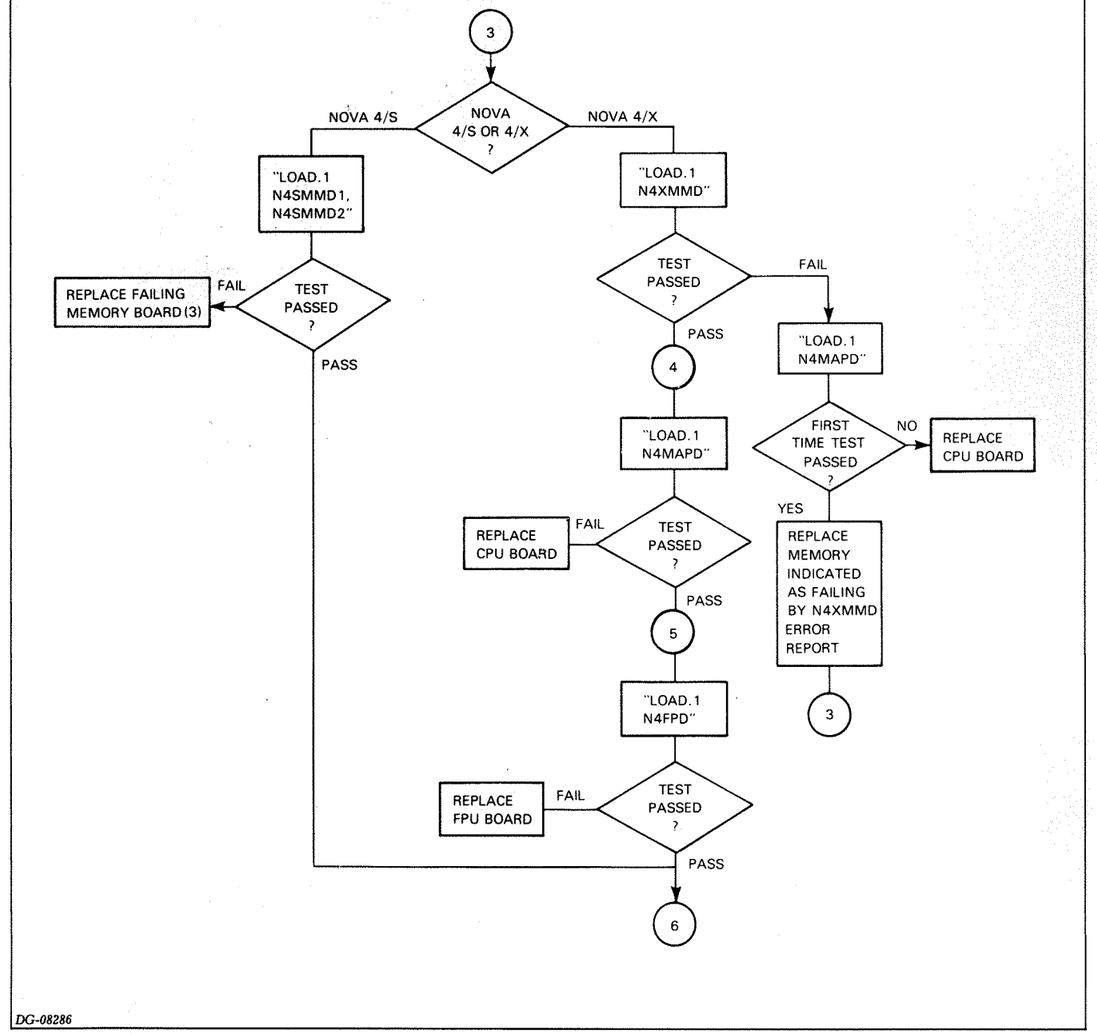

Figure 7.1 TROUBLESHOOTING FLOWCHART (CONTINUED)

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NOVA AND ECLIPSE LOGICAL MEMORY VERIFICATION TEST (DTOS Semi-auto Mode; No Errors Found)

DTOS Mnemonic:	NELMEMV
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	None
Listing No.:	096-002393
Estimated Program Run time:	6 seconds per pass for for 64K bytes

Operator Input:

*LOAD.1 NELMEMV

Program Output:

```
LOAD:
NELMEMV REV.00
NELMEMV REV.00 ENTERED
TOP OF MEMORY= 77777
TESTING COMPLETED...
END OF PASS 1
*
```

Note

The program contains a monitor that gives the operator control over several functions. To access the monitor, enter CNTRL-C while the program is running. This causes the program to print the following:

---ENTER PROGRAM MONITOR---

**? is the monitor prompt. When it appears, enter one of the commands summarized in the table below.

Command	Meaning	Action Taken
A	ABORT	Return to DTOS.
C	CLEAR	Clear error log.
D	DUMP	Print and clear error log.
E	EXIT	Return to main program.
F	FLAGS	Print control flags.
H	HALT	Halt processor.
M	MODIFY	Change test parameters.
O	ODT	Read/write memory (ODT emoulator).
P	PRINT	Print error log.
S	SWREG	Change value of switch register.
T	TERMINATE	Terminate current test and return to program.
?	HELP	Print commands and descriptions.

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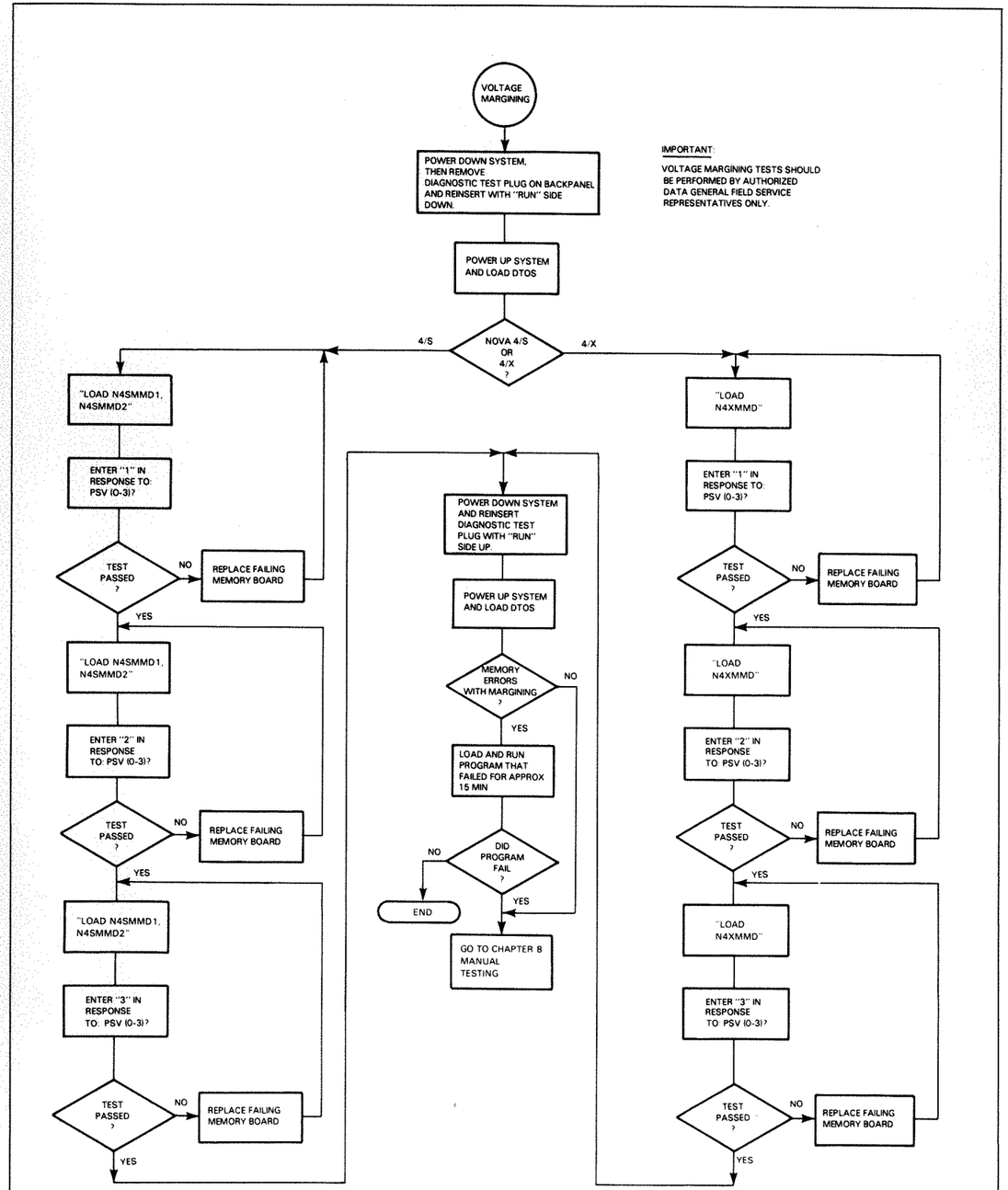

Figure 7.1 TROUBLESHOOTING FLOWCHART (CONTINUED)

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NOVA 3, NOVA 4 MULTIPROGRAMMING RELIABILITY TEST SHORT VERSION (DTOS Semi-auto Mode; No Errors Found)

DTOS Mnemonic:	N3MORT S
DTOS Directory:	HOST
DTOS Command:	LOAD.1 or LOAD.3
Special Machine Requirements:	None
Reference:	Listing No. 096-000347
Estimated Program Run Time:	5 minutes

Operator Input: **Comments**

```
*HOST
*LOAD.3 N3MORT S
Program Output
LOAD:
N3MORT S REV. 06
NOVA 3 MULTIPROGRAMMING
   RELIABILITY TEST (SHORT VERSION)
TOTAL # 1K'S 32 NO MAP                    Note 1
TEST RUN LIST                             Note 2
TST # DESCRIPTION
0    CHKRBRD RAN
1    SC MEMORY TEST
2    ARITHMETIC TEST
4    MUL/DIV TEST
5    REAL TIME CLOCK
6    TTY TEST
!"#$%&'()*,-./0123456789:;?@              Note 3
ABCDEFGHIJKLMNOPQRSTUVWXYZ
R/T (HRS, MIN, ERTOT)   0    5            Note 4
*
```

Notes

1. NO MAP is printed when program is run on NOVA 4/S computer. MAP EXISTS is printed when program is run on NOVA 4/X computer. TOTAL # 1K'S varies with system.
2. The contents of the test run list may vary depending upon the program revision level and equipment configuration.
3. Teletypewriter test. This information may not be printed due to the running time of the program.
4. This information may not be printed due to the running time of the program. The two digits following the (HRS, MIN, ERTOT) mean that the test ran 0 hours, 5 minutes. If a third digit is appended, it refers to the error total, indicating at least one test failed.

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NOVA 3, NOVA 4 MULTI-PROGRAMMING RELIABILITY TEST LONG OR PERIPHERAL VERSION (DTOS Manual Mode; Error Found)

DTOS Mnemonic:	N3MORT L (Long) N3MORT P (Peripheral)
DTOS Directory:	HOST
DTOS Command:	LOAD
Special Machine Requirements:	None
References:	
Listing Long:	096-000348
Listing Peripheral:	096-000508

NOTE: *All input/output devices should be placed on-line. Disc drives and tape units should be loaded with scratch disc packs or tapes to prevent data loss.*

Operator Input: **Comments**

```
*LOAD N3MORTL                             Note 1
Program Output:
LOAD:
N3MORT L REV. 06
@200R
N3MORT LONG - REV 06
TOTAL # 1K'S= MAP EXISTS                  Note 2
TEST RUN LIST                             Note 3
   NAME        DESCRIPTION
   CBRDS       ;CHECKERBOARD MEMORY TEST
   SCMTS       ;SEMICONDUCTORY MEMORY TEST
   ARITH       ;CPU ARITHMETIC TEST
   STKTS       ;NOVA 3 STACK TEST
   BYTES       ;LOAD & STORE BYTE INSTRUCTION
               TEST.
   MUDVT       ;MULTIPLY/DIVIDE TEST
   FPTST       ;FLOATING POINT UNIT TEST
   DCUTS       ;DCU TEST
   NVDSK       ;NOVA DISK TEST (PRIMARY).
   PGDSK       ;PAGING DISK TEST (PRIMARY).
   MVDSK       ;MOVING HEAD DISK TEST
               (PRIMARY).
   PZDSK       ;ZEBRA DISK TEST (PRIMARY).
   MTTES       ;MAG TAPE TEST (PRIMARY).
   CATES       ;CASSETTE TAPE TEST (PRIMARY).
   LPTTS       ;LINE PRINTER TEST
DEV.#27 6060/61 DISK
DSK#    #CYLS   #SEC/S    #SURF
0       815       24        19
DEV.#33 M.H.DISK
DSK#    #CYLS   #SEC/S    #SURF
0       408       12        4
R/T(HRS,MINS,ERTOT)=0    5                Note 4
PROGRAM #11    6060/61    DISK(PRI)       Note 5
AC'S 010000    017377    060201
SCRLO/HI 026000 031777 USER B DCHLO/H1
056000 061777
MEM ALLOCATION TABLE
PHYS   LOGICAL   PHYS   LOGICAL
74     026000    24     030000
CYL #     ZBDST     ZBCST
101012    026114    0;56114
ZBSTA     ZBDOA     ZBDOC
060201    000000    017071                Note 6
R/T(HRS,MINS,ERTUT)= 0 7 1
```

Notes

1. When running peripheral version, substitute N3MORT P.
2. Number of 1K's varies with the size of memory. MAP EXISTS is printed when the CPU is a NOVA 4/X.
3. The tests run vary with the system configuration.
4. This message indicates the program ran for 5 minutes without errors.
5. This message indicates an error was found when testing the 6060/61 disc drive, unit 0. In this case, run the 6060/61 diagnostics.
6. This message indicates the program ran 7 minutes before it encountered the failure indicated above.

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NOVA 4/X MAPPED MEMORY DIAGNOSTIC (DTOS Auto Mode; Errors Found)

DTOS Mnemonic:	N4XMMD
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	NOVA 4/X CPU
Reference:	Listing No. 096-001132

Operator Input: **Comments**

```
*LOAD.1 N4XMMD
```

Program Output:

```
ACTIVE DIRECTORY=HOST
PROCESSOR UNDER TEST=HOST
LOAD:
N4XMMD REV. 01 <Date>
**PROGRAM EXEC**
TEST NAME: MODIFIED DATA=ADDRESS
TEST NAME: DATA=ADDRESS UPPER
TEST NAME: STUCK ADDRESS BIT
TEST NAME: RELOCATING ISZ-DSZ
TEST NAME: MARCHING 1-0
TEST NAME: GALLOPING COLUMNS
***ERRORS ENCOUNTERED
TEST NAME:
BOARD NUMBER=                    Note 1
MODULE=
BANK=
BIT NUMBER(S)
***
```

Note

1. This is an error message. In single memory board systems, the board number is always 1. In multiple board systems, the board assigned the lowest memory address range (e.g., 00000-77777) is designated as board 1, the board assigned the next highest memory address range is designated as board 2, and so on. Refer to the system configuration chart to determine the slot location of the failing memory board.

   Module and bank locations are explained in Chapter 12.

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NOVA 4 MEMORY DIAGNOSTIC UNMAPPED PART 1 and PART 2 (DTOS Auto Mode; No Errors Found)

DTOS Mnemonic:	
Part 1	N4SMMD1
Part 2	N4SMMD2
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	NOVA 4/S CPU
Part 1 Reference:	Listing No. 096-001134
Part 2 Reference:	Listing No. 096-001135
Estimated Program Run Time:	2 minutes

Operator Input: **Comments**

```
* LOAD.1 N4SMMD1
```

Same format to run N4SMMD2

Program Output:

```
ACTIVE DIRECTORY=HOST
PROCESSOR UNDER TEST=HOST
LOAD:
N4SMMD1<Date>
**PROGRAM EXEC**
TEST NAME: MODIFIED DATA=ADDRESS
TEST NAME: STUCK ADDRESS BIT
TEST NAME: MARCHING 1-0
TEST NAME: RELOCATING ISZ-DSZ
TEST NAME: GALLOPING COLUMNS
TEST NAME: GALLOPING ROWS
TEST NAME: GALLOPING DIAGONAL
    .
    .
    .
    .
TEST NAME: GALLOPING DIAGONAL
TESTING COMPLETED...
BOARD NUMBER=                    Note 1
ADDRESS START=
ADDRESS END=
RAM TYPE=
***END PROGRAM***
PASS 1
*
```

Note

1. In multiple memory board systems, this message is printed at the end of the program test for each board. The board assigned the lowest memory address range is designated as board 1 while the board assigned the highest address range is designated as board 2.

   The octal addresses (0-37) refer to the physical 1K blocks and vary, depending upon the address range assigned to each board. The RAM type (4K or 16K) depends upon the size of the memory board under test.

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NOVA 4 MEMORY DIAGNOSTIC UNMAPPED PART 1 and PART 2 (DTOS Auto Mode; Error Found)

DTOS Mnemonic:	
Part 1	N4SMMD1
Part 2	N4SMMD2
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	NOVA 4/S CPU
Part 1 Reference:	Listing No. 096-001134
Part 2 Reference:	Listing No. 096-001135

Operator Input:

*LOAD.1 N4SMMD1

Comments

Same format to run N4SMMD2

Program Output:

ACTIVE DIRECTORY=HOST
PROCESSOR UNDER TEST=HOST
LOAD.1 N4SMMD1 <Date>
PROGRAM EXEC
TEST NAME: MODIFIED DATA=ADDRESS
TEST NAME: STUCK ADDRESS BIT
TEST NAME: MARCHING 1-0
TEST NAME: RELOCATING ISZ-DSZ
TEST NAME: GALLOPING COLUMNS
*** ERROR ENCOUNTERED
TEST NAME:
BOARD NUMBER= Note 1
MODULE=
BANK=
BIT NUMBER(S)
***

Note

1. This is an error message. In single memory board systems, the board number is always 1. In multiple board systems, the board assigned the lowest memory address range is designated as board 1 while the board assigned the highest address range is designated as board 2. Refer to the system configuration chart to determine the slot location of the failing memory board.

   Module and bank locations are explained in Chapter 12.

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NOVA 4/X MAPPED MEMORY DIAGNOSTIC (DTOS Auto Mode; No Errors Found)

DTOS Mnemonic:	N4XMMD
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	NOVA 4/X CPU
Reference:	Listing No. 096-001132
Estimated Program Run Time:	1 Minute

Operator Input:

*LOAD.1 N4XMMD

Comments

Program Output:

ACTIVE DIRECTORY=HOST
PROCESSOR UNDER TEST=HOST
LOAD:
N4XMMD REV.01 <Date>
PROGRAM EXEC
TEST NAME: MODIFIED DATA=ADDRESS
TEST NAME: DATA=ADDRESS UPPER
TEST NAME: STUCK ADDRESS BIT
TEST NAME: MARCHING 1-0
TEST NAME: RELOCATING ISZ-DSZ
TEST NAME: GALLOPING COLUMNS
TEST NAME: GALLOPING ROWS
TEST NAME; GALLOPING DIAGONAL
.
.
.
.
.
.
.
.
.
.
.
.
.
.
TEST NAME: GALLOPING DIAGONAL
TESTING COMPLETED . . .
BOARD NUMBER= Note 1
ADDRESS START=
ADDRESS END=
RAM TYPE=
END PROGRAM
PASS 1

Note

1. In multiple memory board systems, this message is printed at the end of the program test for each board. The board assigned the lowest memory address range (e.g., 00000-77777) is designated as board 1; the board assigned the next highest address range is designated as board 2, and so on.

   The addresses (0-177) refer to the physical 1K blocks and vary depending upon the address range assigned to each board. The RAM (16K or 4K) depends upon the size of the memory board being tested.

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NOVA INSTRUCTION VERIFICATION TEST, PARTS 3 AND 4 (DTOS Semi-auto Mode; No Errors Found)

DTOS Mnemonic:	
Part 3	N34SISV
Part 4	N4SIS V
DTOS Directory:	Host
DTOS Command:	SELECT
Special Machine Requirements:	None
Listing No.:	
Part 3	096-002352
Part 4	096-002353
Estimated Program Run Time:	Less than 1 minute

Operator Input: **Comments**

*SELECT N34SISV, N4SIS V Note 1

Program Output:

```
SELECT N34SISV, N4SIS V
ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST
LOAD:
N34SISV REV. 00
NOVA INSTRUCTION VERIFICATION TEST, PART 3
PASS    1
PASS    2
PASS    3
PASS    4
PASS    5
LOAD:
N4SIS V REV. 00
NOVA INSTRUCTION VERIFICATION TEST, PART 4
PASS    1
PASS    2
PASS    3
PASS    4
PASS    5
*
```

Note

1. This command runs both parts 3 and 4 of the NOVA Instruction Set Verification Test. To run only one part, enter SELECT and the DTOS mnemonic for the part. For example, to run just part 3,enter SELECT N34SISV.

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NOVA 4 MEMORY ALLOCATION AND PROTECTION (MAP) DIAGNOSTIC (DTOS Auto Mode; No Errors Found)

DTOS Mnemonic:	N4MAPD
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	NOVA 4/X CPU
Reference:	LISTING NO. 096-001131
Estimated Program Run Time:	A few seconds, each pass

Operator Input: **Comments**

* LOAD.1 N4MAP D

Program Output:

```
LOAD:
N4MAP D REV.01
NOVA 4 MAP DIAGNOSTIC
MAP FOUND USING SINGLE CYCLE INSTRUCTION
MAP FOUND USING PAGE MAPPING
PAGE MAPPING--MAXIMUM MEMORY SIZE =
000177 PHYSICAL PAGES
SINGLE CYCLE MAPPING--MAXIMUM MEMORY SIZE
= 000177  PHYSICAL PAGES                    Note 1
FPU EXISTS
RTC EXISTS
PASS    1
PASS    2
PASS    3
PASS    4
PASS    5
PASS    6
*
```

Note

1. Memory size varies with memory board configurations.

DGC NOVA 4 FLOATING POINT TEST PROGRAM (DTOS Auto Mode; No Errors Found)

DTOS Mnemonic:	N4FPD
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	Floating Point Unit Option
Reference:	Listing No. 096-001130

Operator Input:

*LOAD.1 N4FPD

Program Output:

```
SELECT N4FPD
ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST
LOAD:
N4FPD REV. 03
DGC NOVA 4 FLOATING POINT DIAGNOSTIC REV. 03
PASS 1
*
```

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NOVA 4 I/O DIAGNOSTIC TEST (DTOS Auto Mode; No Errors Found)

DTOS Mnemonic:	N4IOD
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	Multi-mode I/O Tester Board No. 005-0042183 (if available)
Reference:	Listing No. 096-002523
Run Time:	1 minute (a few seconds without I/O Tester Board)
Restrictions:	Secondary RTC and TTO devices are not tested. I/O tester must be present for full test. This program does not run with the CAT program.

Operator Input: **Comments**

*LOAD.1 N4IOD

Program Output:

```
LOAD.1 N4IOD
ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST
LOAD:
N4IOD REV. 00
N4IOD 00
NOVA 4 I/O AND RTC TEST
RTC PRESENT
I/O TESTER NOT FOUND IN SYSTEM
**** THE QUICK BROWN FOX JUMPS OVER THE
LAZY DOG. ****
ABCDEFGHIJKLMNOPQRSTUVWXYZ0123456789
/#$%&()*+,-.:;<=>-?@][\^'"
'"^\][@?->=<:;.-,+*)(&%&#!
9876543210ZYXWVUTSRQPONMLKJIHGFEDCBA
AC LINE FREQUENCY IS 60 HZ                Note 1
PASS 1
```

Interrupt Priority Test (DTOS Auto Load/Auto Run; No Errors Found)

DTOS Mnemonic:	PRIORX
DTOS Directory:	HOST
DTOS Command:	LOAD.n
Special Machine Requirements:	Peripheral devices must be on line and ready
Reference:	Listing No. 096-002500
Run Time:	Depends on number of devices being tested (2 passes approximately 1 minute)

Operator Input:

*LOAD.1 PRIOR X

Program Output:

```
SELECT PRIORXX
ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST
LOAD:
PRIOR X REV.00
PRIOR X 00 RUNNING
PROCESSORY TYPE IS NOVA(3,4)
FROM: HOST
        EQUIPMENT TABLE, HIGHEST PRIORITY FIRST
          MNEMONIC    DEV CODE
          TTO         11
          RTC         14
          FPU         76
          MTA         22
          DKP         33
          LPT         17
PASS 1
*
```

Note

1. Prints (displays) 50Hz if line frequency is 50Hz.

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NOVA EFFECTIVE ADDRESS INSTRUCTION EXERCISER (DTOS Semi-auto Mode; No Errors Found)

DTOS Mnemonic:	NEFADRX
DTOS Directory:	Host
DTOA Command:	SELECT
Special Machine Requirements:	None
Listing No.:	096-001738
Estimated Program Run Time:	Less than 1 minute

Operator Input:

*SELECT NEFADRX

Program Output:

```
SELECT NEFADRX
ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST
LOAD:
NEFADRX REV. 01
* PROGRAM NAME/REV.:    NEFADRX    1
* PROGRAM DESCRIPTION: NOVA EFF. ADDR. INSTR.
EXERCISER
PASS 1
PASS 2
PASS 3
PASS 4
PASS 5
*
```

NOVA INSTRUCTION SET DIAGNOSTIC, PARTS 1 AND 2 (DTOS Semi-Auto mode; No Errors Found)

DTOS Mnemonic:	
Part 1	NESISV1
Part 2	NESISV2
DTOS Directory:	HOST
DTOS Command:	SELECT
Special Machine Requirements:	None
Listing No.:	
Part 1	096-001733
Part 2	096-001734
Estimated Program Run Time:	Less than 1 minute

Operator Input: **Comments**

*SELECT NESISV1, NESISV2 Note 1

Program Output:

```
SELECT NESISV1, NESISV2
ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST
LOAD:
NESISV1 REV.01
PROGRAM NAME: NESISV1 REV.01
PROGRAM DESCRIPTION:NOVA INSTRUCTION SET
DIAGNOSTIC
PASS 1
PASS 2
LOAD:
NESISV2 REV. 01
PROGRAM NAME:NESISV2 REV. 01
PROGRAM DESCRIPTION:NOVA INSTRUCTION SET
DIAGNOSTIC
PASS 1
PASS 2
*
```

Note

1. This command runs both parts of the NOVA Instruction Set Verification Test. To run only one part, enter SELECT and the DTOS mnemonic for the part. For example, to run just part 1, enter SELECT NESISV1.

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2. This option, together with the option described in Note 3 below, allows the operator to select a portion of memory for testing. The number entered (0-377) selects the first physical 1K block in memory to be tested. This number must be less than the top physical 1K block present in the system.
3. The number entered (0-377) allows the operator to select the last physical 1K block in memory to be tested. If the specified ending address exceeds the top address, the ending address is set to the top of memory.
4. To select specific modules, enter a bit pattern as shown below.

Module Tested	Set Following Bit to 1	Octal Number Entered
A	15	1
B	14	2
C	13	4
D	12	10

For example: entering a 1 selects module A only; entering a 5 selects both modules A and C; 17 or Line Feed (default) selects all modules. For an explanation of modules, see Chapter 12.

5. ECM refers to the error control mode. The number entered affects the action taken when an error is encountered.

ECM	Action Taken
0	Print an error report and return to DTOS.
1	Print an error report and continue.
2	Print an error report and halt (illegal when using power supply voltage margining).
3	Print an error report and go to program monitor (See Note 10, below).
4	Enter error in error log and continue.

6. The following information is printed when an error is found:

*** ERROR ENCOUNTERED
TEST NAME:
BOARD NUMBER=
MODULE=
BANK=
BIT NUMBER(S)

If question concerning supplemental error report is answered yes, the following information is also printed: failure address, expected data, actual data.

If question concerning error log is answered yes, the following information is printed at the conclusion of the testing: chip location (board, bank, module, bit), the address range, test names and failure count. See the appropriate listing for more detailed information.

7. To run tests under marginal conditions, the diagnostic test plug must be in the test position. To select the operating voltages, see the table below.

Octal Number Entered	Voltages VBB	VDD	VCC
0 (Selects nominal voltage only)	−5V	+12V	+5V
1	−4.5V	+10.8V	+4.75V
2	−5.25V	+12.6V	+5.25V
3 (First runs voltages selected by 1; then runs voltages selected by 2.)			

8. Patterns refer to the bit pattern used to select tests. Thus, to select one or more tests, enter the octal number that sets the appropriate bits to 1. See the table below.

Bit Position	Test Name	Mode Run	Estimated Test Time
15	Modified Data =Address	Auto	15 sec
14	Data=Address, Upper	Auto	5 sec
13	Stuck Address Bit	Auto	3 sec
12	Marching I/O	Auto	15 sec
11	Relocating ISZ-DSZ	Auto	5 sec
10	Galloping Columns	Auto	1 min
9	Galloping Rows	Auto	1 min
8	Galloping Diagonal	Auto	1 min
7	Galloping Pattern	Manual	2 hours

Example: 377 selects all tests except Galloping Pattern. All estimated test times are for 256K words of memory and assume no memory.

9. For information about multiprogramming, see the text file in the appropriate listing.
10. The following table summarizes the program monitor commands.

Command	Meaning	Action Taken
A	ABORT	Return to DTOS
C	CLEAR	Clear error log
D	DUMP	Print and clear error log
E	EXIT	Return to main program
F	FLAGS	Print control flags
H	HALT	Halt program
P	PRINT	Print error log
R	RESET	Print control flags; input new values
T	TERMINATE	Terminate the current test and return to program execution

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NOVA 4 MEMORY DIAGNOSTIC UNMAPPED Part 1 and Part 2 (DTOS Manual Mode; No Errors Found)

DTOS Mnemonic:	
Part 1	N4SMMD1
Part 2	N4SMMD2
DTOS Directory:	HOST
DTOS Command:	LOAD
Special Machine Requirements:	NOVA 4/S CPU Diagnostic test plug in test position
Part 1 Reference:	Listing No. 096-001134
Part 2 Reference:	Listing No. 096-001135
Estimated Program Run Time:	See Note 6 below

WARNING: *Do NOT type CTRL-R, CTRL-D or BREAK, or hit the front panel RESET switch during any program run where voltages are margined. To stop the program, see PROGRAM TERMINATION below.*

Operator Input:	Comments
*LOAD N4SMMD1	Same format to run N4SMMD2
Program Output:	
ACTIVE DIRECTORY = HOST PROCESSOR UDNER TEST = HOST	
LOAD: N4SMMD1 REV. 01	
** PROGRAM EXEC ** INPUT NEW VALUES FOR CONTROL FLAGS MODULES TO BE TESTED (0-17)?	Note 1
Operator Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 2 FOLLOWED BY A CARRIAGE RETURN>	Note 2
Program Output:	
ECM <0-4>	
Operator Input:	
<ENTER 0 FOLLOWED BY A CARRIAGE RETURN>	Note 3
Program Output:	
SUPPLEMENTAL ERROR INFORMATION (Y/N)?	Question asked when ECM=0, 1, 2 or 3 Otherwise,
PRINT ERROR LOG AT CONCLUSION (Y/N)?	Question asked when ECM=4. See Note 4
Operator Input:	
<Y or N FOLLOWED BY A CARRIAGE RETURN>	Yes or No
Program Output:	
POWER SUPPLY VOLTAGES (0-3)?	
Operator Input:	
FOR NORMAL OPERATION, ENTER 0 FOLLOWED BY A CARRIAGE RETURN. FOR VOLTAGE MARGINING, ENTER APPROPRIATE NUMBER AS INDICATED IN TROUBLESHOOTING FLOWCHART FOLLOWED BY A CARRIAGE RETURN	Note 5
Program Output:	
PATTERNS (0-377)?	
Operator Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 6 FOLLOWED BY A CARRIAGE RETURN>	Note 6

NOTE: *When this diagnostic test is run using the LOAD command, the test will continue until stopped by the operator. See Program Termination below.*

Program Termination

Operator Input:	
CTRL-C	Enters the program monitor -- see Note 7 below
CTRL-A	Aborts the program, returns voltages to nominal levels and returns to DTOS

Notes

The following notes summarize information appearing in the text file portion of the program listings. For more detailed information, refer to the appropriate listing.

1. The table below shows the control flags default settings (Line Feed Selects default.)

Description of Control Key	Control Flag (CF)	Program Octal Value	Default
Starting address in memory	STADR	0	Beginning of memory
Ending address in memory	ENDADR	Top	Top of memory
Modules under test	MUT	0	All
Error control mode	ECM	0	Print error, return to DTOS
Supplementary error information	SEI	0	None
Power supply voltages	PSV	0	Nominal only
Error log print	LP	0	No log printed at conclusion of testing
Patterns to be run	PATS	177	All except Galloping Patterns test
Multiprogramming	MULTI	0	None
Manual program location	MPR	0	Done by program

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2. To select specific modules, enter a bit patterns as shown below.

Module Tested	Set Following Bit to 1	Octal Number Entered
A	15	1
B	14	2
C	13	4
D	12	10

For example: entering a 1 selects Module A only; entering a 5 selects both modules A and C; 17 or Line Feed (default) selects all modules. For an explanation of modules, see Chapter 12.

3. ECM refers to the error control mode. The number entered affects the action taken when an error is encountered.

ECM	Action Taken
0	Print an error report and return to DTOS.
1	Print an error report and continue
2	Print an error report and halt (illegal when using power supply voltage margining).
3	Print an error report and go to program monitor (See Note 7).
4	Enter error in error log and continue.

4. The following information is printed when an error is found:

***ERROR ENCOUNTERED
TEST NAME:
BOARD NUMBER=
MODULE =
BANK =
BIT NUMBER(S)=

If the question concerning supplemental error report is answered yes, the following information is also printed: failure address, expected data, actual data.

If question concerning error log is answered yes, the following information is printed at the conclusion of the testing: chip location (board, bank, module, bit), the address range, test names and failure count. See the appropriate listing for more detailed information.

5. To run tests under marginal conditions, the diagnostic test plug must be in the test position. To select the operating voltages, see the table below.

Octal Number Entered	Voltages VBB	VDD	VCC
0 (Selects nominal voltages only.)	-5V	+12V	+5V
1	-4.5V	+10.8V	+4.75V
2	-5.25V	+12.6V	+5.25V
3 (First runs voltages selected by 1; then runs voltages selected by 2.)			

6. Patterns refer to the bit pattern used to select tests. Thus, to select one or more tests, enter the octal number that sets the appropriate bits to 1. See the table below.

Bit Position	Test Name	Mode Run	Estimated Test Time
15	Modified Data =Address	Auto	5 sec
14	Stuck Address Bit	Auto	1 sec
13	Marching I/O	Auto	5 sec
12	Relocating ISZ-DSZ	Auto	2 sec
11	Galloping Columns	Auto	15 sec
10	Galloping Rows	Auto	15 sec
9	Galloping Diagonal	Auto	15 sec
8	Galloping Pattern	Manual	30 min.

Example: 177 selects all tests except Galloping Pattern.

All estimated test times are for 32K words of memory and assume no memory errors are detected.

7. The following table summarizes the program monitor commands.

Command	Meaning	Action Taken
A	ABORT	Return to DTOS
C	CLEAR	Clear error log
D	DUMP	Print and clear error log
E	EXIT	Return to main program
F	FLAGS	Print control flags
H	HALT	Halt program
P	PRINT	Print error log
R	RESET	Print control flags; input new values
T	TERMINATE	Terminate the current test and return to program execution

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NOVA 4X MAPPED MEMORY DIAGNOSTIC (DTOS Manual Mode; No Errors Found)

DTOS Mnemonic:	N4XMMD
DTOS Directory:	HOST
DTOS Command:	LOAD
Special Machine Requirements:	NOVA 4/X CPU Diagnostic test plug in test position
Reference:	Listing No. 096-001132
Estimated Program Run Time:	See Note 8 below

WARNING: *Do NOT Type CTRL-R, CTRL-D or BREAK, or hit the front panel RESET switch during any program run where voltages are margined. To stop the program, see PROGRAM TERMINATION below.*

	Comments
Operator Input:	
*LOAD N4XMMD	
Program Output:	
ACTIVE DIRECTORY = HOST PROCESSOR UNDER TEST = HOST	
LOAD: N4XMMD REV. 01 N4XMMD REV. 01	
** PROGRAM EXEC **	
INPUT NEW VALUES FOR CONTROL FLAGS STARTING ADDRESS (P.B. 0-377)?	Note 1
Operator Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 2 FOLLOWED BY A CARRIAGE RETURN>	Note 2
Program Output:	
ENDING ADDSRESS (P.B. 0-377)?	
Operator Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 3 FOLLOWED BY A CARRIAGE RETURN>	Note 3
Program Output:	
MODULES TO BE TESTED (0-17)?	
Operator Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 4 FOLLOWED BY A CARRIAGE RETURN>	Note 4
Program Output:	
ECM <0-4>	
Operator Input:	
<ENTER 0 FOLLOWED BY A CARRIAGE RETURN>	Note 5
Program Output:	
SUPPLEMENTAL ERROR INFORMATION (Y/N)?	Question asked when ECM=0,1,2 or 3.
PRINT ERROR LOG AT CONCLUSION (Y/N)?	Question asked when ECM=4 (see Note 6).
Operator Input:	
<Y OR N FOLLOWED BY A CARRIAGE RETURN>	Yes or No
Program Output:	
POWER SUPPLY VOLTAGES (0-3)?	
Operator Input:	
FOR NORMAL OPERATION, ENTER 0 FOLLOWED BY CARRIAGE RETURN. FOR VOLTAGE MARGINING, ENTER APPROPRIATE NUMBER AS INDICATED IN TROUBLESHOOTING FLOWCHART FOLLOWED BY A CARRIAGE RETURN	Note 7
Program Output:	
PATTERNS (0-377)?	
Output Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 8 FOLLOWED BY A CARRIAGE RETURN>	Note 8
Program Output:	
MULTIPROGRAMMING (Y/N)	
Operator Input:	
<ENTER N FOLLOWED BY A CARRIAGE RETURN>	Note 9

NOTE: *When this diagnostic test is run using the LOAD command, the test will continue until stopped by the operator. See Program Termination below.*

Program Termination

Operator Input:	
CTRL-C	Enters the program monitor (see Note 10)
CTRL-A	Aborts the program, returns voltages to nominal levels and returns to DTOS

Notes

The following notes summarize information appearing in the text file portion of the program listing. For more detailed information, refer to the listing.

1. The table below shows the control flags default settings (Line Feed selects default).

Description of Control Flag	Control Flag	Program Octal Value	Default
Starting address in memory	STADR	0	Beginning of memory
Ending address in memory	ENDADR	Top	Top of memory
Modules under test	MUT	0	All
Error control mode	ECM	0	Print error, return to DTOS
Supplemenary error information	SEI	0	None
Power supply voltages	PSV	0	Nominal only
Error log print	LP	0	No log printed at conclusion of testing
Patterns to be run	PATS	177	All except Galloping Patterns test
Multiprogramming	MULTI	0	None
Manual program location	MPR	0	Done by program

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Chapter 8
MANUAL TESTING

Chapters 3 through 7 should isolate most malfunctions associated with he NOVA 4/S and 4/X computers. The remainder of the troubleshooting is directed to system problems, namely, input/output.

DTOS LOADING FAILURE

If you cannot load DTOS as specified in Chapter 7, follow the steps listed below. If you find a fault as you proceed through the steps, take corrective action and attempt to load DTOS again.

1. Disconnect the loading unit (disc or tape drive) and power it up off line.

   Refer to the documentation for the device. Check to ensure that all functions that can be performed off line are responding properly. (For example, load the tape drive with a scratch tape and advance the tape to the beginning of tape position; advance the tape; rewind it.) If the unit fails to perform properly, either troubleshoot or replace the unit.
2. Examine the device cable. Is it connected properly? Are there any loose wires? Is so, replace the device cable.
3. Examine the condition of the paddleboard cable and connectors. If they appear to be without fault, slip the paddleboard connectors off the appropriate backpanel pins and then reinsert them, making sure they are properly seated.
4. Replace the CPU board.
5. Replace the bus terminators.
6. Replace the controller board if the unit is operating properly off line and the device cable and paddleboard assembly appear to be in good condition and properly connected.
7. Move the controller board to a different slot, making sure the priority chain is maintained by inserting jumpers, across the open slot. See the appropriate 5- or 16-slot, installation data sheets.
8. Replace the paddleboard assembly and the device cable.

If the above procedures fail to repair the malfunction, call DGC Field Service for assistance. If you correct the problem by following the above procedures, run the bootstrap test (TESTOK).

Bootstrap Test (TESTOK)

New releases of the DTOS media include a bootstrap-loading test that runs as part of the bootstrap-loading procedure. The test quickly checks the basic functions of the system hardware (excluding peripherals). When the test runs successfully, it displays the word TESTOK on the system operator's console. Otherwise, it halts the CPU before displaying the entire word. Thus, the portion of the displayed TESTOK word indicates the probable areas of failure, as shown in Table 8.1.

Message	Meaning
None *	When no part of the word displays (after 30 seconds), the following are probable areas of failure: A JMP, JSR, or STA instruction An indirect JMP or JSR TTO busy could not be cleared
T	Indicates that either an arithmetic/logic or an indexed memory-reference instruction failed. The following are the probable areas of failure: First: CPU board Second: memory subsystem
TE	Indicates that the test could not size memory. The most probable failure is the memory subsystem.
TES	Indicates that the data=address subtest failed. The most probable failure is the memory subsystem.
TEST	Indicates that the data=complement-of-address subtest failed. The most probable failure is the memory subsystem.
TESTO	Indicates that the memory-pattern subtest failed. The most probable failure is the memory subsystem.
TESTOK	Indicates that the entire program ran successflly.

Table 8.1 TESTOK message interpretation

**If your system operator's console is on device codes other than 10 and 11, see Table 8.2.*

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When TESTOK Is Not Displayed

In systems with the system operator's console on device codes other than 10 and 11, the bootstrap test runs, but the word TESTOK is not displayed. If the test finds no errors, the DTOS prompt (*) appears on the system operator's console after an interval of approximately 90 seconds (after DTOS loads and runs the initializing programs).

If the test detects an error, it halts the CPU and displays the PC contents.

You can find the probable areas of failure simply by matching the PC contents to a value in Table 8.2.

Contents of PC at Halt Time for Tape/Disk Versions		
Tape	**Disk**	**Meaning**
130 176	514 531	The following are probable areas of failure: A JMP, JSR, or STA instructions An indirect JMP or JSR TTO busy could not be cleared
204 212 214 217 223 225 227 231 234 236	537 545 547 552 556 560 562 564 567 571	Indicated that either an arithmetic/logic or an indexed memory-reference instruction failed. The following are the probable areas of failure: First: CPU board Second: memory subsystem
No halts during memory sizing.		Indicates that the test could not size memory. The most probable failure is the memory subsystem.
277 301	632 634	Indicates that the data = address subtest failed. The most probable failure is the memory subsystem.
323 325	713 715	Indicates that the data = complement-of-address subtest failed. The most probable failure is the memory subsystem.
346 356	736 746	Indicates that the memory-pattern subtest failed. The most probable failure is the memory subsystem.
No halts, no errors.		Indicates that the entire program ran successfully.

Table 8.2 Interpretation of PC contents

Memory Tests Within Bootstrap Test

Table 8.3 is intended to help you analyze a memory failure during the bootstrap test. When TES, TEST, or TESTO are the only parts of the TESTOK word that are displayed, look in Table 8.3 to determine the failing adddress and the good and bad data. All three memory tests run with memory unmapped (first 32K only).

Test Name	AC0	AC1	AC2
Data=address (TES)	Bad data	---	Failng address (good data)
Data= complement of address (TEST)	Complement of bad data	---	Failing address (complement this number to get the good data)
Memory pattern (TESTO)	Good pattern	Bad pattern	Failing address

Table 8.3 Value of ACs for memory tests

RELIABILITY/DIAGNOSTIC TEST FAILURE

Successful completion of the CPU self-test and the loading of DTOS indicates that the main portion of the NOVA 4/S or 4/X computer is operating properly and the input/output transactions between the disc (tape) drive controller, the CPU and memory were accomplished without fault.

After replacing the field replaceable units specified in Chapter 7, follow the steps listed below.

1. Remove all I/O controllers from the chassis, except the disc (tape) drive controller that is used as the DTOS loading device. Make sure the priority chain is maintained on the backpanel by placing jumpers across the slots that previously held I/O controllers. See the appropriate 5- or 16-slot installation data sheets. Also, make sure the load balancing rules for the 16-slot chassis are followed as shown in the 16-slot installation data sheets.
2. Remove the paddleboard connectors on the backpanel for all unused I/O controllers.
3. Load DTOS and run the failing reliability or diagnostic test.
4. If the test passes, add one I/O controller with its associated paddleboard connectors and rerun the test. Continue adding I/O controller boards until you isolate the malfunctioning controller.

If the above steps fail to correct the problem, call DGC Field Service for assistance.

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USER PROGRAM FAILURE

A user program failure after successful completion of the NOVA 4/S or 4/X reliability and diagnostic testing points to either a software problem or an I/O controller/device malfunction.

When this situation occurs, recheck any panic codes or error reports generated by the operating system. If these reports fail to indicate the source of the malfunction, follow the steps listed below.

1. Load DTOS
2. Enter LOAD N3MORT L on the system terminal keyboard. (This is the NOVA 3 Multi-programming Reliability Test, long version).
3. Allow the program to run for a minimum of 30 minutes. When the program detects an error, it sends an error message to the terminal (see sample program run summary shown earlier in the chapter).

   NOTE: *To stop the reliability test, press the Break key. This places the CPU in console mode.*

4. If an error occurs, run the diagnostics for the device indicated. See the appropriate device documentation. Take corrective action and rerun the user program that failed.

If the user program fails again, run the NOVA 2 Multi-programming Reliability Test, Peripheral version (DTOS mnemonic, N3MORT P), following the same steps as outlined above.

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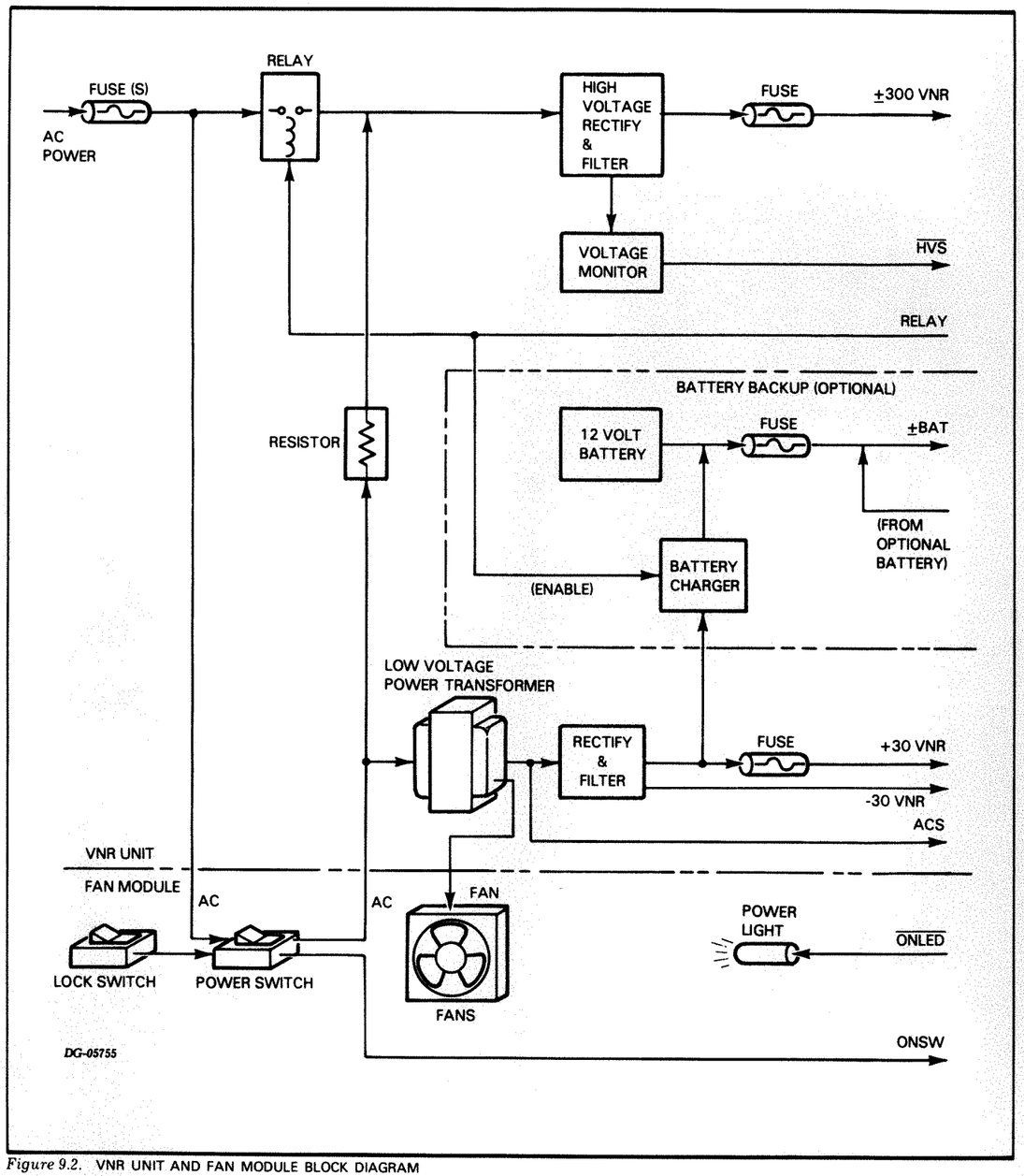

Figure 9.2. VNR UNIT AND FAN MODULE BLOCK DIAGRAM

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CHAPTER 9
16-SLOT POWER SUPPLY OPERATION

INTRODUCTION

The NOVA 4 16-slot power supply converts a 120 or 220/240 ac voltage source to the five regulated dc voltages required by the NOVA 4 computers. It also generates the system clocks. A battery backup option generates the regulated dc memory voltages from a 12 volt battery during an ac power failure.

The power supply consists of a VNR (voltage non-regulated) unit and a printed circuit board. The VNR unit supplies both non-regulated dc voltage to the power supply printed circuit board and ac voltage to the fan module via the internal cable. The power supply printed circuit board supplies the regulated dc voltages and system clocks to the system printed circuit boards via the backpanel.

A line cord with a 12-pin connector determines the operating voltage for the power supply.

FUNCTIONAL OVERVIEW

The 16-slot power supply uses a forward off-line switching regulator to produce the high power outputs required by the NOVA 4 computers. The major components of this off-line switching regulator are a rectifier and filter, a buck regulator, and a dc to dc converter.

Figure 9.1 shows the interconnection of these components.

The rectifier and filter convert power from the ac line to a high voltage dc source. The voltage varies with the line, but is typically 300 volts.

The buck regulator takes power from the filter and provides a constant voltage for the dc to dc converter. It monitors the output voltage, and delivers more current as the load increases to keep the output in regulation. The buck regulator includes a high voltage switch and a pulse width modulator. The switch alternately opens and closes the path between the filter and the dc to dc converter. The pulse width modulator opens and closes the switch at a constant 40 Khz rate, but varies the duty cycle (the ratio between the "on" time and the "off" time) to achieve regulation.

The dc to dc converter takes power from the buck regulator and produces the low voltage output. It includes an H-bridge chopper, a power transformer and a rectifier and filter. The chopper converts regulated dc power to a high voltage square wave for the power transformer. It does this by alternately closing a current path in one direction and then the opposite direction between the buck regulator and the transformer's primary winding. The transformer converts the high voltage/low current input to a low voltage/high current output, which the rectifier and filter convert back to dc.

To summarize, the off-line forward switching regulator performs five power transformations to convert 110/220VAC to 5VDC. As you scan Figure 9.1 from left to right, these transformations are:

120 or 220/240 VAC (rms) - 300VDC - 180VDC - 180VAC (peak) - 5VAC - 5VDC

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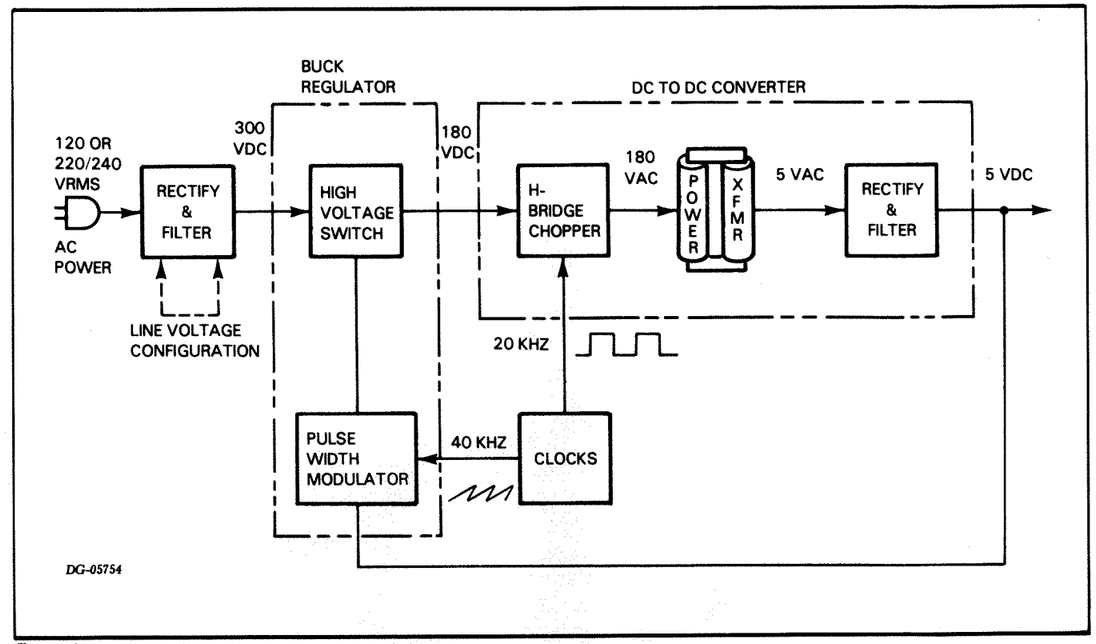

Figure 9.1. OFF-LINE SWITCHING REGULATOR BLOCK DIAGRAM

THEORY OF OPERATION

We can now take a look at the actual functional blocks included in the NOVA 4 power supply. These blocks are distributed between the VNR unit and the power supply circuit board. We will pay particular attention to the signals that flow in and out of these modules. This may help you to more easily and accurately identify a failing field replaceable unit.

VNR Unit

The VNR (voltage-non-regulated) unit provides high voltage and low voltage dc power for the power supply board. It can also generate battery backup power when that option is configured. Figure 9.2 shows the component parts of the VNR unit. The easiest way to understand them is to follow a power on/off sequence.

When you first turn on the power switch, current flows from the ac power line, through the line fuse(s) and to the low voltage power transformer. The transformer output is rectified and filtered to provide **+30VNR** and **-30VNR** for the control circuits on the power supply board. The transformer also powers the fans and sends a low voltage ac signal **(ACS)** to the real time clock circuits.

Current also flows through a very large resistor and into the high voltage rectifier and filter. The resistor limits the current flow as the filter capacitors charge, which keeps them from blowing the line fuse(s). When the capacitors are sufficiently charged, the voltage monitor asserts the high voltage sense **(HVS)** signal. The supply board responds by closing the relay, which short circuits the resistor. This makes full power available to the off-line switching regulator, which completes the power-on sequence.

When you turn the power switch off, the fan module negates the on-switch **(ONSW)** signal. Following a short delay (to allow the CPU to save critical information), the supply board opens the relay, which disconnects the VNR unit from the ac power line.

The optional battery backup module generates 12 volt dc power for special battery backup circuits on the power supply board. These circuits maintain critical memory voltages when a power failure occurs in order to save data stored in semiconductor memory modules. The battery can support four memory boards for 24 minutes. If that is not enough time, you can connect a larger external battery (an automotive battery, for example). The backup option includes a battery charger that is powered by the low voltage dc supply. The charger is enabled whenever the relay is turned on.

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Power Supply Board

The power supply board provides several regulated dc voltages for the computer chassis. It also generates several clock and status signals for the CPU. Figure 9.3 shows the component parts of the power supply board. It does not show the battery backup circuits; we will cover those later.

Before we examine the off-line switching regulator, we should look at some of the support circuits:

- The auxiliary supply regulators power all supply circuits except the main voltage regulators. They also provide an adjustable voltage reference. This reference sets the levels of all the output voltages (which eliminates the need for individual adjustments).
- The master clocks generate several clock signals for the CPU. They also provide a ramp signal for the pulse width modulator along with switch signals for the H-bridge chopper.
- The remote programming logic accepts data patterns from the CPU and directs the main voltage regulators to increase or decrease their output voltages **(RP1 - RP6).** It can also force an over-current fault **(RP8),** or lower the under-voltage thresholds **(RP7)** to prevent a power fault indication when the main output voltages are margined.
- The sequencing logic turns the off-line switching regulator on or off in several steps. The power-up sequence begins after the power switch is turned on **(ONSW),** the clocks start up **(RAMP)** and the high voltage bulk supply stabilizes **(HVS).** First the relay closes. Then the **+11SW** signal starts the H-bridge chopper. Finally the power-on **(PON)** signal starts the buck regulator. If the power switch is turned off, or a power or clock fault occurs, the sequencer opens the relay, stops the buck regulator and disables the H-bridge chopper.

We can now look at the main supply regulators. You will recognize all the main components of the off-line switching regulator at the top of Figure 9.3. Note that the remote programming inputs to the pulse width modulator **(RP1, RP2)** can margin the 5-volt output level up or down.

Unfortunately, the off-line switcher can produce only one regulated output (even if it could regulate all the outputs, they would change anyway when 5-volts was margined). So additional circuits are needed to regulate the remaining outputs. Because the power demands on these outputs are relatively low, linear series pass regulators are a practical choice. The 10-volt transformer winding powers the -5V regulator. Note that the remote programming feature can margin -5V up or down **(RP5, RP6).** The 14-volt transformer winding powers the +12V regulator. This component regulates ac power from the transformer before it rectifies it. Note that it can also be margined **(RP3, RP4).** The 3-volt regulator is powered by the 4-volt transformer winding. It rides on top of the 12-volt regulator to provide a +15-volt output. Although it cannot be margined separately, the +15-volt output level changes when +12V is margined.

The remaining circuits detect various kinds of power faults. They protect the supply from excessive loads, protect the computer from excessive voltages, and flag power failures.

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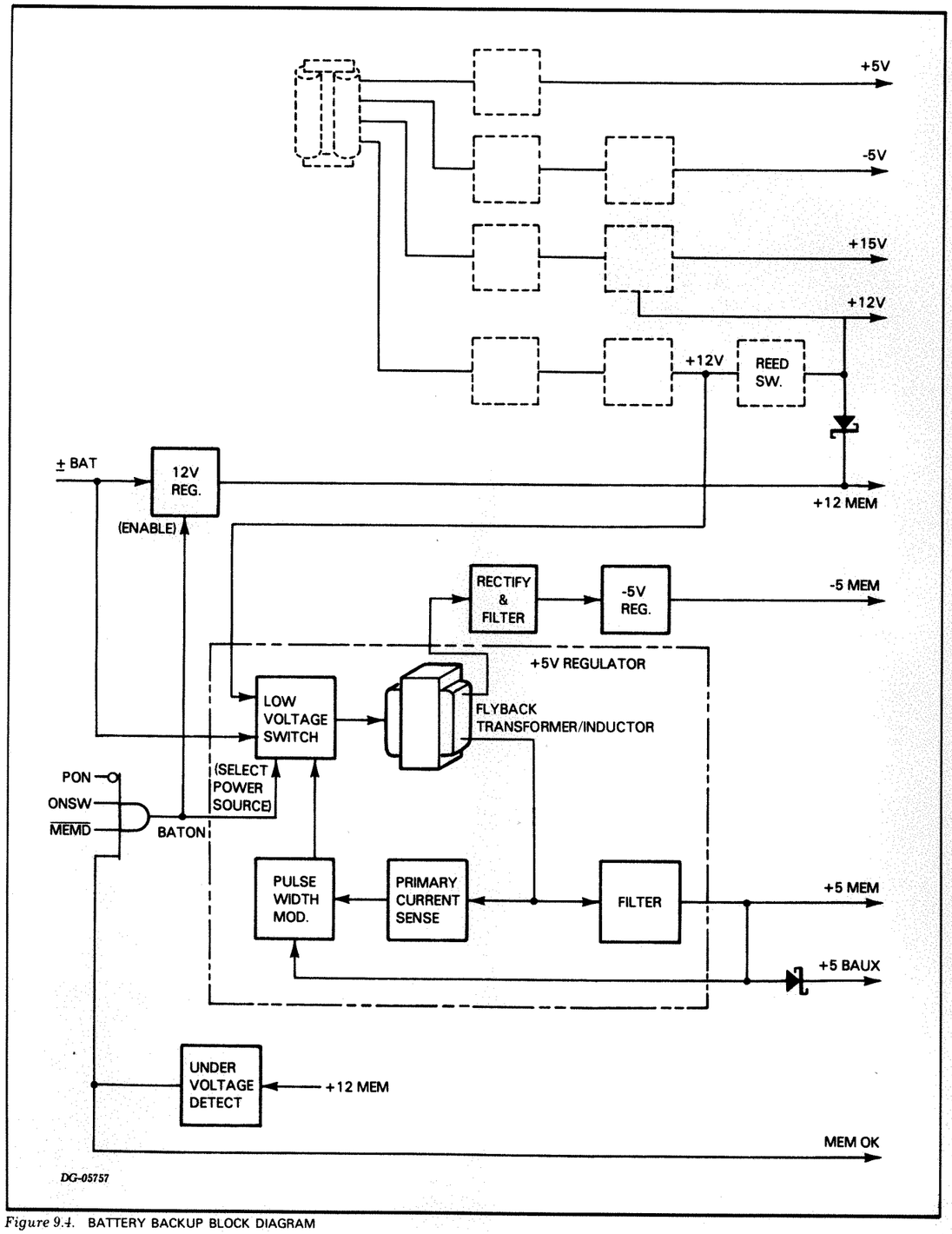

Figure 9.4. BATTERY BACKUP BLOCK DIAGRAM

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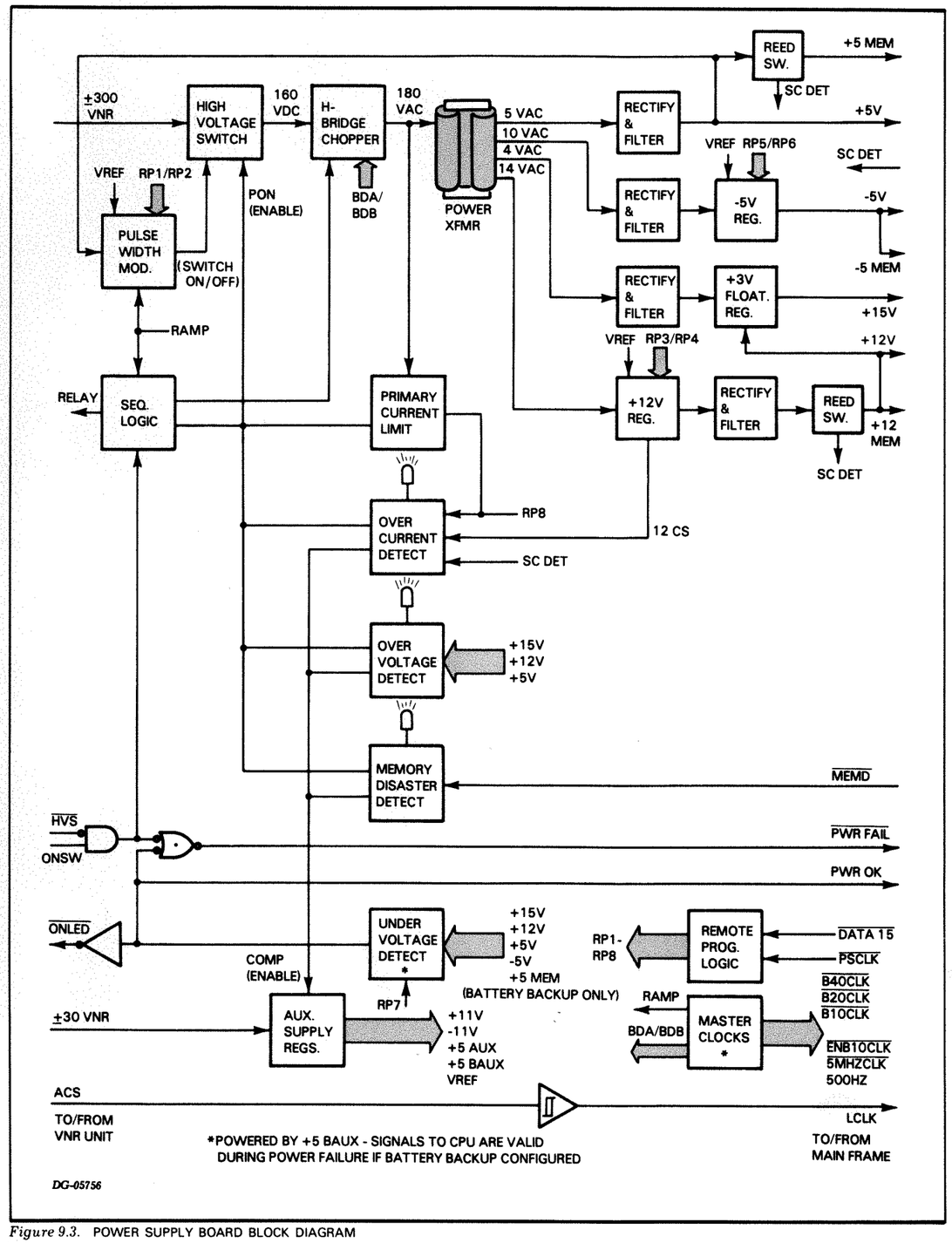

Figure 9.3. POWER SUPPLY BOARD BLOCK DIAGRAM

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The over-current detector monitors signals from several sources:

- The **12CS** signal indicates that the+12V regulator is overloaded.
- The **SC DET** signal indicates that there is a short circuit on one of the supply outputs (except -5V or -5 **MEM-P**). (Short circuits on+5V are detected on the backpanel.)
- The remote programming logic can assert the **RP8** signal to simulate an overcurrent fault. This lets the computer test the protection and battery backup circuits.
- The primary current limiter monitors the total current flow into all the loads. If an over-current condition occurs, the limiter immediately negates the **PON** signal and disables the buck regulator for the remainder of the 40 kHz clock cycle (the regulator turns on again at the start of the next cycle). This effectively reduces the duty cycle of the pulse width modulator, and so limits the amount of power delivered. (The supply actually goes into full current limiting when you first turn it on in order to charge the output filter capacitors). If the supply stays in current limiting too long, the limiter circuits assert the **RP8** signal.

Table 9.1
16-SLOT CHASSIS POWER SUPPLY
SPECIFICATIONS WITHOUT BATTERY BACKUP

Output	Voltage		Current	
	Min	Max	Min	Max
+5V	+5.10V	+5.20V	7.5A	100A
+12V	+11.8V	+12.2V	0	12.5A*
+15V	+14.5V	+15.5V	0	1.5A*
-5V	-4.9V	-5.1V	0	3A
-11V	-11.0V	-12.5V	0	0.02A
+5 MEM	+5.10V	+5.20V	0	4.5A*
+12 MEM	+11.8V	+12.2V	0	6A*
-5 MEM	-4.9V	-5.1V	0	0.3A*

** The sum of the currents on +12V, +15, and +12 MEM must NOT exceed 12.5 Amps.*

When an over-current fault occurs, the over-current light turns on and the detector negates the **PON** and **COMP** signals. This shuts down the entire supply. The detector re-enables the supply two seconds later. If the overload is still present, the detector shuts the supply down again. This process can continue for five more cycles. If the overload is still present, the supply shuts down for good.

The over-voltage detectors monitor the+15V,+12V and +5V outputs. If any of these outputs exceed a preset voltage level, the over-voltage light turns on and the detector shuts down the supply. (The -5V regulator has a built-in over-voltage protector. If a fault occurs, the protector clamps the -5V bus to less than -8 volts.)

The memory disaster detector monitors the **MEMD** signal from the memory cards. If any one of those cards loses -5 **MEM,** a critical memory voltage, memory disaster light comes on and the detector shuts down the supply.

The under-voltage detector monitors all of the output voltages. If any output falls below a preset level, the detector negates the **PWR OK** signal, turns off the power-on light and flags a power failure. (Note that a power failure is also flagged when the power switch is turned off or if the 300 VNR supply fails.)

Battery Backup

The battery backup option supports the memory voltages when a power failure occurs. It also powers the system clocks and the power status indicators and provides a **MEM OK** status flag to indicate that the memory voltages are ok. Figure 9.4 shows the parts of the battery backup option that are added to the power supply board.

Table 9.2
16-SLOT POWER SUPPLY
SPECIFICATIONS WITH BATTERY BACKUP

Output	Voltage		Current	
	Min	Max	Min	Max
+5V	+5.10V	+5.20V	7.5A	100A
+12V	+12.5V	+12.1V	0	12.5A*
+15V	+14.5V	+15.5V	0	1.5A*
-5V	-4.9V	-5.1V	0	3A
-11V	-11.0V	-12.5V	0	0.02A
+5 MEM	+4.8V	+5.1V	0.25A	4.5A*
+12 MEM	+11.7V	+12.1V	0	6A*
-5 MEM	-4.9V	-5.1V	0	0.3A

** The sum of the currents on +12V, +15V, +12 MEM, and 0.55 times the sum of the currents on+5 MEM and -5 MEM must NOT exceed 12.5 Amps.*

The battery backup option generates three voltages:+12 **MEM,** +5 **MEM-P,** and -5 **MEM-P** (note that the main supply regulators support these voltages when battery backup is not configured). It draws power from one of two sources. During normal operation, power comes from the +12V main supply output. If a failure occurs, power then comes from the battery. The backup option includes three voltage regulators along with some control circuits. To see how these circuits work, let us examine each voltage regulator and then follow a power failure sequence.

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The +12V regulator draws power directly from the battery. It is a simple linear series pass design and has no built-in protection circuits.

The +5V regulator draws power from either the +12V main supply or from the battery. It is a buck switching regulator and is very similar to the one in the main supply. When the low voltage switch turns on, current flows from the source, through the primary winding of the flyback transformer and on to the output. The pulse width modulator controls the duty cycle of the switch to regulate the output voltage. If too much current flows in the primary winding, the current limiter reduces the modulator's duty cycle.

The -5V regulator draws power from the +5V regulator via the flyback transformer. It is a simple linear series pass design and has built-in current limiting.

The battery on **(BATON)** signal controls battery backup operation. When the supply operates normally, the **PON** signal is asserted and the **BATON** is negated. This turns off the +12V regulator, and current flows from the +12V supply, through the Schottky diode and to the +12 **MEM** output. At the same time, the low voltage switch selects the +12V supply, which in turn powers the +5 **MEM-P** and -5 **MEM-P** outputs.

When a power failure occurs, the **PON** signal is negated. If the failure did not occur because of a memory disaster, the **BATON** signal is asserted. This switches the regulators over to battery operation. As long as the battery retains sufficient charge, the +12 **MEM** output stays in regulation and the **MEM OK** signal is asserted. But when the battery discharges to a dangerously low level, the under-voltage dectector negates the **MEM OK** signal, which in turn negates the **BATON** signal. This shuts the supply down entirely. (Note that the entire supply also shuts down when the power switch is turned off.)

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INTERCONNECTION WITH SYSTEM

The 16-slot power supply board communicates with the rest of the system via jacks 17 and 35 to the backpanel. Tables 9.3 through 9.5 list each signal either generated or received by the power supply board together with the jack locations of the signal. (Footnotes to all tables follow Table 9.5.)

Table 9.3
VOLTAGE SIGNALS

Signal	Jack Pin	Source	Destination *	Description
GND	J17 Even Pins J35 Pins 1-2, 4, 37-42	Power Supply	Backpanel	Power or logic ground
+5V	J17 Odd Pins	Power Supply	Backpanel	+5V Source
+5 MEM-P**	J35 Pins 33-36	Power Supply	Backpanel	Same as +5V if battery backup not configured
-5V	J35-27 J35-28	Power Supply	Backpanel	-5V Source
-5 MEM-P**	J35-19	Power Supply	Backpanel	Same as -5V if battery backup not configured
-11V	J35-25	Power Supply	Backpanel	EIA Interface voltage
+12V	J35 Pins 43-46	Power Supply	Backpanel	+12V Source
+12 MEM	J35 Pins 29-32	Power Supply	Backpanel	Same as +12V if battery backup not configured
+15V	J35-49 J35-50	Power Supply	Backpanel	+15V Source

Table 9.4
POWER SUPPLY STATUS SIGNALS

Signal	Jack Pin	Source	Destination *	Description
$\overline{\text{DATA 15}}$	J35-3	Power Supply	Backpanel	Data for voltage margining logic.**
$\overline{\text{MEMD}}$	J35-21	Backpanel	Power Supply	Failure on -5 MEM
MEMOK	J35-23	Power Supply	Backpanel	+12 MEM Voltage OK
$\overline{\text{ONLED-P}}$	J35-11	Power Supply	Backpanel	All DC output voltages OK
$\overline{\text{PWR FAIL}}$	J35-9	Power Supply	Backpanel	Power switch off or DC power failure
PWR OK	J35-16	Power Supply	Backpanel	All DC output voltages OK
$\overline{\text{SC DET}}$	J35-47	Power Supply	Backpanel	Short circuit on +5V, +5 MEM, +12V, or +12 MEM
		Backpanel	Power Supply	

Table 9.5
CLOCK SIGNALS***

Signal	Jack Pin	Source	Destination *	Description
$\overline{\text{B10CLK}}$	J35-6	Power Supply	Backpanel	10 MHZ Square wave
$\overline{\text{B20CLK}}$	J35-14	Power Supply	Backpanel	20 MHZ Square wave
$\overline{\text{B40CLK}}$	J35-10	Power Supply	Backpanel	40 MHZ Square wave
$\overline{\text{ENB10CLK}}$	J35-15	Power Supply	Backpanel	10 MHZ Pulse Train
LCLK	J35-17	Power Supply	Backpanel	50/60 HZ Square wave (AC line frequency)
$\overline{\text{PSCLK}}$**	J35-5	Backpanel	Power Supply	Strobes data pattern into voltage margining logic
$\overline{\text{5 MHZ CLK}}$	J35-7	Power Supply	Backpanel	5 MHZ Square wave
500 HZ	J35-18	Power Supply	Backpanel	500 HZ Square wave

* *See the 16-slot backpanel schematic, DGC No. 001-001563, or the 5-slot backpanel schematic, DGC No. 001-0001619, for the locations of signals on the backpanel.*

** *Some of the voltage signals are affected by the position of the diagnostic test plug on the backpanel. When the plug is inserted with the RUN side UP,* **$\overline{\text{PSCLK}}$** *is grounded. This disables the voltage margining logic. When the plug is inserted with the RUN side DOWN, the margining feature is enabled, and signal paths on the backpanel are altered as follows:*

- +5 **MEM-P** *no longer supplies power for the memory boards. Instead, they draw power from +5V. (This is necessary because the +5* **MEM-P** *voltage cannot be margined when battery backup is configured.)*
- -5 **MEM-P** *no longer supplies power for the memory boards. Instead, they draw power from -5V. (This is necessary because the -5* **MEM-P** *voltage cannot be margined when battery backup is configured.)*
- *The power-on light is disconnected as a reminder that the diagnostic test plug is not in the run position (that is, the RUN side is DOWN).*

*** *See Appendix D for a timing diagram of the system clock signals.*

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Test Points

Table 9.6 lists and explains the signals that appear on the test points (J1) on the front of the 16-slot power supply module.

Table 9.6
TEST POINT SIGNALS

Signal	J1 Pin	Description
+15V	8	Same as +15V supply on backpanel.
+12V	10	Same as +12V supply on backpanel.
+5V	15	Same as +5V supply on backpanel.
+5 AUX	7	Internal +5V supply for the power supply logic. (All supply functions are disabled when there is no +5 AUX. The VNR unit supplies +30V for the +5 AUX regulator.)
-5V	6	Same as -5V supply on backpanel.
VREF	14	Internal +5.80V reference for all regulators. (All internal and external supply voltages go out of regulation if VREF fails.)
GND	9	Power and logic ground.
HVS	4	High voltage from the VNR unit exceeds 260V. (All external supply voltages except -11V shut down if high voltage fails and battery backup comes on-line if configured.)
PON	11	External supply voltage regulators are enabled. (Goes to low state if HVS is in low state, an emergency condition such as a memory disaster occurs, an internal failure occurs, or power switch turned off. Battery backup comes on-line when PON goes to low state if power switch is on.)
POK	5	All external supply voltages ok.
$\overline{\text{PWR FAIL}}$	3	POK or HVS in low state or power switch is turned off.
$\overline{\text{PWM}}$	1	40 KHz pulse train from pulse width modulator. Clocks the main switching regulator which powers the external supply voltage regulators.
20 K	16	20 KHz square wave. Clocks the circuits which transform high voltage from the main switching regulator to low voltages for the external supply voltage regulators.
Q30-C	12	20 KHz drive signal in the power transformation circuits mentioned above.
Q29-C	13	20 KHz drive signal in the power transformation circuits mentioned above.
CURRENT	2	Voltage proportional to current flow in primary winding of power transformer that converts high voltage from the main switching regulator to low voltage for the external supply voltage regulators.

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CHAPTER 10
5-SLOT POWER SUPPLY OPERATION

INTRODUCTION

The NOVA 4 5-slot power supply converts a 100/120 or 220/240 ac voltage power source to the five regulated dc voltages required by the NOVA 4 computers. It also generates the system clocks. A battery backup option generates the regulated dc memory voltages from a 6V battery during an ac power failure.

The entire power supply, including the battery backup option and battery, is contained on a single printed circuit board. This board supplies the regulated dc voltages and system clocks to the printed circuit boards via the backpanel and provides ac power for the fan modules via the internal cable. A line cord with a 12-pin connector is used to determine the operating voltage for the power supply.

NOTE *Throughout this chapter, reference designators (e.g., C1 and T1) refer to the 5-slot power supply logic schematic, DGC No. 001-001616. Thus when reading this chapter, it is helpful to refer to the schematic.*

ORGANIZATION

The 5-slot power supply, like the 16-slot power supply, uses a forward off-line switching regulator to produce the high power voltage levels required by the NOVA 4 computers. The major components of the 5-slot power supply's off-line switching regulator are a VNR source, a pulse width modulation control, an inverter, and a dc regulator.

In addition to the off-line switching regulator, the 5-slot power supply includes a line filter, an auxiliary voltage supply, soft start logic, several voltage regulators, various fault detection circuits, and the system clock circuitry.

Figure 10.1 shows the interconnection of all these components.

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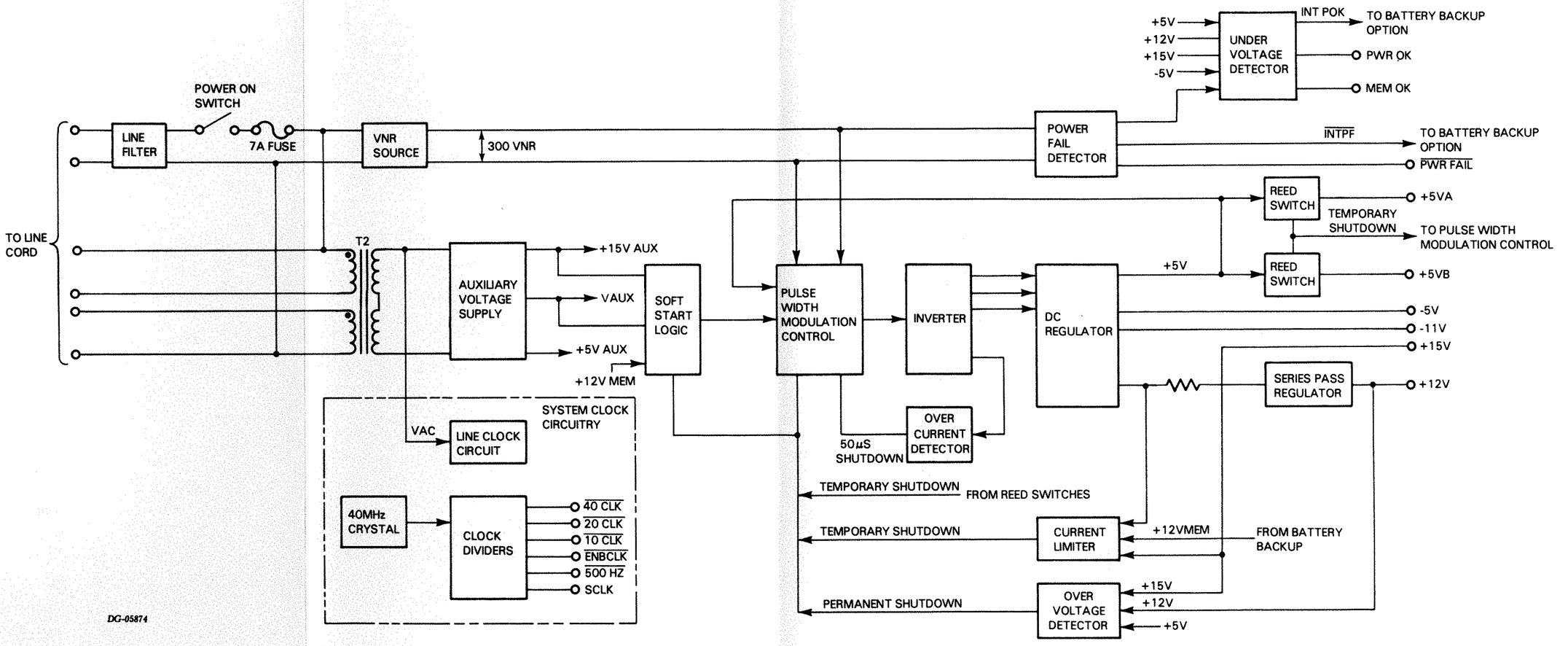

Figure 10.1. BASIC 5-SLOT POWER SUPPLY BLOCK DIAGRAM

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INTERCONNECTION WITH SYSTEM

The 5-slot power supply board communicates with the rest of the system via the jack J1 to the backpanel. Tables 10.3 through 10.5 list each signal either generated or received by the power supply board together with the jack locations of the signal. (Footnotes for all three tables follow Table 10.5.)

Table 10.3
VOLTAGE SIGNALS

Signal	Jack Pin	Source	Destination *	Description
GND	J1 PINS 1, 2, 4, 8, 35-42, 51, 52, 55-64, 79-88	Power Supply	Backpanel	Power or logic ground
+3V	J1-31, J1-32	Power Supply	Backpanel	+3V Source for backpanel bus terminators
+5VA	J1 PINS 91-100	Power Supply	Backpanel	+5V Source
+5VB	J1 PINS 67-76	Power Supply	Backpanel	+5V Source
+5 MEM	J1-33, J1-34	Power Supply	Backpanel	Same as +5V if battery backup not configured
-5V	J1-27 J1-28	Power Supply	Backpanel	-5V Source
-5 MEM	J1-19	Power Supply	Backpanel	Same as -5V if battery backup not configured
-11V	J1-24	Power Supply	Backpanel	EIA Interface voltage
+12V	J1 PINS 43-46	Power Supply	Backpanel	+12V Source
+12 MEM	J1 PINS 47-50	Power Supply	Backpanel	Same as +12V if battery backup not configured
+15V	J1-53, J1-54	Power Supply	Backpanel	+15V Source

Table 10.4
POWER SUPPLY STATUS SIGNALS

Signal	Jack Pin	Source	Destination *	Description
$\overline{\text{MEMD}}$	J1-21	Backpanel	Power Supply	Unused
MEM OK	J1-23	Power Supply	Backpanel	+5 MEM Voltage OK
$\overline{\text{ONLED-P}}$	J1-11	Power Supply	Backpanel	All DC output voltages OK
$\overline{\text{PWR FAIL}}$	J1-9	Power Supply	Backpanel	Power switch off or AC power failure
PWR OK	J1-16	Power Supply	Backpanel	All AC output voltages OK

Table 10.5
CLOCK SIGNALS**

Signal	Jack Pin	Source	Destination *	Description
$\overline{\text{B10CLK}}$	J1-6	Power Supply	Backpanel	10 MHZ Square wave
$\overline{\text{B20CLK}}$	J1-14	Power Supply	Backpanel	20 MHZ Square wave
$\overline{\text{B40CLK}}$	J1-10	Power Supply	Backpanel	40 MHZ Square wave
$\overline{\text{ENB10CLK}}$	J1-15	Power Supply	Backpanel	10 MHZ Pulse Train
LCLK	J1-17	Power Supply	Backpanel	50/60 HZ Square wave (AC line frequency)
$\overline{\text{5 MHZ CLK}}$	J1-7	Power Supply	Backpanel	5 MHZ Square wave
500 HZ	J1-18	Power Supply	Backpanel	500 HZ Square wave

* *See the 5-slot backpanel schematic, DGC No. 001-0001619, for the locations of signals on the backpanel.*

** *See Appendix D for a timing diagram of the system clock signals.*

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OPERATION

Off-Line Switching Regulator

The ac line voltage passes through a line filter to the VNR source where it is converted into a high dc voltage source. Although this dc voltage source varies from 259 VNR to 337 VNR with the line voltage, it is referred to as 300 VNR.

For 100/120 volt operation, the 300 VNR source rectifies and doubles the ac line source by connecting the junction of C1 and C2 (J1-9) to the neutral side of the line (J1-8) to provide a 300 VNR ac source; for 220/240 operation, it simply rectifies the ac line source.

The pulse width modulation control governs the operation of the inverter, and, in turn, of the dc regulator, by controlling the amount of power through the inverter. It opens and closes the power path once every 50 us (at a 20 KHz rate) and varies the ratio between the **open** time and the **closed** time (the duty cycle) in accordance with the variation on the +5V output. As the line voltage decreases or the +5V output load increases, the pulse width modulation control increases the **closed** time to transfer more power. In this way, the pulse width modulation control regulates the +5V output of the dc regulator.

Inverter

The inverter receives power from the 300 VNR source and transforms it into the ac voltage outputs which power the dc regulator. Its main component is transformer T1. T1 operates at 20 KHz with a variable duty cycle. Its maximum duty cycle is just less than 50 percent.

DC Regulator

The dc regulator receives ac voltages from the inverter and converts them into five different low dc voltage outputs: +5V, +12V, +15V, -5V, and -11V. It consists of rectifiers, an inductor L1, various filter circuits, and two voltage regulators.

The +5V output feeds back to the pulse width modulation control to regulate the duty cycle of the inverter, which, in turn, regulates all the outputs of the dc regulator.

The +12V output passes through a simple series pass regulator to produce a very well regulated +12V supply.

The +15V output is derived from T1 and the +5V in the dc regulator. It has no additional regulation. Since the pulse width modulation control removes all line variations from +5V, line variations will not affect the +15V output. Load variations on either the +5V or +15V outputs do affect the +15V output; however, their effect is relatively small.

The -5V and -11V receive additional regulation. The -5V output is regulated by a +5V three terminal regulator with its positive output grounded. The -11V output is regulated by a -12V three terminal regulator.

Auxiliary Voltage Supply

The ac line voltage powers the transformer T2 to produce an auxiliary voltage which functions as a control voltage for the power supply. This voltage goes through a 3-terminal voltage regulator to produce the +15V **AUX** and **VAUX.** The auxiliary voltage supply also produces +5V **AUX.** These voltages power most of the power supply circuits and also provide voltage references.

Soft Start Logic

The soft start logic allows the output voltages of the power supply to come up slowly and not overshoot when the system is powered up. Its main component is a capacitor with a large time constant. This capacitor must charge up before the pulse width modulation control can switch full power to the inverter. Most of the faults which shut down the pulse width modulation control also discharge this capacitor to allow the output voltages to come up slowly when the fault is removed.

Fault Detection Circuits

Various circuits monitor the operation of the power supply, checking for under voltage, over voltage, and over current conditions.

Under Voltage Detection

The under voltage detector continually monitors the +5V, -5V, +12V and the +15V outputs. When any of these outputs falls below the minimum operating level (see Table 10.1), it drives the **INT POK** signal to a low state.

Table 10.1
5-SLOT CHASSIS POWER SUPPLY SPECIFICATIONS

Output	Voltage Min	Voltage Max	Current Min	Current Max
+5V	+4.95V	+5.2V	5A	35A
+12V	+11.7V	+12.7V	0	5A*
+15V	+14.0V	+16.0V	0	5A*
-5V	-4.75V	-5.25V	0	1.5A
-11V	-11.0V	-12.5V	0	0.025A
+5 MEM	+4.95V	+5.2V	0	1A
+12 MEM	+11.3V	+12.7V	0	3.0A*
-5 MEM	-4.75V	-5.25V	0	0.05A

* *The sum of the maximum currents on the +12V, +15V, and the +12 MEM lines must NOT exceed 5 Amps. When battery backup is operating, +12 MEM draws a maximum current of 0.3A.*

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The power fail detector monitors the 300 VNR source for under voltage conditions on the ac line source. When it detects an under voltage condition, it pulls the **INTPF** to the low state. This signal drives the **PWR FAIL** signal to the low state to inform the system of an impending ac power failure. Approximately 22 ms later, **INT POK** is driven to the low state and stays in the low state for 155 ms or longer depending on how long the power failure lasts.

Whenever, **INT POK** goes to a low state, it drives **PWR OK** to a low state to reset the CPU. If battery backup is not present and the line fails, **PWR OK** stays in the low state, and later, it drives **MEM OK** to the low state. If battery backup is present, **PWR OK** stays in the low state and **MEM OK** stays in the high state as long as the battery lasts.

Over Voltage Detection

The over voltage detector protects against over voltage conditions on the +5V, +12V, and +15V outputs. If any of these outputs goes above the shut down level (see Table 10.2), this detector shuts the pulse width modulation control down permanently. The pulse width modulator control will not start again until the power supply is turned off and on again using the front console power switch. This over voltage fault also discharges the capacitor in the soft start logic to allow the voltage outputs to come up slowly when the system is powered up again.

Table 10.2
OVER VOLTAGE SHUTDOWN LEVELS

Output	Shutdown Voltage
+5V	5.66 +/- 1%
+12V	13.56 +/- 5%
+15V	17.3 +/- 5%

Over Current Detection

The main over current protection device is a cycle by cycle current limiter. It consists of a current sense transformer T3 in the inverter and an over current detector. The over current detector monitors the current in the secondary winding of this transformer. When the current flowing in this winding is too great, the over current detector shuts the pulse width modulation control down for one cycle (50 usec).

A secondary over current protection device, the current limiter, monitors the current on the +12V, +15V, and +12V **MEM** outputs. When the sum of the current on these three outputs goes above 5 Amps, the current limiter temporarily shuts down the pulse width modulation control. Although the shutdown time will vary with the load on these outputs, it is typically 0.5 sec. This over current fault also discharges the capacitor in the soft start logic to allow the voltage outputs to come up slowly when the fault condition is removed.

Two reed switches with a one turn winding around them function as current sensors for the +5V outputs. When the current on either of the two +5V outputs, goes above 20-25 Amps, the reed switches temporarily shut down the pulse width modulation control. This over current fault also discharges the capacitor in the soft start logic to allow the voltage outputs to come up slowly when the fault condition is removed.

BATTERY BACKUP OPTION

The battery backup option generates 6-volt dc power for the optional battery backup circuitry. This circuitry maintains the following critical memory voltages when a power failure occurs: +5V **MEM,** +12V **MEM,** and -5V **MEM.** These voltages are needed to refresh data stored on the dynamic RAM memory board. In addition, the battery backup circuitry powers the systems clocks and the front console lights, and provides a memory status signal **(MEM OK)** to indicate when the memory voltages are above the minimum operating levels.

Besides the battery, the battery backup option consists of a battery switch, a linear regulating circuit, a pulse width modulation control, flyback converter, several protection circuits, and a battery charger. Figure 10.2 shows the interconnection between these components.

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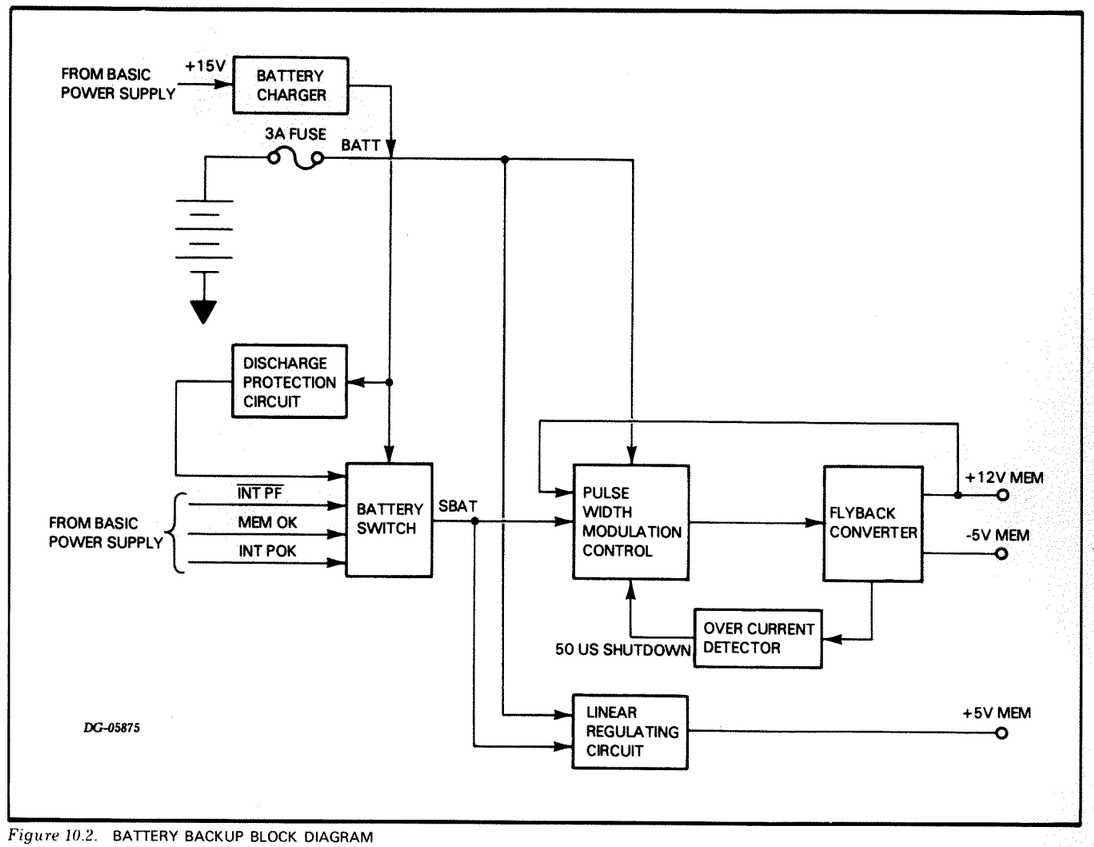

Figure 10.2. BATTERY BACKUP BLOCK DIAGRAM

Operation

The battery switch monitors the state of the **INT PF,** the **MEM OK,** and the **INT POK** signals to determine when ac power fails and when ac power recovers. If **INT PF** goes to the low state when **MEM OK** is in the high state, power is failing. The battery switch turns on the battery to supply power **(BATT)** to the rest of the battery backup circuitry. When the power recovers, **INT PF** goes to the high state. Shortly, the voltage outputs from the basic power supply come up and cause **INT POK** to go to the high state. If the battery is on when the outputs recover, **MEM OK** is in the high state; if the battery is off, **MEM OK** goes to the high state. When both **INT POK** and **MEM OK** are in the high state, the battery switch turns off the battery.

The linear regulating circuit regulates the battery's output voltage to produce the +5V **MEM** output. This circuit is a series pass regulator with current limiting.

The pulse width modulation control governs the amount of power supplied to the flyback converter. It opens and closes the power path between the battery and the flyback converter once every 50 us (at a 20 KHz rate) and varies the ratio between the **open** time and the **closed** time (the duty cycle) in accordance with the variation on the +12V **MEM** output of the flyback regulator. In this way, the pulse width modulation control regulates the +12V **MEM** output.

The flyback converter transforms the 6V dc output from the battery into a regulated +12V **MEM** output and a -5V **MEM** output.

The over current detector is a cycle by cycle current limiter. When it detects an over current condition, it shuts down the pulse width modulation control for one cycle (50 us).

The discharge protection circuit monitors the voltage level of the battery. When it drops below 5.4 volts, the discharge protection circuit turns off the battery to prevent it from degrading.

The battery charger recharges the battery when the basic power supply is operating.

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CHAPTER 11
CPU OPERATION

INTRODUCTION

The major component of the NOVA 4/S and 4/X CPU board is a central processing unit (CPU) which executes the NOVA instruction set enhanced with load and store byte instructions and, optionally, signed multiply and divide instructions. In addition, the CPU board includes a virtual console, an asynchronous communications interface, and a real time clock facility.

The CPU consists of a control processor and a data manipulation unit. The control processor governs system activities. It operates in two modes: run and console. In run mode, the control processor executes instructions stored in main memory. An integral prefetch processor (PFP) fetches the instructions from memory, and thus leaves the control processor free to execute one instruction immediately after another. In console mode, the CPU executes instructions stored in the virtual console. The data manipulation unit performs the arithmetic and logical operations required to carry out the instructions in both modes.

The CPU in a NOVA 4/X system also includes a Memory Management and Protection Unit (MMPU). This unit allocates physical memory in 1K blocks and provides both memory and I/O protection facilities. The MMPU is part of the control processor.

The virtual console allows a user to examine and modify the system's state using a terminal (system terminal) connected to the resident asynchronous interface.

The asynchronous interface is a programmed I/O controller which contains both a transmitter and a receiver. It provides full-duplex communication between a serial asynchronous terminal and the CPU.

The real time clock facility provides the system with four program selectable time bases. Both the asynchronous interface and the real time clock use a non-maskable interrupt facility.

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ORGANIZATION

The CPU board is organized around three major internal buses - **ALUIN, ALUOUT,** and **PFP** - and three system buses - **MEMIN, MEMOUT,** and **I/O.** The interconnection of these buses and the major units comprising the CPU board is shown in Figure 11.1.

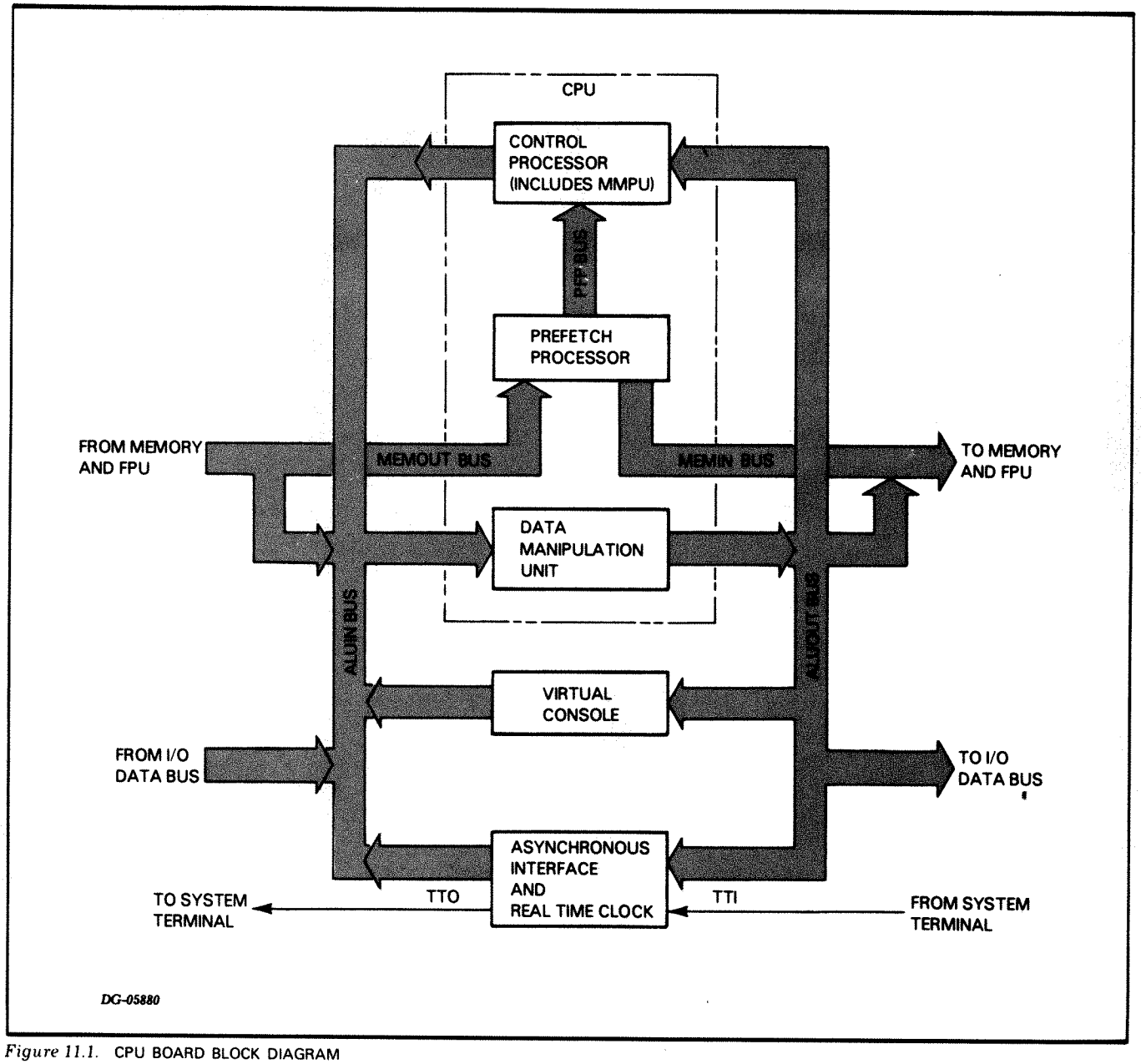

Figure 11.1. CPU BOARD BLOCK DIAGRAM

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Internal Buses

The 16-bit wide, unidirectional **ALUIN** bus carries information to the data manipulation unit from all major units of the CPU board.

The 16-bit wide, unidirectional **ALUOUT** bus carries information from the data manipulation unit to all major units of the CPU board.

The 16-bit wide, unidirectional **PFP** bus carries information to the CPU from the prefetch processor.

System Buses

The 17-bit wide **MEMIN** bus is a unidirectional path which carries both 17-bit memory addresses and 16-bit data words from the CPU to memory. When a floating point unit (FPU) is present, this bus also carries data words from the CPU to the FPU. Associated with the **MEMIN** bus are the following memory control lines: **MEMSTART** (start memory), **MEMSORRY** (memory busy), **MEMWRITE** (memory write operation), **INHSEL** (inhibit memory start), **BMEMCLK** (memory bus clock), and **MEMWAIT** (delay memory access).

The 16-bit wide **MEMOUT** bus is a undirectional path which carries 16-bit data words from the memory to the CPU. When an FPU is present, this bus also carries data words from the FPU to the CPU and from memory to the FPU.

The 48-line I/O bus carries information between the CPU and the system I/O controllers. This bus includes the 16-bit wide, bidirectional data bus (**DATA<0-15>**) which transfers all data. The remaining 32 lines carry programmed I/O, program interrupt, data channel, and system control signals.

OPERATION

Control Processor

The control processor executes the CPU instruction set by interpreting each assembly language instruction as a macroinstruction. It decodes the macroinstruction and then executes the appropriate sequence of microinstructions stored in the control store ROMs to perform the specified function. When executed, the microinstructions control the data paths and the operation of the data manipulation unit as well as the PFP, the memory, input/output, and the optional FPU.

Besides the PFP and the MMPU (NOVA 4/X only), the control processor consists of the following major units:

- System timing logic
- Instruction register
- Instruction decode logic
- Starting address generator
- Control store
- Microsequencer
- Microinstruction register
- Test multiplexors
- Microcode decode logic
- Memory control logic
- FPU control logic
- I/O logic

The interconnection of these units is shown in Figure 11.2.

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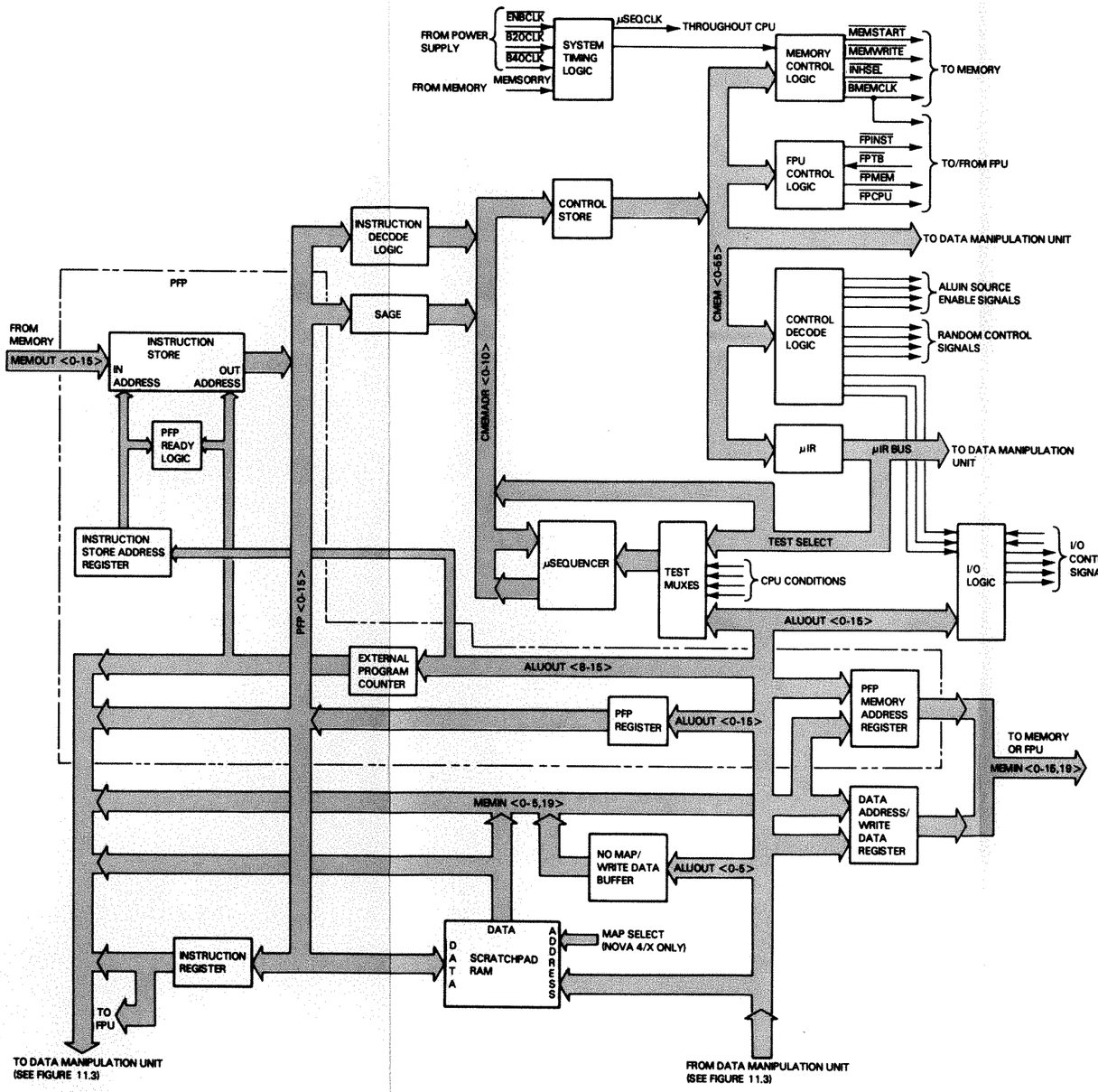

Figure 11.2. CONTROL PROCESSOR BLOCK DIAGRAM

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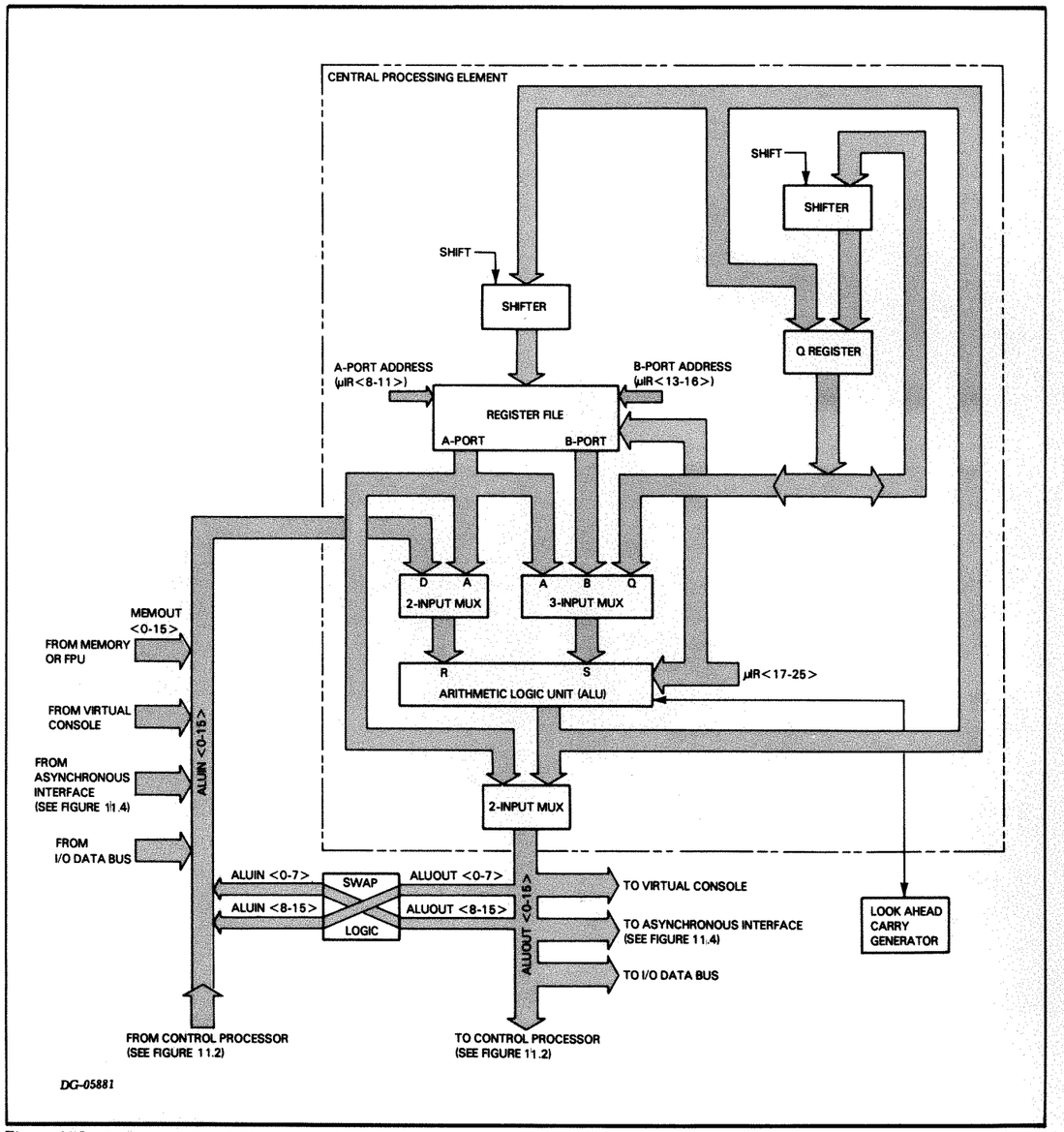

Figure 11.3. DATA MANIPULATION UNIT BLOCK DIAGRAM

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System Timing Logic

The system timing logic uses the clocks supplied by the power supply, **ENB10CLK, B20CLK** , and **B40CLK** , to generate the major CPU clocks: **USEQCLK** and **BMEMCLK. USEQCLK** is nominally a 200 ns clock which provides the microinstruction cycle timing. **BMEMCLK** is a 100 ns clock which provides the primary clock for the PFP and the memory control logic. When an FPU is present, both the control processor's FPU control logic and the FPU use **BMEMCLK.**

Instruction Register

The instruction register stores instructions which the control processor receives via the **PFP** bus from the PFP in run mode and from the virtual console in console mode.

Instruction Decode Logic

The instruction decode logic performs an initial decode of arithmetic-logic instructions (ALC), I/O instructions, and any other instructions which specify accumulators.

Starting Address Generator

The starting address generator (SAGE) determines the starting address for the next sequence of microinstructions to be executed and supplies this address to the control store. Before the control processor begins a new sequence of microinstructions, the SAGE examines the state of the following service request lines, which are listed in order of priority with the data channel having the highest priority and an instruction the lowest:

1. Data channel
2. I/O or non-maskable interrupt
3. Prefetch processor
4. Instruction

If a service request is present, the SAGE generates the appropriate starting address for the highest priority service required.

Control Store

The control store contains 56-bit microinstructions stored in fourteen 512 word by 8-bit ROMs organized in two banks of seven ROMs. A microinstruction is selected by the address supplied by the SAGE or the microinstruction sequencer. When selected, it is sent to microinstruction register and the control decode logic via the CMEM bus.

Microinstruction Register

The microinstruction register stores the microinstruction currently being executed. It distributes the control information contained in the microinstruction fields to the test multiplexors, the microinstruction sequencer, the memory control logic, the FPU control logic, and the data manipulation unit.

Microinstruction Sequencer

The microinstruction sequencer supplies the control store with the address of the next microinstruction in the sequence to be executed. It contains a microinstruction program counter and a four word stack.

Each microinstruction specifies a state change condition (a test) that determines what information the microinstruction register uses to generate the address. If the control processor finds that the specified state change condition is true, the microinstruction sequencer uses the data contained in the true state change field of the current microinstruction; otherwise, it uses the data appearing in the false state change field.

Since the state change condition is usually true, the microinstruction sequencer goes ahead and generates the address using the true state change field at the same time that the control processor checks the state condition. If the condition is found true, the microinstruction sequencer immediately provides the address to the control store. If the condition is found false, the microinstruction sequencer regenerates the address using the false change field. The microinstruction sequencer takes 200 ns to provide the address when the state change condition is true and 400 ns when the state change condition is false.

Test Multiplexors

The test multiplexors determine if the state change condition (test) specified by the current microinstruction is true or false. It uses information supplied by the control store, the microinstruction register, the PFP, the MMPU, the data manipulation unit, and the CPU logic governing the virtual console, FPU, and I/O operations.

Control Decode Logic

The control decode logic decodes portions of the microinstruction appearing on the **CMEM** bus to produce control information which governs the operation of most major units on the CPU board.

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Memory Control Logic

This control section initiates all memory read and write operations specified by the information appearing on the **uIR** bus. In a system with an FPU, memory read and write operations are also used to transfer data between the FPU and memory and between the CPU and the FPU (see Chapter 13).

As shown in Figure 11.2, the CPU is connected to the **MEMIN** bus via the PFP memory address register and data address/write data register. The CPU is connected to the **MEMOUT** bus via the PFP instruction store and the **ALUIN** bus.

The CPU allows 500 ns for a read operation and 200 ns for a write operation. Both operations proceed in two phases: an address transfer and a data transfer.

During the address phase of either a read or write operation, the memory control logic drives a 17-bit address onto the **MEMIN** bus and drives the **MEMSTART** signal to the low state. If the PFP is fetching an instruction, the address is supplied by the PFP memory address register; otherwise, the address is supplied by the address/write data register. If the memory is busy, it drives **MEMSORRY** to the low state to freeze the **BMEMCLK** until the memory is ready to start another read or write operation.

During the data transfer phase of a read operation, the CPU loads the 16-bit word appearing on the **MEMOUT** bus into the PFP's instruction store if the PFP requested the memory operation; otherwise, it loads the word into the central processing element of the data manipulation unit.

During the data transfer phase of a write operation, the CPU drives the data onto the **MEMIN** bus from the data address/write data register.

FPU Control Logic

In a system with an FPU, the FPU control logic initiates the operation of the FPU under the direction of information appearing on the uIR bus and status information from the FPU. It informs the FPU when the control processor decodes a floating point instruction and when the memory control logic initiates a memory operation to transfer data between the FPU and the CPU or memory (see Chapter 13).

I/O Logic

The I/O logic governs the operation of the I/O bus drivers and receivers which connect the CPU to the system I/O bus. It performs the following functions:

- Generates the I/O synchronizing signal, **RQENB**
- Receives both I/O interrupt requests and data channel requests
- Supports programmed I/O and data channel transactions

The NOVA 4's I/O bus adheres to the standard NOVA I/O bus conventions. For more information, see the *Interface Designer's Reference* (DGC No. 015-000031).

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PFP

The PFP fetches assembly language instructions from main memory when the control processor operates in run mode. It continues to fetch and store instructions until it is eleven instructions ahead of the instruction being executed by the control processor. In this way, the PFP makes it possible for the control processor to execute one instruction after another without having to wait for the instructions to be fetched from memory.

The PFP consists of the following major units:

- Instruction store
- PFP memory address register
- Instruction store address register
- External program counter
- PFP ready logic.
- PFP register

The instruction store consists of four 16-word by 4-bit, 2-port RAMs. It holds the instructions which the PFP fetches from memory until the control processor is ready to execute them.

The PFP memory address register supplies the 17-bit physical address of the instruction to be fetched from memory.

The instruction store address register supplies the address of the instruction store location which will hold the fetched instruction.

The external program counter selects the instruction stored in the instruction register. It contains the eight low-order bits of the logical memory address, while the seven high-order bits are stored in the internal program counter in the data manipulation unit.

The PFP ready logic determines when the PFP should fetch another instruction from memory.

The PFP register receives data from the **ALUOUT** bus and supplies it to the **PFP** bus. This data is either map data for the scratchpad RAM or an instruction from the virtual console ROM for the control processor.

MMPU

In run mode, the MMPU on the NOVA 4/X CPU board allocates memory in 1K word blocks and converts each 15-bit logical memory address into a 17-bit physical memory address. It also provides memory and I/O protection.

The two program maps and the two data channel maps, which the MMPU uses, are stored in the scratchpad RAM. When the MMPU is enabled during a CPU memory operation, the appropriate map in the scratchpad RAM supplies the seven high-order physical address bits via the **MEMININ** bus, while the data manipulation unit supplies the ten low-order bits via **ALUOUT<6-15>** . The scratchpad RAM also contains the program-accessible map violation data register and the map violation address register.

In the NOVA 4/S or in a NOVA 4/X when the MMPU is not enabled, the two high-order physical address bits, **MEMININ<19,0>** , are zero and the no map/write data buffer (not the scratchpad RAM) holds the remaining five high-order physical address bits and supplies them via **MEMININ<1-5>** . The data manipulation unit supplies the ten low-order bits via **ALUOUT<6-15>** . The no map/write data buffer also holds the six high-order data bits during a memory write operation and supplies them via **MEMININ<0-5>.**

Data Manipulation Unit

The data manipulation unit performs arithmetic and logical functions on the data designated by the microinstructions which are executed by the control processor. It consists of the following major components:

- Central processing element
- Look-ahead carry generator
- Swap logic

The interconnection of these components is shown in Figure 11.3.

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Table 11.4
MEMORY READ DATA

Signal	Back-panel Pin	Source	Destination	Description
MEMOUT0	A7	Memory FPU	CPU, FPU CPU	High-order data bit
MEMOUT1	A9	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT2	A13	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT3	A11	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT4	A15	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT5	A17	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT6	A21	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT7	A19	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT8	A26	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT9	A22	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT10	A12	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT11	A18	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT12	A28	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT13	A24	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT14	A16	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT15	A20	Memory FPU	CPU, FPU CPU	Low-order data bit
MEMOUT16	A31	Memory	–	Reserved for future use
MEMOUT17	A30	Memory	–	Reserved for future use
MEMOUT18	A29	Memory	–	Reserved for future use
MEMOUT19	A23	Memory	–	Reserved for future use
MEMOUT20	A27	Memory	–	Reserved for future use

Table 11.5
DATA CHANNEL AND INTERRUPT SIGNALS*

Signal	Back-panel Pin	Source	Destination	Description
$\overline{\text{DCHA}}$	A60	CPU	I/O	Data channel acknowledge
DCHI	B37	CPU	I/O	Data channel input
DCHO	B33	CPU	I/O	Data channel output
$\overline{\text{DCHMO}}$	B17	I/O	CPU	Data channel mode select
DCHR	B35	I/O	CPU	Data channel request
FASTDCH	A95	CPU	I/O	High speed device
INTA	A40	CPU	I/O, FPU	Interrupt acknowledge
$\overline{\text{INTR}}$	B29	I/O, FPU	CPU	Interrupt request
$\overline{\text{MSKO}}$	A38	CPU	I/O, FPU	Mask out
$\overline{\text{RQENB}}$	B41	CPU	I/O, FPU	Request synchronizing clock
$\overline{\text{SELB}}$	A82	I/O	CPU	Selected device busy
$\overline{\text{SELD}}$	A80	I/O, FPU	CPU	Selected I/O device done. From FPU only when an exponent overflow, exponent underflow, or divide by zero occurs.

* *See Interface Designer's Reference (DGC No. 015-000031), for more information on how the I/O signals function.*

Table 11.6
I/O DEVICE CODE*

Signal	Back-panel Pin	Source	Destination	Description
$\overline{\text{DS0}}$	A72	CPU	I/O, FPU	Device select bit 0
$\overline{\text{DS1}}$	A68	CPU	I/O, FPU	Device select bit 1
$\overline{\text{DS2}}$	A66	CPU	I/O, FPU	Device select bit 2
$\overline{\text{DS3}}$	A46	CPU	I/O, FPU	Device select bit 3
$\overline{\text{DS4}}$	A62	CPU	I/O, FPU	Device select bit 4
$\overline{\text{DS5}}$	A64	CPU	I/O, FPU	Device select bit 5

* *See Interface Designer's Reference (DGC No. 015-000031), for more information on how the I/O signals function.*

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The central processing element consists of four 4-bit microprocessor slices which are cascaded to form a 16-bit unit. The major sections of the central processing element are: a high-speed arithmetic/logic unit (ALU) and a 16-word by 16-bit register file. The register file contains sixteen registers including the following program-accessible registers: the four accumulators, the stack pointer, the frame pointer, and the map status register. It also includes the internal program counter which holds the seven high-order logical address bits of the instruction currently being executed.

The register file has two ports: A and B. Data in any of its registers can be read from the A port using the 4-bit A address field provided by the microinstruction register, **uIR<8-11>** . Similarily, data in any of the above 16 registers can be read from the B port using the 4-bit B address field provided by the microinstruction register, **uIR<13-16>** . When enabled, new data is always written into the register specified by the B address field.

The high speed ALU performs arithmetic and logical operations on the two 16-bit inputs designated R and S. The R input field is driven by a 2-input multiplexor while the S input field is driven by a 3-input multiplexor. The operation performed by the ALU is specified by information supplied by the microinstruction register, **uIR<17-25>.**

The look-ahead carry generator and the byte swap logic are support components for the central processing element.

Virtual Console

The virtual console resides in a 512-word by 16-bit ROM. This ROM also contains the assembly language instructions needed to implement the computer self-test.

When the control processor operates in console mode, the virtual console ROM supplies the instructions which the control processor executes. When the virtual console ROM is enabled, it places an instruction on the **ALUIN** bus. The instruction passes unchanged through the ALU to the **ALUOUT** bus and into the control processor via the **PFP** bus.

A 32-word scratchpad in the scratchpad RAM provides temporary storage for the control processor when it operates in console mode. When a console function addresses a physical memory location, the last location in the scratchpad (block 31) provides the seven high-order physical address bits. The scratchpad also contains the program-accessible data switch register.

Asynchronous Interface and Real Time Clock

The asynchronous interface is a programmed I/O controller which provides full-duplex communications between the CPU and a serial, asynchronous terminal via either a 20mA current loop or an EIA RS-232C communications line.

The interface contains the following major units:

- Universal asynchronous transmitter/receiver (UAR/T)
- Baud rate generator
- 8-bit status register

The interconnection between these units is shown in Figure 11.4.

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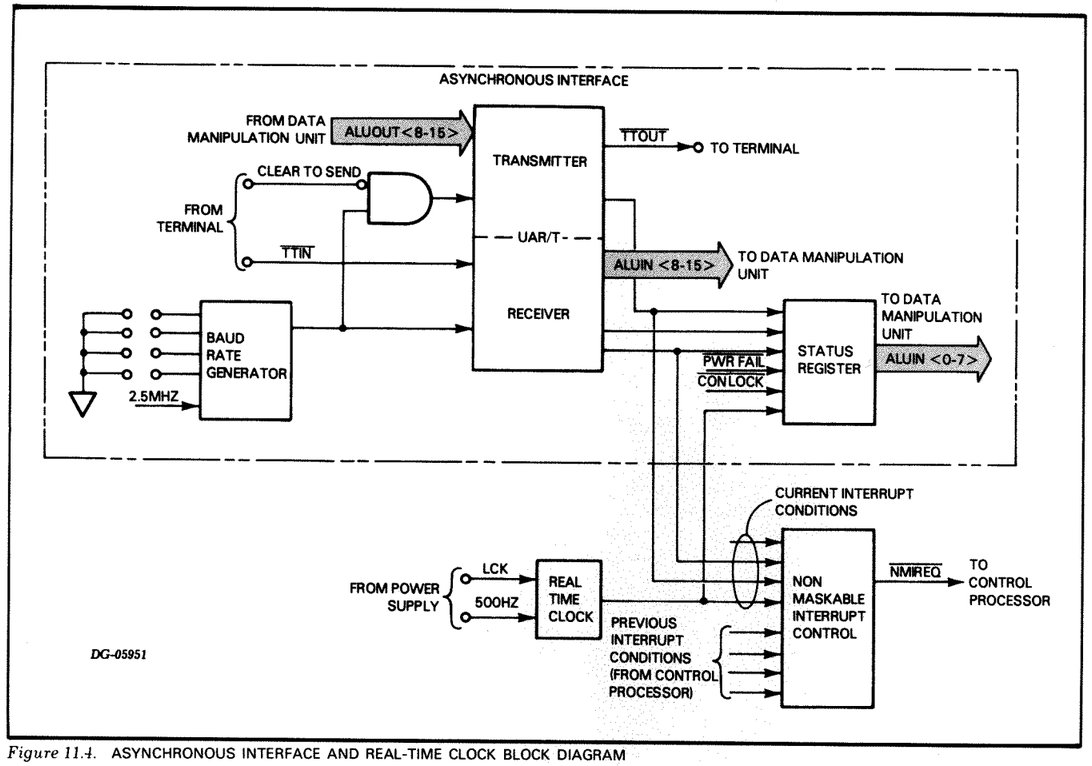

Figure 11.4. ASYNCHRONOUS INTERFACE AND REAL-TIME CLOCK BLOCK DIAGRAM

The UAR/T, which contains both a transmitter and receiver, is the communications link between the interface and the terminal. Jumpers select its line characteristics, including baud rate. The baud rate generator is driven by a 2.5MHz clock and supplies the UAR/T's transmitter and receiver clock inputs.

When communicating with the terminal, the UAR/T transmits and receives character codes in serial form. When communicating with the CPU under program control, the UAR/T's transmitter receives data in parallel form from the **ALUOUT** bus and the receiver places data in parallel form on the **ALUIN** bus.

The modem control signal, **Clear to Send,** is connected to the UAR/T's transmitter clock input line and inhibits data transmission when at the low state.

The real time clock facility provides four program-selectable time bases: power line frequency, 10 Hz, 100 Hz, and 1000 Hz.

Both the interface and the real time clock use a non-maskable interrupt control which is independent of the standard I/O interrupt facility. The Busy and Done flags and the priority mask bits for these devices are located in the I/O flag register, which resides in the data manipulation unit.

The non-maskable interrupt control compares previous interrupt conditions (which are stored in the RF register in the control processor) with current interrupt conditions. Whenever a current condition differs from the corresponding previous condition, the interrupt control generates a non-maskable interrupt. Next, the control processor equalizes both sets of interrupt conditions so the interrupt control can detect future interrupt conditions. An interrupt condition occurs when the interface receives a start bit, the receiver buffer contains a character, the transmitter buffer is empty, or the real time clock generates a pulse.

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INTERCONNECTION WITH SYSTEM

The CPU board communicates with the rest of the system via its A and B connectors to the backpanel. Tables 11.1 through 11.12 list each signal either generated or received by the CPU board together with the backpanel location of the signal.

Table 11.1
CLOCK SIGNALS*

Signal	Back-panel Pin	Source	Destination	Description
B10CLK	A35	Power Supply	CPU, Memory, FPU	10 MHZ Square wave
B20CLK	A39	Power Supply	CPU, Memory, FPU	20 MHZ Square wave
B40CLK	A36	Power Supply	CPU, Memory, FPU	40 MHZ Square wave
ENB10CLK	A49	Power Supply	CPU	10 MHZ Pulse train
LCLK	A88	Power Supply	CPU	50/60 HZ Square wave (AC line frequency)
PSCLK	A92	Power Supply	CPU	Strobes data pattern into voltage margining logic.
5MHZCLK	A47	Power Supply	CPU	5 MHZ Square wave
500HZ	A90	Power Supply	CPU	500 HZ Square wave

* *See Appendix D for a timing diagram of the system clock signals.*

Table 11.2
MEMORY CONTROL AND CLOCK SIGNALS

Signal	Back-panel Pin	Source	Destination	Description
BMEMCLK*	A43	CPU	Memory, FPU	10 MHZ Square wave MEMIN bus clock
INHSEL	B83	CPU	Memory	Prevents memory from starting up during a CPU-FPU data transfer.
MEMOK	A96	Power Supply	CPU	+12 MEM Voltage OK
MEMSORRY	A51	Memory	CPU	Memory busy
MEMSTART	A55	CPU	Memory	Memory operation starting
MEMWAIT	A32	–	CPU	Reserved for future use
MEMWRITE	A5	CPU	Memory	Memory Write operation starting

* *See Appendix D for a timing diagram.*

Table 11.3
MEMORY PHYSICAL ADDRESS WRITE DATA

Signal	Back-panel Pin	Source	Destination	Description
MEMIN0	B12	CPU FPU	Memory, FPU Memory	Physical address bit or high-order data bit
MEMIN1	B14	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN2	B16	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN3	B18	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN4	B26	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN5	B24	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN6	B22	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN7	B20	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN8	B28	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN9	B30	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN10	B32	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN11	B42	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN12	B47	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN13	B45	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN14	B44	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN15	B43	CPU FPU	Memory, FPU Memory	Low-order physical address bit or low-order data bit
MEMIN16	B10	CPU	Memory	Reserved for future use
MEMIN17	B9	CPU	Memory	Reserved for future use
MEMIN18	B8	CPU	Memory	Reserved for future use
MEMIN19	B7	CPU	Memory	High-order physical address bit

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256K Byte Board			128K Byte Board		64K Byte Board			32K Byte Board	
MODULE	BANK 0	BANK 1	MODULE	BANK 0	MODULE	BANK 0	BANK 1	MODULE	BANK 0
	0	200000		0		0	40000		0
	4	200004		4		4	40004		4
	10	200010		10		10	40010		10
	14	.		14		14	.		14
A	.	.	A	.	A	.	.	A	.
	.	.		.		.	.		.
	.	.		.		.	.		.
	.	.		.		.	.		.
	177774	377774		177774		37774	77774		37774
	1	200001		1		1	40001		1
	5	200005		5		5	40005		5
	11	200011		11		11	40011		11
	.	.		.		.	.		.
B	.	.	B	.	B	.	.	B	.
	.	.		.		.	.		.
	.	.		.		.	.		.
	177775	377775		177775		37775	77775		37775
	2	200002		2		2	40002		2
	6	200006		6		6	40006		6
	12	200012		12		12	40012		12
	.	.		.		.	.		.
C	.	.	C	.	C	.	.	C	.
	.	.		.		.	.		.
	.	.		.		.	.		.
	177776	377776		177776		37776	77776		37776
	3	200003		3		3	40003		3
	7	200007		7		7	40007		7
	13	200013		13		13	40013		13
	.	.		.		.	.		.
D	.	.	D	.	D	.	.	D	.
	.	.		.		.	.		.
	.	.		.		.	.		.
	177777	377777		177777		37777	77777		37777

Figure 12.1. ADDRESS INTERLEAVING

DG-05952

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Table 11.7
I/O FUNCTION SIGNALS*

Signal	Back-panel Pin	Source	Destination	Description
CLR	A50	CPU	I/O	Clear
DATIA	A44	CPU	I/O	Data in A
DATIB	A42	CPU	I/O	Data in B
DATIC	A54	CPU	I/O	Data in C
DATOA	A58	CPU	I/O	Data out A
DATOB	A56	CPU	I/O	Data out B
DATOC	A48	CPU	I/O	Data out C
IORST	A70	CPU	I/O	I/O Reset
IOPLS	A74	CPU	I/O	I/O Pulse
STRT	A52	CPU	I/O	Start

* *See Interface Designer's Reference (DGC No. 015-000031), for more information on how the I/O signals function.*

Table 11.8
I/O DATA BUS SIGNALS*

Signal	Back-panel Pin	Source	Destination	Description
$\overline{\text{DATA0}}$	B62	CPU I/O	I/O CPU	High-order data bit
$\overline{\text{DATA1}}$	B65	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA2}}$	B82	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA3}}$	B73	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA4}}$	B61	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA5}}$	B57	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA6}}$	B95	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA7}}$	B55	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA8}}$	B60	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA9}}$	B63	CPU I/O	I/O CPU	Data bit
$\overline{\text{DATA10}}$	B75	CPU I/O, FPU	I/O CPU	Data bit
$\overline{\text{DATA11}}$	B58	CPU I/O, FPU	I/O CPU	Data bit
$\overline{\text{DATA12}}$	B59	CPU I/O, FPU	I/O CPU	Data bit
$\overline{\text{DATA13}}$	B64	CPU I/O, FPU	I/O CPU	Data bit
$\overline{\text{DATA14}}$	B56	CPU I/O, FPU	I/O CPU	Data bit
$\overline{\text{DATA15}}$	B66	CPU I/O, FPU	I/O CPU	Low-order data bit

* *See Interface Designer's Reference (DGC No. 015-000031), for more information on how the I/O signals function.*

Table 11.9
FRONT CONSOLE SIGNALS

Signal	Back-panel Pin	Source	Destination	Description
$\overline{\text{CONRSTH}}$	B51	Front Console	CPU	From front console reset switch
$\overline{\text{CONLED}}$	B49	CPU	Front Console	CPU in run mode
$\overline{\text{CONPL}}$	B48	Front Console	CPU	Program load from device selected by CPU program load jumper register
$\overline{\text{CONLOCK}}$	B40	Front Console	CPU	CPU and power supply locked
$\overline{\text{CONRSTL}}$	B52	Front Console	CPU	From front console RESET switch
PWROK	A4	Power Supply	CPU, Memory, FPU	DC Voltages OK

Table 11.10
ASYNCHRONOUS INTERFACE SIGNALS

Signal	Back-panel Pin	Source	Destination	Description
CLEARTOSEND	A93	System Console	CPU	System console ready to receive data
$\overline{\text{ITTO}}$	A83	CPU	System Console	+15V Current loop voltage
$\overline{\text{READERRUN}}$	A89	CPU	System Console	Start reader
$\overline{\text{TTIN}}$	A94	System Console	CPU	Serial input
$\overline{\text{TTOUT}}$	A85	CPU	System Console	Serial output

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Table 11.11
FLOATING POINT UNIT SIGNALS
(16-SLOT BACKPANEL ONLY)

Signal	Back-panel Pin	Source	Destination	Description
IR1	A67	CPU	FPU	Instruction bit 1
IR2	A63	CPU	FPU	Instruction bit 2
IR14 (FIR3)	A69	CPU	FPU	Instruction bit 14
IR15 (FIR3)	A71	CPU	FPU	Instruction bit 15
IR5	A61	CPU	FPU	Instruction bit 5
IR6	A59	CPU	FPU	Instruction bit 6
IR7	A57	CPU	FPU	Instruction bit 7
IR8	A73	CPU	FPU	Instruction bit 8
IR9	A75	CPU	FPU	Instruction bit 9
$\overline{\text{FPABORT}}$	A91	CPU	FPU	Abort FPU operation
$\overline{\text{FPB}}$	A86	FPU	CPU	Reserved for future use
$\overline{\text{FPCPU}}$	A76	CPU	FPU	FPU-CPU data transfer
$\overline{\text{FPINST}}$	A84	CPU	FPU	FP instruction
$\overline{\text{FPMEM}}$	A78	CPU	FPU	FPU-memory data transfer
$\overline{\text{FPSKP1}}$	A79	FPU	CPU	FPU status signal
$\overline{\text{FPSKP2}}$	B13	FPU	CPU	Reserved for future use
$\overline{\text{FPTB}}$	A77	FPU	CPU	FPU busy executing previous FP instruction

Table 11.12
VOLTAGE SIGNALS (FROM POWER SUPPLY BOARD)

Signal	Backpanel Pins
GND	A1, A2, A14, A25, A33, A34, A37, A41, A45, A65 A99, A100 B1, B2, B21, B39, B50, B68, B80, B89, B92, B99, B100
+5V	A3, A4, A97, A98 B3, B4, B38, B97, B98
+15V	A10 B48, B84
+12V	B87, B88, B90
-11V	A77

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CHAPTER 12
MEMORY OPERATION

INTRODUCTION

The NOVA 4/S computer supports up to 64K bytes (32K words) of dynamic RAM, and can contain a maximum of two memory boards. The NOVA 4/X computer supports up to 256K bytes (128K words) of dynamic RAM, and can contain a maximum of four memory boards. RAM boards are available in the following sizes:

- 256K bytes (128K words)
- 128K bytes (64K words)
- 64K bytes (32K words)
- 32K bytes (16K words)

The RAMs on the 256K byte and 128K byte memory boards are organized as 16,384 x 1 bit. The RAMs on the 64K byte and 32K byte memory boards are organized as 4,096 x 1 bit.

Each board's RAM array is divided into four modules, A, B, C, and D. The modules on the 256K byte and 64K byte boards are further divided into two banks, 0 and 1. The modules on the 128K byte and 32K byte boards contain only one bank, bank 0.

On each memory board, the memory addresses are four-way interleaved between modules. This addressing scheme is shown in Figure 12.1. Note that the 128K byte and 32K byte boards contain only bank 0.

The four-way interleaving scheme on each board greatly increases the performance of the memory boards. The cycle time for a memory read or write operation is 400ns. However, due to four-way interleaving and separate timing generators for each module, read operations can be executed every 100ns and write operations every 200ns. This, of course, assumes that the memory board is addressed so that each module completes its 400ns cycle time before the module is addressed again. This condition is guaranteed when consecutive locations are addressed.

If an attempt is made to address a location within a module that is performing a memory operation, the memory board asserts the **$\overline{\text{MEMSORRY}}$** signal which is sent to the CPU.

The NOVA 4/S and 4/X CPUs allow 500ns for a read operation and 200ns for a write operation.

The timing diagram, figure 12.2, shows a write and a read operation issued to two consecutive locations contained in modules A and B.

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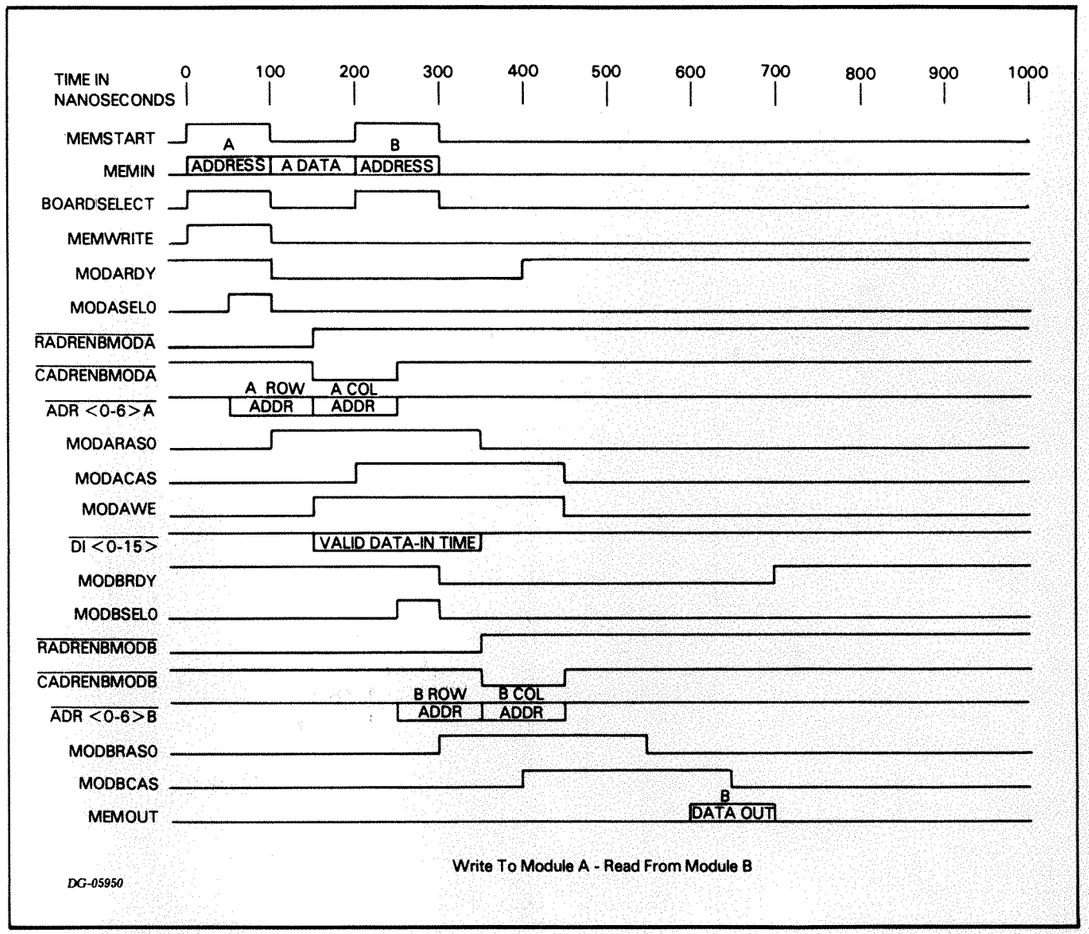

Write To Module A - Read From Module B

Figure 12.2. TIMING DIAGRAM

ARCHITECTURE

The block diagram, Figure 12.3, shows the principal components plus the control and data paths of the RAM memory boards. In addition to the RAM array, the memory boards contain:

- Two parallel data buses (memory in and memory out)
- An interface timing generator
- An input buffer
- An input data latch
- Board, module, and bank select logic
- Refresh logic
- Module A, B, C, and D timing logic
- Row and column address latches for each module
- Address drivers
- A four-to-one output multiplexer
- Four output registers
- A memory out bus driver

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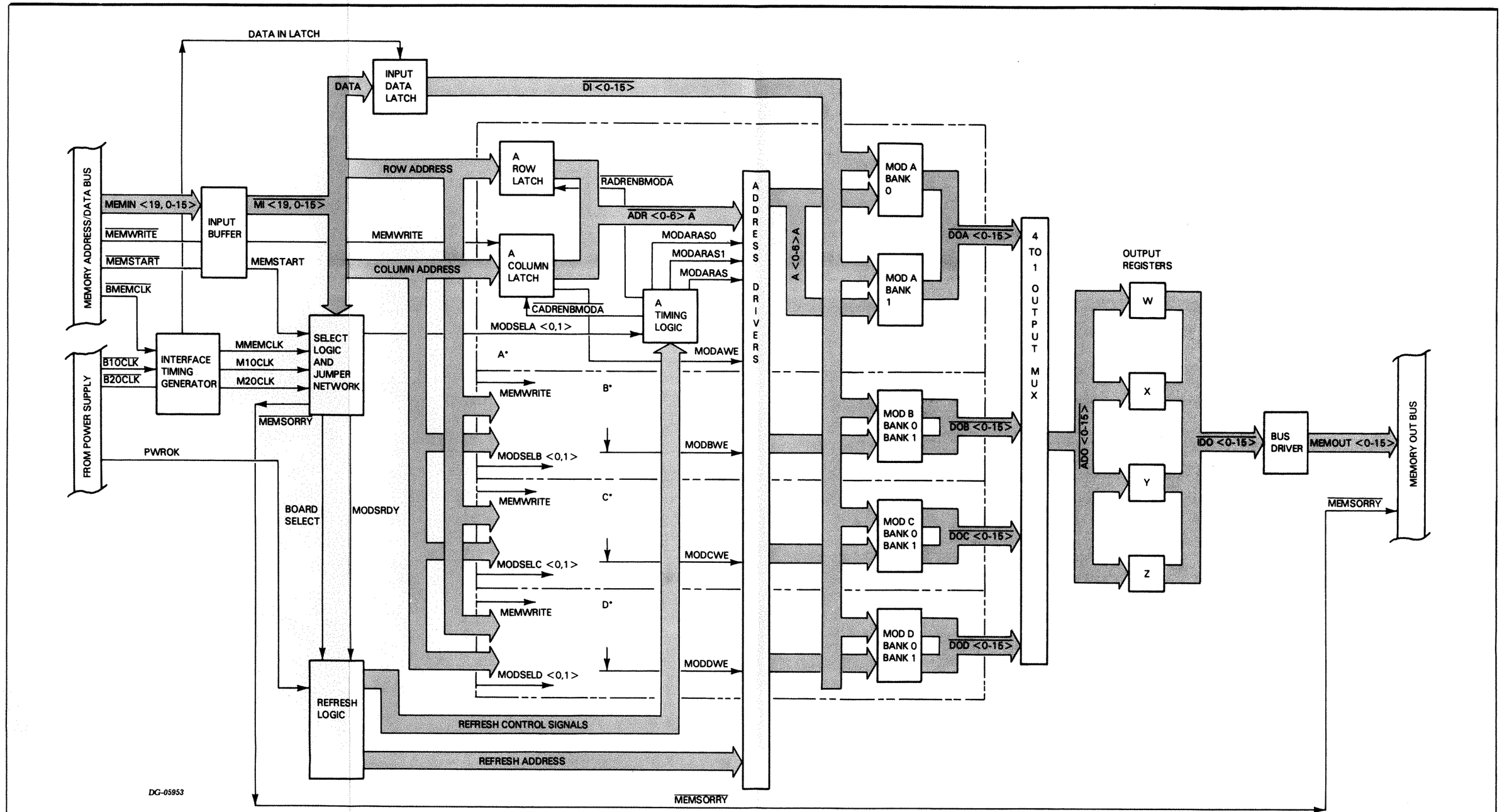

* MODULES A, B, C, AND D HAVE IDENTICAL TIMING AND ADDRESSING CIRCUITS.

** 128K BYTE AND 32K BYTE BOARDS CONTAIN BANK 0 ONLY.

Figure 12.3. MEMORY BLOCK DIAGRAM

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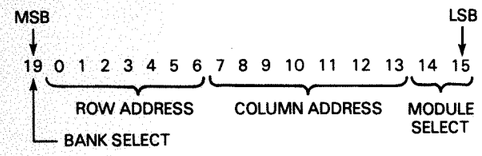
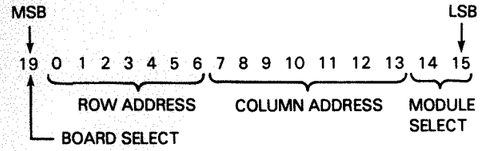
OPERATIONS

When the CPU asserts the **MEMSTART** signal, all the memory boards in the system examine the address appearing on the memory address/data bus **MEMIN <19,0-15>.** This 17-bit address is decoded by the different size memory boards as shown below.

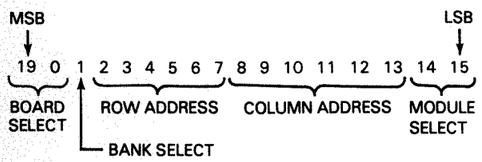
256K Byte Board



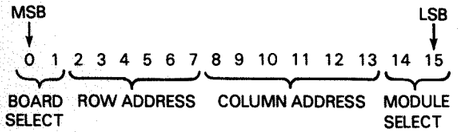
128K Byte Board



64K Byte Board



32K Byte Board



Since the 256K byte board is normally the only board in the system when present, it does not use the board select lines shown above for the remaining boards. The select logic for the remaining boards examines the board select lines to determine if the address is within the range assigned to the board by the on-board jumper configuration. If it is, the select logic then examines the module and bank select lines. Note that there are no bank select lines on the 128K byte and 32K byte boards since they contain only bank 0. The interface timing generator controls the select logic timing.

Each module has an associated row and column address latch. The information on the row address lines is transferred to the selected module's row address latch to determine the RAM array row address. The information on the column address lines is transferred to the selected module's column address latch to determine the RAM array column address. These addresses are both transferred to the selected module and bank on the **ADR <0-6> <A,B,C,D>** lines. The selected module's timing signals **RADRENBMOD <A,B,C,D>** and **CADRENBMOD <A,B,C,D>** transfer the row address first and then the column address.

In a memory write operation, the CPU asserts the **MEMWRITE** signal and the data on the memory in bus is transferred to the data latch. The **MEMWRITE** signal generates the **MOD <A,B,C,D> WE** signal via the selected column latch. This signal enables the output of the data latch, **DI <0-15>,** to be written into the addressed RAM location.

In a memory read operation, the data contained in the selected RAM location appears on the **DO <A,B,C,D> <0-15>** lines when the location is addressed. The four-to-one output multiplexer selects this data from the appropriate module and transfers it via the **ADO <0-15>** lines to one of four output registers. The output register transfers the data to the bus driver via the **IDO <0-15>** lines. The data is then driven onto the memory out bus **(MEMOUT <0-15>).**

The output registers called W, X, Y, and Z, are selected consecutively. For example, if register Y was used for a memory operation, register Z will be used for the next, and then register W and so on. This is done independently of the module and bank selection.

When all four modules are idle (i.e., ready to accept a read or write command), the refresh logic is enabled. Memory refreshing occurs approximately every 25μsec on the 32K byte and 64K byte boards and approximately every 13μsec on the 128K byte and 256K byte boards. The refresh logic generates refresh control signals which force the module control logic to enable the row address inputs of the RAM array. The refresh logic then generates its own address which are transferred to the RAM array.

If the system has the battery back-up option, a power fail causes the low state of the **PWROK** signal to enable the refresh logic. Refreshing is the only operation performed by the memories when the system is being powered by the battery back-up option. If the system does not have the battery back-up option, then a power fail causes the contents of memory to be lost.

If the CPU selects a memory board while it is performing a read, write or refresh operation, the memory board sends the **MEMSORRY** signal to the CPU.

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INTERCONNECTION WITH SYSTEM

The memory communicates with the rest of the system via its A and B connectors to the backpanel. Tables 12.1 through 12.6 list each signal either generated or received by a memory board together with the backpanel location of the signal.

Table 12.1
CLOCK SIGNALS*

Signal	Backpanel Pin	Source	Destination	Description
$\overline{\text{BMEMCLK}}$	A43	CPU	Memory, FPU	10 MHZ square wave MEMIN bus clock
$\overline{\text{B10CLK}}$	A35	Power Supply	CPU, Memory, FPU	10 MHZ square wave
$\overline{\text{B20CLK}}$	A39	Power Supply	CPU, Memory	20 MHZ square wave

* *See Appendix D for a timing diagram of the system clock signals.*

Table 12.2
MEMORY CONTROL SIGNALS

Signal	Backpanel Pin	Source	Destination	Description
$\overline{\text{INHSEL}}$	B83	CPU	Memory	Prevents memory from starting up during a CPU-FPU data transfer.
$\overline{\text{MEMD}}$	B96	MEMORY	Power Supply	DC power failure on -5 MEM.
$\overline{\text{MEMSORRY}}$	A51	MEMORY	CPU	Memory busy
$\overline{\text{MEMSTART}}$	A55	CPU	Memory	Memory operation starting
$\overline{\text{MEMWAIT}}$	A32	–	CPU	Reserved for future use
$\overline{\text{MEMWRITE}}$	A5	CPU	Memory	Memory Write operation starting

Table 12.3
MEMORY PHYSICAL ADDRESS/WRITE DATA

Signal	Backpanel Pin	Source	Destination	Description
MEMIN0	B12	CPU FPU	Memory, FPU Memory	Physical address bit or high-order data bit
MEMIN1	B14	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN2	B16	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN3	B18	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN4	B26	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN5	B24	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN6	B22	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN7	B20	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN8	B28	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN9	B30	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN10	B32	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN11	B42	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN12	B47	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN13	B45	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN14	B44	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN15	B43	CPU FPU	Memory, FPU Memory	Low-order physical address bit or low-order data bit
MEMIN16	B10	CPU	Memory	Reserved for future use
MEMIN17	B9	CPU	Memory	Reserved for future use
MEMIN18	B8	CPU	Memory	Reserved for future use
MEMIN19	B7	CPU	Memory	High-order physical address bit

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Table 12.4
MEMORY READ DATA

Signal	Backpanel Pin	Source	Destination	Description
MEMOUT0	A7	Memory FPU	CPU, FPU CPU	High-order data bit
MEMOUT1	A9	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT2	A13	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT3	A11	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT4	A15	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT5	A17	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT6	A21	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT7	A19	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT8	A26	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT9	A22	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT10	A12	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT11	A18	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT12	A28	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT13	A24	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT14	A16	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT15	A20	Memory FPU	CPU, FPU CPU	Low-order data bit
MEMOUT16	A31	Memory	–	Reserved for future use
MEMOUT17	A30	Memory	–	Reserved for future use
MEMOUT18	A29	Memory	–	Reserved for future use
MEMOUT19	A23	Memory	–	Reserved for future use
MEMOUT20	A27	Memory	–	Reserved for future use

Table 12.5
POWER STATUS SIGNAL

Signal	Backpanel Pin	Source	Destination	Description
PWROK	A4	Power Supply	CPU, Memory, FPU	DC voltages OK

Table 12.6
VOLTAGE SIGNALS (FROM POWER SUPPLY BOARD)

Signal	Backpanel Pins
GND	A1, A2, A14, A25, A33, A34, A37, A41, A45, A99, A100 B1, B2, B21, B39, B50, B68, B80, B89, B92, B99, B100
+5V	A3, A4, A97, A98 B3, B4, B97, B98
+5 MEM	B93, B94
-5 MEM	B91
+12 MEM	B70, B71, B72

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CHAPTER 13
FLOATING POINT UNIT OPERATION

INTRODUCTION

The NOVA 4 floating point unit (FPU) executes the NOVA 3 floating point instruction set with the exception of the diagnostic instructions. These instructions are replaced by microdiagnostics which are resident on the FPU board. The microdiagnostics are run when the computer starts to execute the floating point diagnostic program (see Chapter 7).

The floating point instruction set performs operations on numbers supplied by main memory or two registers on the FPU board: the floating point accumulator (FPAC) and the temporary register (TEMP). These numbers are either 4 bytes wide (single precision) or 8 bytes wide (double precision). Each number consists of a sign, a fractional part called the mantissa, and an exponent. The first byte contains the sign and the exponent; the remaining bytes contain the mantissa.

The CPU initiates the operation of the FPU and controls all data transfers between itself, the FPU, and memory. When a floating point instruction uses a number stored in memory or stores a number in memory, the CPU synchronizes the operations of the FPU and memory to transfer the number. Similarly, when a floating point instruction uses data in a CPU accumulator or stores data in a CPU accumulator, the CPU synchronizes its operation with the FPU's operation to transfer the data.

The FPU consists of three processors: a control processor, a mantissa processor, and an exponent processor. The **MEMIN** and **MEMOUT** buses provide the data paths between the FPU, the CPU, and memory. Figure 13.1 shows the interconnection between the three processors and these buses.

The control processor governs the overall functioning of the FPU. It synchronizes the operation of the FPU with the operations of the CPU and memory and controls the interaction between the exponent processor and the mantissa processor. It also contains the program-accessible FPU status register.

The exponent and mantissa processors perform arithmetic and logical operations on the exponent and mantissa portions of floating point numbers, respectively. These processors share two program accessible registers: the floating point accumulator, FPAC, and the temporary register, TEMP. The exponent processor contains the sign and exponent part of the registers while the mantissa processor contains the mantissa part.

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OPERATION

When the CPU decodes a floating point instruction, it sends instruction bits **IR<1,2,5-9,14,15>** to the FPU and drives **FPINST** low. Then, it checks the **FPTB** signal line. If this line is low, the FPU is still busy executing a previous floating point instruction. In this case, the CPU waits until the FPU is done before initiating any data transfers which may be required by the new instruction. While it is waiting, the CPU can only service data channel requests.

When **FPINST** goes to the low state, the FPU's control processor loads instruction bits **IR<1,2,5-9,14,15>** from the CPU into its instruction register (FIR). If the FPU is busy with a previous instruction, it drives **FPTB** to the low state to notify the CPU that it is busy. When it is done, it drives **FPTB** to a high state. Next, it decodes the bits in the FIR and begins to execute the appropriate sequence of microinstructions to perform the function specified by the instruction.

If the control processor is still executing the previous floating point instruction when **FPINST** goes to the low state, **FPTB** will be in the low state. In this situation, the FPU's control processor loads the instruction bits into the FIR, but waits until it is done with the previous instruction and has driven **FPTB** to the high state before decoding these instruction bits.

The FPU initiates an interrupt request only when an exponent underflow, exponent overflow, or a divide by zero condition is detected, the interrupt disable flag is reset, and bit 13 of the status register (inhibit fault interrupt bit) is 0. If the FPU has detected an exponent underflow, exponent overflow, or a divide by zero condition, it will drive **SELD** to a low state in response to an *I/O Skip* instruction to its device code, 76_8.

Data Transfers to and from the FPU

All data transfers between the FPU and memory occur during the data phase of a memory read or write operation. The CPU initiates the data transfer in the same way it starts any memory read or write operation by driving **MEMSTART** to the low state. It informs the FPU of the upcoming memory-FPU transfer by driving **FPUMEM** to the low state. During the address phase of the memory operation, the CPU sends the address to memory via the **MEMIN** bus. During the data transfer phase, the FPU either sends the data word to memory via the **MEMIN** bus (write operation) or receives the data word from memory via the **MEMOUT** bus (read operation).

All data transfers between memory and the FPU are either single or double precision numbers. A single precision number requires two consecutive memory operations; a double precision number requires four consecutive memory operations.

During the transfer of a number from memory to the FPU, the FPU loads the contents of the **MEMOUT** bus into its working register. The working register stacks the words up one at a time until it has received the entire number. The working register sends the first word (containing the sign and exponent) to the exponent processor where the word is stored in the 2-port exponent register file. It sends the remaining words to the mantissa ALU.

Once the number is in the exponent and mantissa processors the FPU begins to perform the specified functions. Under the direction of the control processor, the exponent processor manipulates the sign and the exponent and the mantissa processor manipulates the mantissa of the number involved. When the operation is completed, the result is stored in the FPAC register.

During the transfer of a number from the FPU to memory, the sign and exponent part of the FPAC pass from the 2-port exponent register file through the B-exponent shifter and onto the **MEMIN** bus. Next, the mantissa part of the FPAC passes, one word at a time, from the mantissa ALU through the working register and onto the **MEMIN** bus.

All transfers of data between the FPU and the CPU take place during the data phase of a memory read or write operation. In this case, when the CPU initiates the memory operation, it inhibits memory by driving **INHSEL** to a low state and notifies the FPU of the upcoming FPU-CPU transfer by driving **FPUCPU** to a low state.

The timing for data transfers between the FPU and the CPU or memory is given in Figure 13.2.

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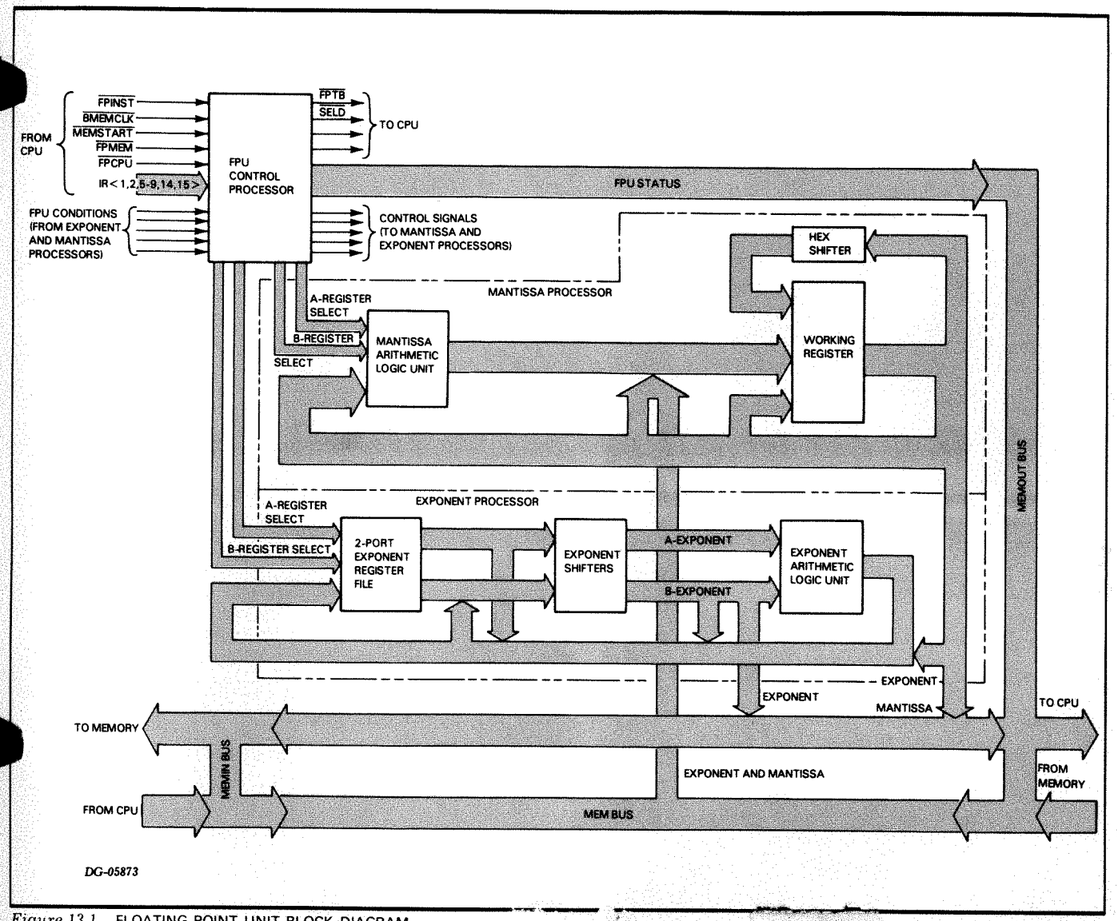

Figure 13.1. FLOATING POINT UNIT BLOCK DIAGRAM

Phil-
I hope this helps.
One of the last
pages has a back-
plane layout showing
the 777 hookup pins.
(Drawing 001001563) Refer
to CPU print 001001624
for Electronics involved
Good luck
Ralph

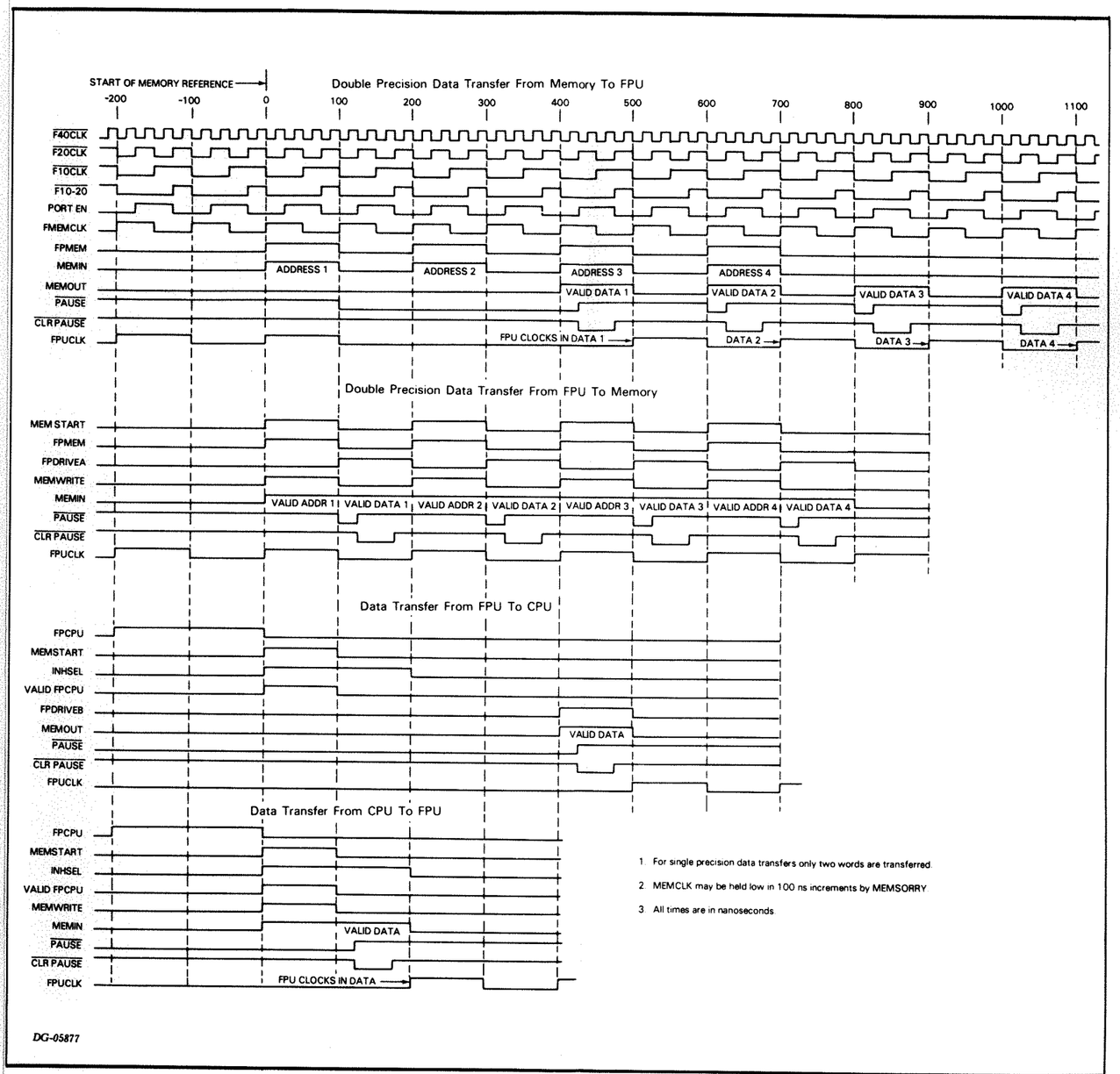

Figure 13.2. TIMING DIAGRAM FOR DATA TRANSFER BETWEEN MEMORY AND THE FPU OR CPU

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INTERCONNECTION WITH SYSTEM

The FPU board communicates with the rest of the system via its A and B connectors to the backpanel. Tables 13.1 through 13.9 list each signal either generated or received by the FPU board together with the backpanel locations of the signal.

Table 13.1
CLOCK SIGNALS*

Signal	Backpanel Pin	Source	Destination	Description
B10CLK	A35	Power Supply	CPU, Memory, FPU	10 MHZ Square wave
B20CLK	A39	Power Supply	CPU, Memory, FPU	20 MHZ Square wave
B40CLK	A36	Power Supply	CPU, Memory, FPU	40 MHZ Square wave
BMEMCLK	A43	CPU	Memory, FPU	10 MHZ Square wave MEMIN bus clock

* *See Appendix D for a timing diagram of the system clock signals.*

Table 13.2
FPU CONTROL SIGNALS

Signal	Backpanel Pin	Source	Destination	Description
IR1	A67	CPU	FPU	Instruction bit 1
IR2	A63	CPU	FPU	Instruction bit 2
IR14 (FIR3)	A69	CPU	FPU	Instruction bit 14
IR15 (FIR4)	A71	CPU	FPU	Instruction bit 15
IR5	A61	CPU	FPU	Instruction bit 5
IR6	A59	CPU	FPU	Instruction bit 6
IR7	A57	CPU	FPU	Instruction bit 7
IR8	A73	CPU	FPU	Instruction bit 8
IR9	A75	CPU	FPU	Instruction bit 9
FPABORT	A91	CPU	FPU	Abort FPU operation
FPB	A86	CPU	FPU	Reserved for future use
FPCPU	A76	CPU	FPU	FPU-CPU data transfer
FPINST	A84	CPU	FPU	FPU instruction
FPMEM	A78	CPU	FPU	FPU-Memory data transfer
FPSKP1	A79	FPU	CPU	FPU status signal
FPSKP2	B13	FPU	CPU	Reserved for future use
FPTB	A77	FPU	CPU	FPU busy executing previous FP instruction

Table 13.3
MEMORY PHYSICAL ADDRESS/WRITE DATA

Signal	Backpanel Pin	Source	Destination	Description
MEMIN0	B12	CPU FPU	Memory, FPU Memory	Physical address bit or high-order data bit
MEMIN1	B14	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN2	B16	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN3	B18	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN4	B26	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN5	B24	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN6	B22	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN7	B20	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN8	B28	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN9	B30	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN10	B32	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN11	B42	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN12	B47	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN13	B45	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN14	B44	CPU FPU	Memory, FPU Memory	Physical address bit or data bit
MEMIN15	B43	CPU FPU	Memory, FPU Memory	Low-order physical address bit or low-order data bit

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Table 13.4
MEMORY READ DATA

Signal	Back-panel Pin	Source	Destination	Description
MEMOUT0	A7	Memory FPU	CPU, FPU CPU	High-order data bit
MEMOUT1	A9	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT2	A13	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT3	A11	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT4	A15	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT5	A17	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT6	A21	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT7	A19	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT8	A26	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT9	A22	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT10	A12	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT11	A18	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT12	A28	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT13	A24	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT14	A16	Memory FPU	CPU, FPU CPU	Data bit
MEMOUT15	A20	Memory FPU	CPU, FPU CPU	Low-order data bit

Table 13.5
DATA CHANNEL AND INTERRUPT SIGNALS*

Signal	Back-panel Pin	Source	Destination	Description
INTA	A40	CPU	I/O, FPU	Interrupt Acknowledge
$\overline{\text{INTR}}$	B29	I/O, FPU	CPU	Interrupt request
$\overline{\text{MSKO}}$	A38	CPU	I/O, FPU	Mask out
$\overline{\text{RQENB}}$	B41	CPU	I/O, FPU	Request enable (synchronizing clock)
$\overline{\text{SELD}}$	A80	I/O, FPU	CPU	Selected I/O device done. From FPU only when an exponent overflow, exponent underflow, or divide by zero occurs

* *See Interface Designer's Reference (DGC No. 015-000031), for more information on how the I/O signals function.*

Table 13.6
I/O DEVICE CODE*

Signal	Back-panel Pin	Source	Destination	Description
$\overline{\text{DS0}}$	A72	CPU	I/O, FPU	Device select bit 0
$\overline{\text{DS1}}$	A68	CPU	I/O, FPU	Device select bit 1
$\overline{\text{DS2}}$	A66	CPU	I/O, FPU	Device select bit 2
$\overline{\text{DS3}}$	A46	CPU	I/O, FPU	Device select bit 3
$\overline{\text{DS4}}$	A62	CPU	I/O, FPU	Device select bit 4
$\overline{\text{DS5}}$	A64	CPU	I/O, FPU	Device select bit 5

* *See Interface Designer's Reference (DGC No. 015-000031), for more information on how the I/O signals function.*

Table 13.7
I/O DATA BUS SIGNALS*

Signal	Back-panel Pin	Source	Destination	Description
DATA10	B75	CPU I/O, FPU	I/O CPU	Data bit 10
DATA11	B58	CPU I/O, FPU	I/O CPU	Data bit 11
DATA12	B59	CPU I/O, FPU	I/O CPU	Data bit 12
DATA13	B64	CPU I/O, FPU	I/O CPU	Data bit 13
DATA14	B56	CPU I/O, FPU	I/O CPU	Data bit 14
DATA15	B66	CPU I/O, FPU	I/O CPU	Data bit 15

* *See Interface Designer's Reference (DGC No. 015-000031), for more information on how the I/O signals function.*

Table 13.8
POWER STATUS SIGNAL

Signal	Back-panel Pin	Source	Destination	Description
PWROK	A4	Power Supply	CPU, Memory, FPU	DC Voltages OK

Table 13.9
VOLTAGE SIGNALS (FROM POWER SUPPLY BOARD)

Signal	Backpanel Pins
GND	A1, A2, A14, A25, A33, A34, A37, A41, A45, A65, A99, A100 B1, B2, B21, B39, B50, B68, B80, B89, B92, B99, B100
+5V	A3, A4, A97, A98 B3, B4, B97, B98

PART III
MECHANICAL REPLACEMENT PROCEDURES

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FAN REPLACEMENT FOR 5-SLOT CHASSIS

1. Power down the system, open the rear cabinet door, and unplug the AC source from the cabinet.
2. Remove the power cord connector and any I/O cables.
3. Remove the front panel (see p.118.)
4. Remove the 8 screws which secure the chassis to the cabinet rails. There are 2 screws per rail.
5. Slide the chassis out from the front of the cabinet. The slides will support it until it is about half way out of the cabinet.

CAUTION *The chassis weighs about 50 lbs (about 23 kgs) fully loaded. You may need help.*

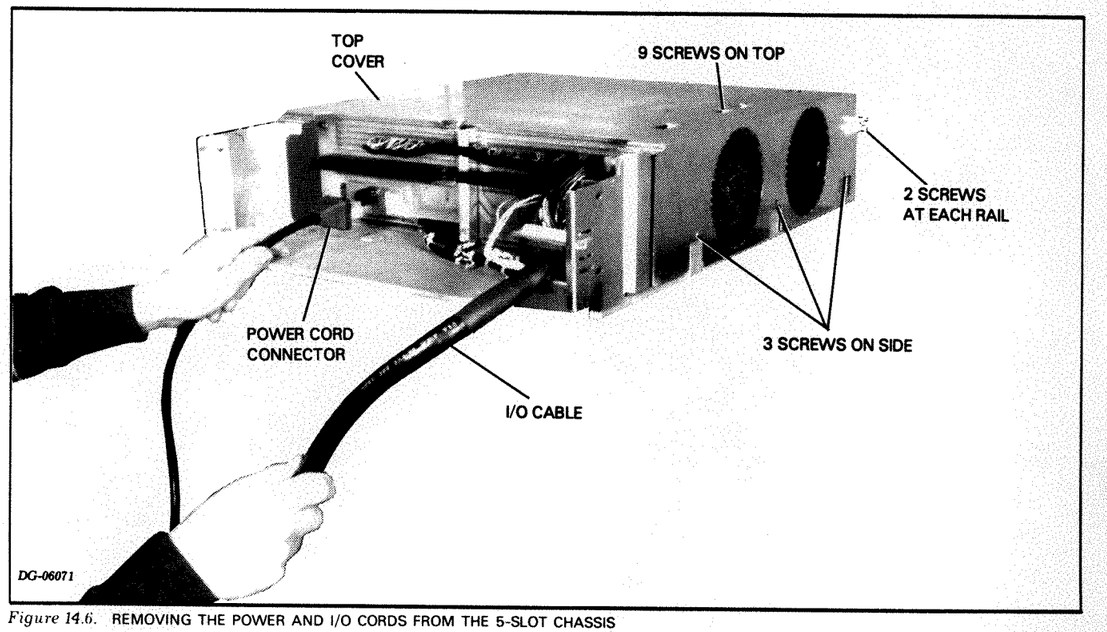

Figure 14.6. REMOVING THE POWER AND I/O CORDS FROM THE 5-SLOT CHASSIS

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CHAPTER 14
REMOVING AND INSTALLING FRU'S

INTRODUCTION

This chapter gives step by step instructions for removing and installing the FRUs. Please abide by the following in all procedures:

- Metric tools must be used in all the procedures.
- Extreme caution must be used in procedures that involve opening the power supply units. After powering down the system, you must wait AT LEAST 5 MINUTES before proceeding with the replacement.
- Do not attempt to remove or replace any component not included in these procedures.

Fifteen procdures are described in the order listed below.

1. Front Panel Replacement
2. Fan and Fan Module Replacement for 16-Slot Chassis
3. Fan Replacement for 5-Slot Chassis
4. Console PC Board Replacement for 16-Slot Chassis
5. Console PC Board Replacement for 5-Slot Chassis
6. PC Board Replacement
7. CPU Board Replacement
8. Memory Board Replacement
9. Power Supply PC Board Replacement
10. VNR Unit Replacement
11. Paddleboard and Terminator Replacement
12. 16-Slot Wiring Harness Replacement
13. 5-Slot Wiring Harness Replacement
14. Backpanel Replacement for 16-Slot Chassis
15. Backpanel Replacement for 5-Slot Chassis

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FRONT PANEL REPLACEMENT

There are two versions of the front panel assemblies, locking and nonlocking.

1. To remove a locking front panel, find the metal latch located at the center of each side of the front panel. Using a screw driver, push them in towards each other. This will release the latches and allow the front panel to be pulled off.

   To remove a nonlocking front panel, find the release button located at the center of each side of the front panel. Push them in towards each other and remove the front panel.

2. To replace either a locking or nonlocking front panel, line up the guide pins and push until it locks in place.

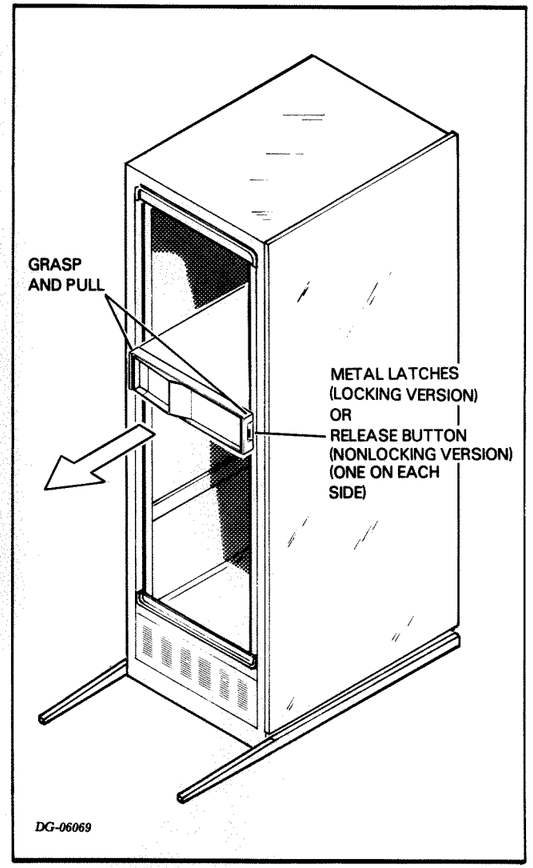

Figure 14.1. REMOVING THE FRONT PANEL

FAN AND FAN MODULE REPLACEMENT FOR 16-SLOT CHASSIS

1. Power down the system.
2. Remove the front panel. (See Front Panel Replacement procedure.)
3. Remove 2 nuts with lock washers located to the left of the console switches.
4. Grasp the fan module at the top and bottom and pull out.

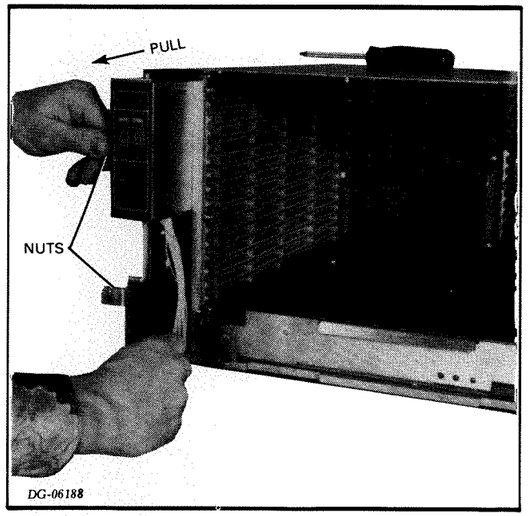

Figure 14.2. REMOVING THE FAN MODULE FROM A 16-SLOT CHASSIS

5. To remove a fan:
   a. Place the fan module on a table with the fan side up.

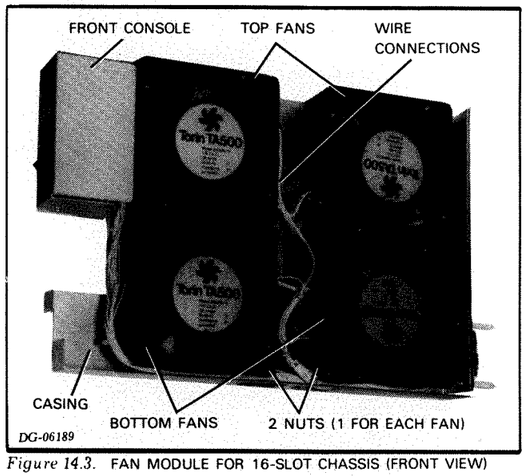

Figure 14.3. FAN MODULE FOR 16-SLOT CHASSIS (FRONT VIEW)

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   b. Disconnect the two wires from the faulty fan. Note the position of the wire connectors on the fan so you can install the new fan in the same position.
   c. If the fan is a bottom fan, remove the nut, lock washer, and the washer on the stud holding the fan to the casing.
   d. Turn the module over and remove the self-tapping screw(s) holding the fan to the casing. (1 screw for a bottom fan; 2 screws for a top fan.)

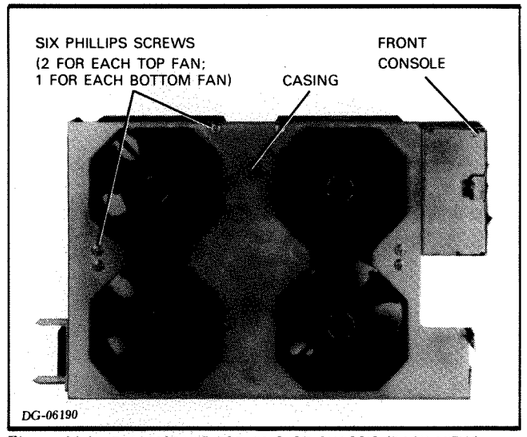

Figure 14.4. FAN MODULE FOR 16-SLOT CHASSIS (BACK VIEW)

   e. Carefully lift the fan module up. The faulty fan should remain on the table.
   f. Install the new fan. If it is a bottom fan, make sure it is on the stud properly, and then replace the washer, locking washer, and the nut.
   g. Carefully turn the module on its side, holding the new fan to make sure it stays in the correct position.
   h. Replace the self-tapping screw(s) which hold the fan to the casing. (1 screw for a bottom fan; 2 screws for a top fan.)
   i. Reconnect the 2 wires to the new fan.

6. To replace the fan module:
   a. Remove the 3 screws on the console PC board assembly. (See p. 122.)
   b. Remove the console PC board assembly. (See p. 122)
   c. Remove the console PC board casing from the new fan module.
   d. Install the console PC board in the casing of the new fan module. Replace the casing.
7. Slide the module in and push until it locks in place.
8. Replace the 2 nuts and lock washers.
9. Replace the front panel and power up the system.

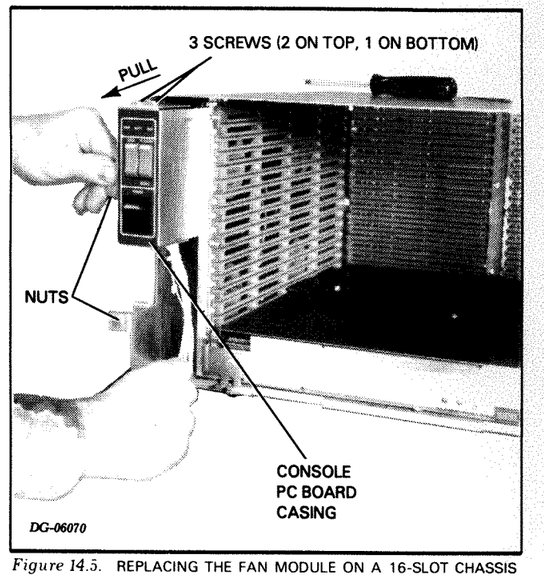

Figure 14.5. REPLACING THE FAN MODULE ON A 16-SLOT CHASSIS

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PC BOARD REPLACEMENT

1. Power down the system.

NOTE *If you are replacing a memory board or the power supply PC board, see the replacement procedures for these boards, pp. 126 and 127, respectively. For the CPU board, see below.*

2. Remove the front panel (see p. 118).
3. Locate the PC board that is to be replaced. (See your systems' Configuration Chart for slot assignments.)
4. Use the ejector keys to remove the PC board.
5. Make sure the new board is tailored (jumpered) correctly and install the new board. Make sure it is seated properly. (The ejector keys should close completely.)
6. Replace the front panel and power up the system.

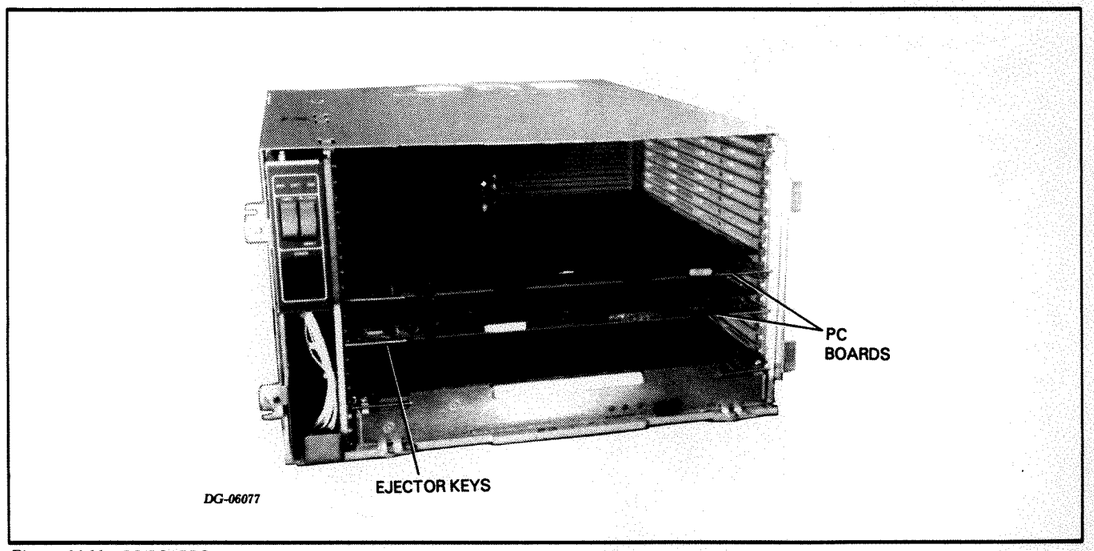

Figure 14.11. PC BOARDS

CPU BOARD REPLACEMENT

1. Power down the system.
2. Remove the front panel (see p. 118).
3. Remove the CPU board. (It is ALWAYS located in slot 1.)
4. Install the correct jumpers on the new CPU using the diagram and the tables below showing jumper positions and the Installation Data Sheets.
5. Install the new CPU board in slot 1 of the chassis. (Refer to the table below for the CPU assembly numbers.)
6. Replace the front panel and power up the system.

Table 14.1
CPU BOARD ASSEMBLY NUMBERS

Assembly No.	Description
005-012067	NOVA 4/X with Multiply Divide
005-012785	NOVA 4/X without Multiply Divide
005-012786	NOVA 4/S with Multiply Divide
005-012787	NOVA 4/S without Multiply Divide

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6. Place the chassis on a secure table.
7. Remove the top cover (9 screws on the top and 3 screws on the left or fan side).
8. Lift the top cover up and over to the left so that it lies on its side. (See photo below, Figure 14.7.)
9. Disconnect the wires from the fan that connect the fans to the power supply. Note the color scheme so you can replace them correctly.
10. Remove the 2 screws holding each fan to the cover and remove the fans.
11. Install the new fans and replace the 4 screws.
12. Reconnect the wires. (Refer to p. 133 for the correct wire color scheme if necessary.)
13. Place the cover back in position over the chassis and replace the screws (9 on the top and 3 on the side).
14. Slide the chassis back into the front of the cabinet.
15. Replace the 8 screws which secure the chassis to the cabinet rails. There are 2 screws per rail.
16. Replace the front panel.
17. Replace the power cord connector at the rear, and replace all I/O cables.
18. Plug in the AC source, close the rear cabinet door, and power up the system.

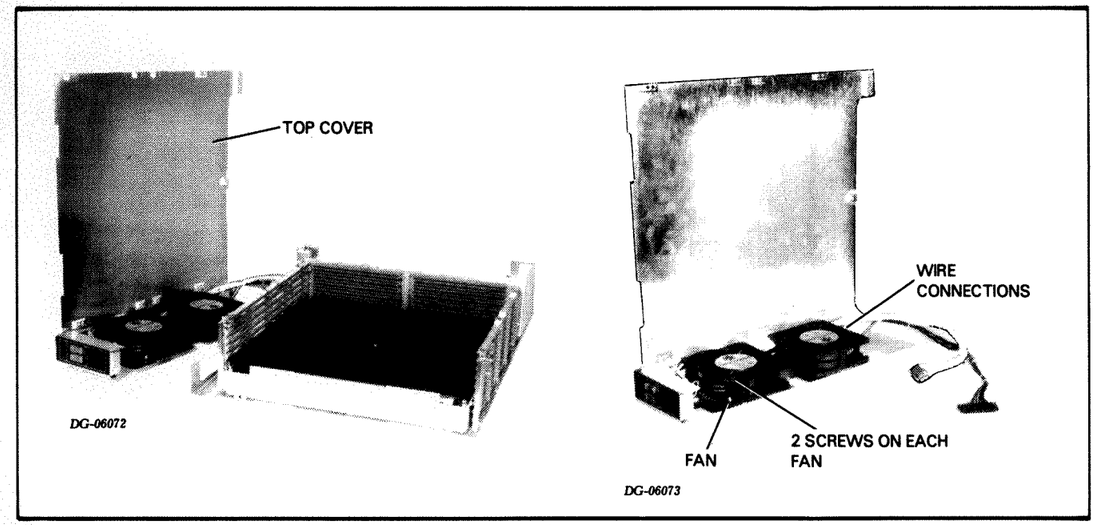

Figure 14.7. REMOVING THE TOP COVER, DISCONNECTING THE FAN MODULE FROM A 5-SLOT CHASSIS

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CONSOLE PC BOARD REPLACEMENT FOR 16-SLOT CHASSIS

1. Power down the system and remove the front panel (see p.118).
2. Remove the fan module (see p.118 , steps 3-4.)
3. Remove 3 screws, 2 on the top of the console PC board casing and 1 on the bottom. (Each screw has 1 lock washer.)

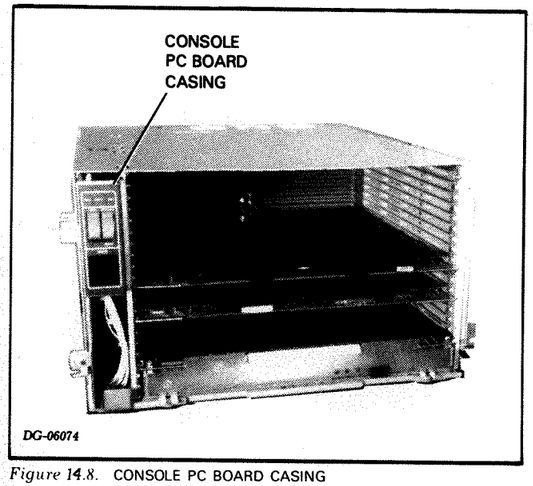

Figure 14.8. CONSOLE PC BOARD CASING

4. Unplug cable P1 on the back of the console PC board.
5. Remove the 4 screws which mount the PC board to its stand-offs. (Each screw has 2 lock washers.)
6. Mount the new PC board and replace the screws and lock washers.
7. Plug cable P1 into the new PC board.
8. Replace the 3 screws and lock washers on the PC board casing.
9. Replace the fan module and the front cover.

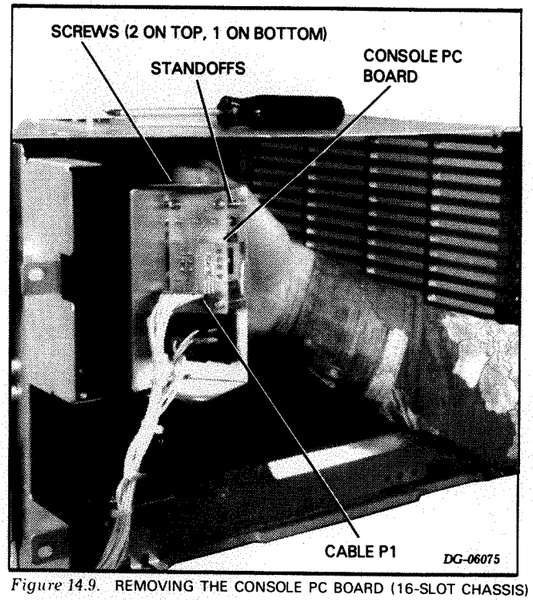

Figure 14.9. REMOVING THE CONSOLE PC BOARD (16-SLOT CHASSIS)

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CONSOLE PC BOARD REPLACEMENT FOR 5-SLOT CHASSIS

1. Go to the Fan Replacement For 5-Slot Chassis procedure (p.120) and perform steps 1-8.
2. Unplug cable P3 on the back of the console PC board.
3. Remove the 4 screws which mount the PC board to its stand-offs. (Each screw has 2 washers.)
4. Mount the new PC board and replace the screws and washers.
5. Plug cable P3 into the new PC board.
6. Go to page 121 and perform steps 13-18.

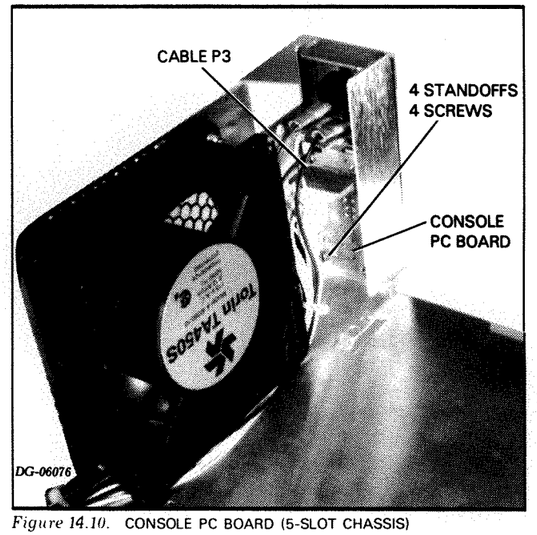

Figure 14.10. CONSOLE PC BOARD (5-SLOT CHASSIS)

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6. Remove the 5 screws on the top of the power supply assembly (one in each corner and one in the center) and remove the top cover.
7. Locate the battery in the front-left corner of the board.
8. Disconnect the two wires (red and black, positive and negative, respectively) that connect the battery to the PC board.

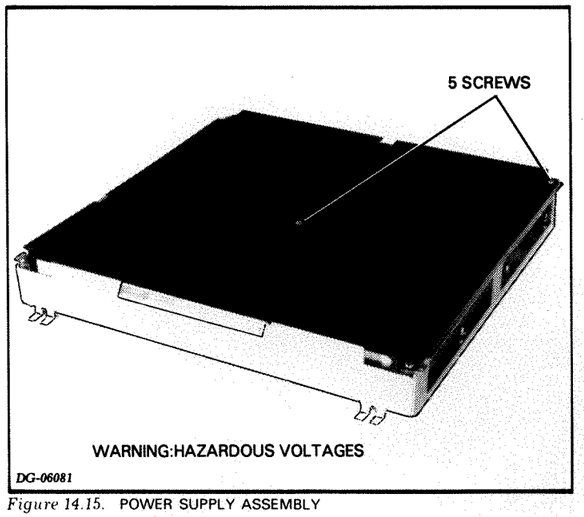

Figure 14.15. POWER SUPPLY ASSEMBLY

9. Remove the 4 screws that secure the battery bracket and remove the battery. Replace the bracket (4 screws).
10. Replace the top cover (5 screws).
11. Remove the 5 screws on the top of the new power supply assembly and remove the top cover.
12. Locate the battery bracket in the front-left corner of the board and remove it (4 screws).
13. Install the battery from the old assembly into the bracket of the new assembly.
14. Replace the bracket (4 screws) and connect the wires.
15. Replace the top cover (5 screws).
16. Install the new power supply PC board assembly into the chassis.
17. If this is a 5-slot chassis, replace the power cord and cable P1. Close the rear cabinet door.
18. Replace the 2 screws at the front of the assembly.
19. Replace the front panel.
20. Plug in the AC source. Power up the system.

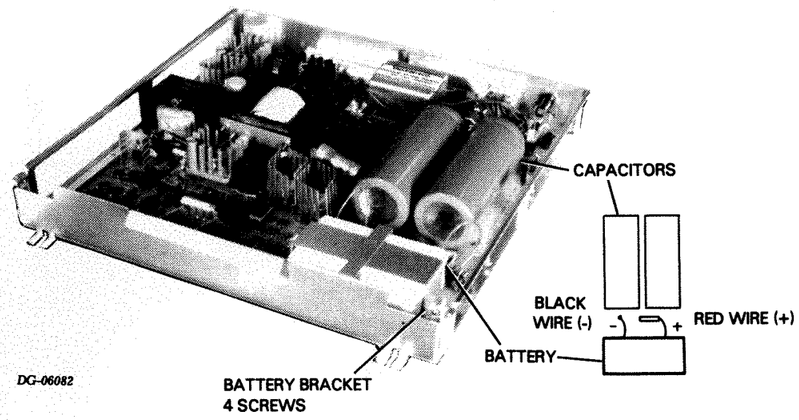

Figure 14.16. POWER SUPPLY PC BOARD

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Table 14.2
PROGRAM LOAD JUMPERS

Jumper	Jumper Position
W9	Jumper is in if program load device is a high-speed device; otherwise jumper is out.
W13, W15 W14, W12 W10, W8	Positions of these jumpers indicate the device code of program load device. W13 is most significant bit; W8 least significant bit.

Table 14.3
TYPE OF TRANSMISSION JUMPERS

Type of Transmission	Jumpers Inserted
20 MA CURRENT LOOP	W4, W7, W2, W1
EIA RS232-C	W6, W3

Table 14.4
BAUD RATE JUMPERS

Baud Rate	Jumper Position				
	W17	W18	W19	W20	W27
50	In	In	Out	In	Out
75	In	In	Out	Out	Out
110	Out	Out	Out	Out	In
134.5	In	Out	In	In	Out
150	Out	Out	Out	In	Out
200	In	Out	In	Out	Out
300	Out	Out	In	Out	Out
600	In	Out	Out	In	Out
1200	Out	In	Out	Out	Out
1600	Out	In	Out	In	Out
2400	Out	Out	In	In	Out
4800	Out	In	In	Out	Out
9600	Out	In	In	In	Out
19200	In	In	In	Out	Out

Table 14.5
CHARACTER LENGTH JUMPERS

Character Length	Jumper Position	
	W25	W24
5 Bits	In	In
6 Bits	Out	In
7 Bits	In	Out
8 Bits	Out	Out

Table 14.6
STOP BIT JUMPER

Number of Stop Bits	W23 Jumper Position
1	In
2	Out

Table 14.7
PARITY JUMPERS

Type of Parity	Jumper Position	
	W22	W21
Even	Out	In
Odd	In	In
None	Out	Out

Table 14.8
REAL-TIME CLOCK JUMPER

Function	W28 Jumper Position
Enables real-time clock	In
Disables real-time clock	Out

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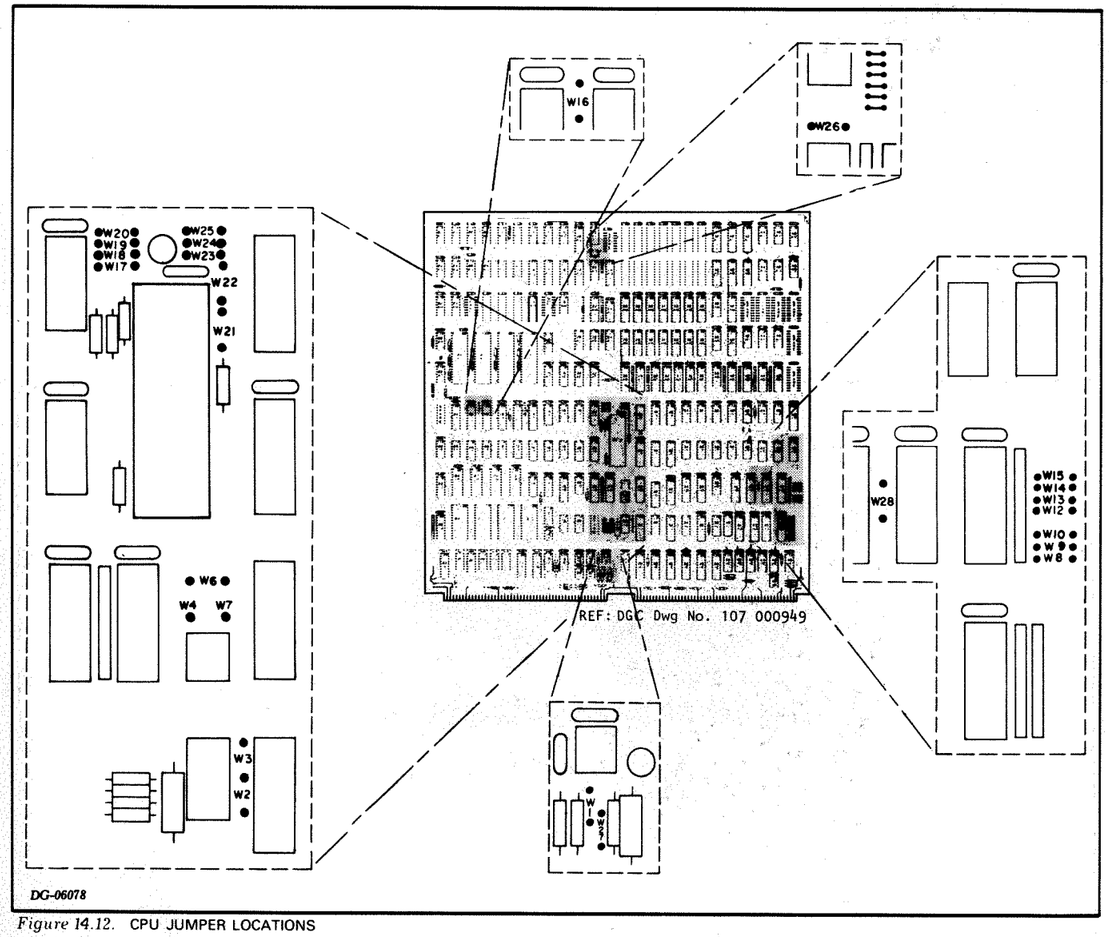

Figure 14.12. CPU JUMPER LOCATIONS

MEMORY BOARD REPLACEMENT

1. Power down the system.
2. Remove the front panel (see p.118).
3. Locate the failing memory board using the memory configuration table, and remove it using the ejector keys.
4. Insert the board select jumpers on the new memory board. (Refer to the Installation Data Sheets for jumpering information.) Be sure to select the jumper configuration for the correct size of the board and the memory locations it will occupy.
5. Return the memory board to the correct slot in the chassis.
6. Replace the front panel and power up the system.

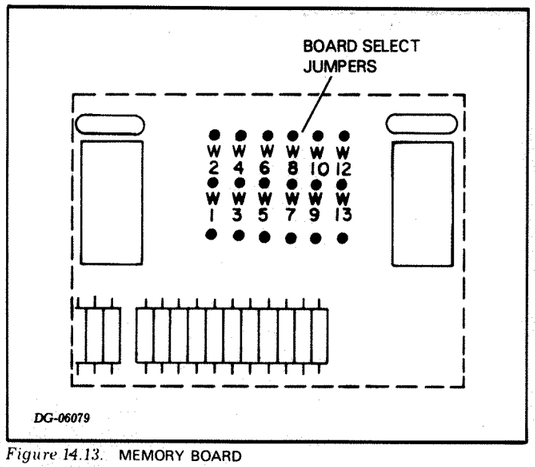

Figure 14.13. MEMORY BOARD

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POWER SUPPLY PC BOARD REPLACEMENT

1. Power down the system. Unplug the AC source from the cabinet.
2. If this is a 5-slot chassis, open the rear cabinet door and remove the power cord connector and the wiring harness cable P1.
3. Remove the front panel (see p.118). The power supply PC board assembly is located in slot 0 of the chassis.
4. Remove the 2 screws which secure the power supply assembly to the chassis.
5. Remove the assembly using the ejector keys.

NOTE *If you are replacing the power supply PC board for any 16-slot chassis, or a 5-slot chassis without the battery back-up option, proceed to step 16. If you are replacing the power supply PC board for a 5-slot chassis with the battery back-up option, wait for 5 minutes to allow the capacitors to discharge, and continue with step 6.*

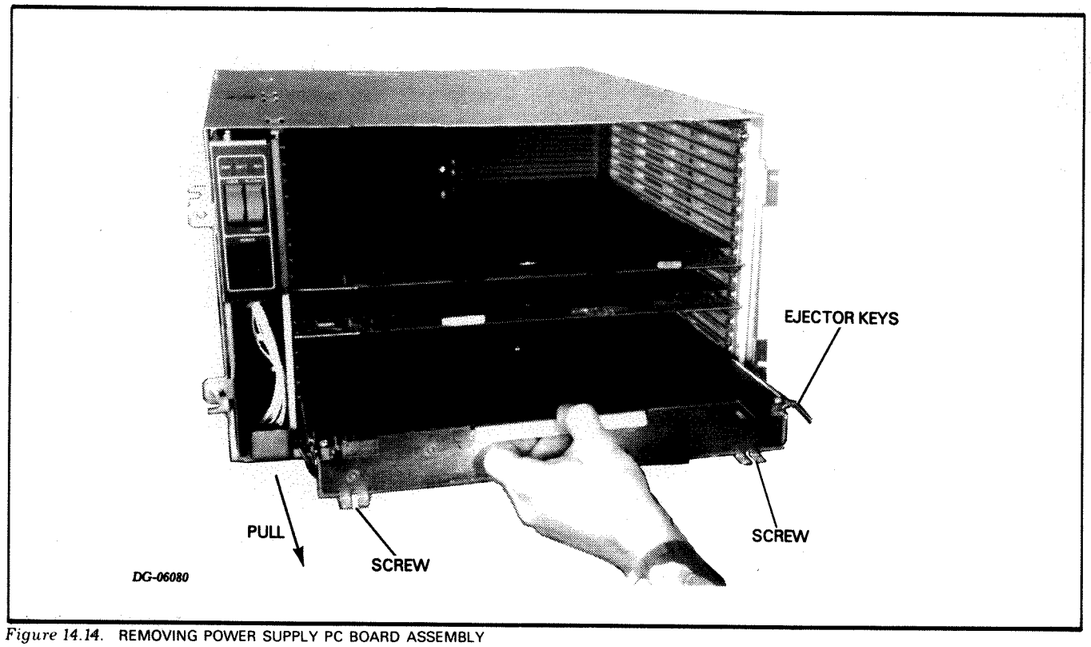

Figure 14.14. REMOVING POWER SUPPLY PC BOARD ASSEMBLY

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16-SLOT WIRING HARNESS REPLACEMENT

1. Go to the VNR Unit Replacement procedure (p.129) and perform steps 1-5.
2. Remove the 2 screws on cable P1. Unplug cables P1, P2, and P3, and remove the wiring harness. (Refer to the illustration below and wiring diagram No. 001-001607.)
3. Plug in cables P1, P2, and P3 of the new wiring harness in the proper sockets. (Refer to the illustration below and wiring diaram No. 001-001607.) Replace the 2 screws on cable P1.
4. Go to the VNR Unit Replacement procedure and perform steps 12-17.

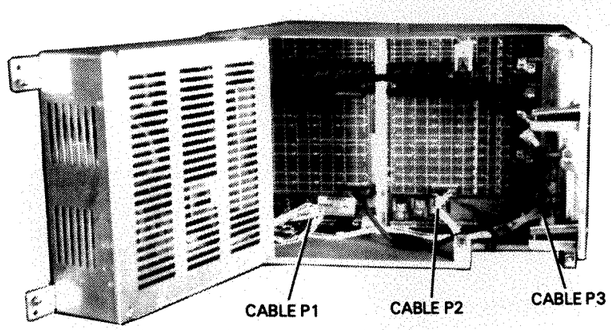

Figure 14.20. 16-SLOT CHASSIS, WITH VNR UNIT AND WIRING HARNESS EXPOSED

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VNR UNIT REPLACEMENT

1. Power down the system, open the rear cabinet door, and unplug the AC source from the cabinet. Wait AT LEAST 5 minutes before proceeding.
2. Unplug the power cord connector on the back of the VNR unit.
3. Loosen the 2 fasteners on the right side of the VNR unit (1/4 ccw turn).

NOTE *There may also be 2 shipping screws on the right side of the VNR unit as well as the fasteners. These screws should be removed and discarded.*

Pull the VNR unit on the right side so that it swings out on its hinges.

4. Remove the 4 screws on the inside cover. Remove the cover.

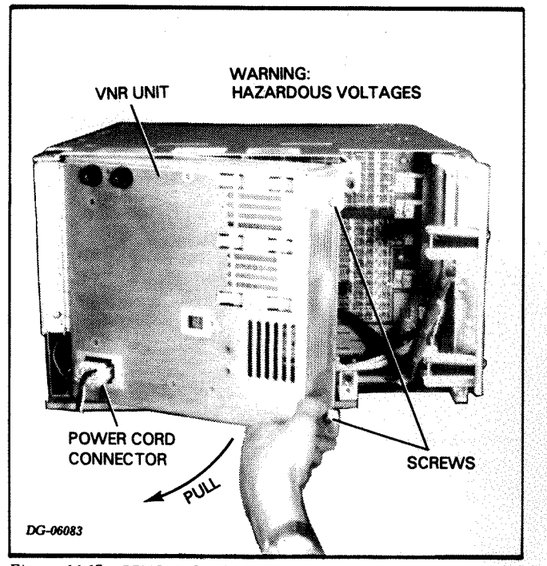

Figure 14.17. REMOVING VNR UNIT

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5. Unplug cable P4 located at the bottom right section of the unit.
6. When battery backup option is present, remove the battery bracket (4 screws). Disconnect the battery wires and remove the battery. Replace the battery bracket (4 screws).
7. Replace the inside cover (4 screws).
8. Remove the 4 screws located on the inside of the hinge.
9. Secure the new VNR unit to the chassis by replacing the 4 screws on the inside of the hinge.
10. Remove the 4 screws on the inside cover. Remove the cover.
11. When appropriate, remove the battery bracket (4 screws). Insert the battery from the old VNR unit and connect the wires. (The polarity of the wires is etched on the PC board.)
12. Connect cable P4 located at the bottom right section of the unit.
13. Replace the inside cover (4 screws).
14. Push the VNR unit in towards the chassis and tighten the 2 fasteners.
15. Connect the power cord connector, P1/J1, on the back of the VNR unit.
16. Plug in the AC source. Close the rear cabinet door.
17. Power up the system.

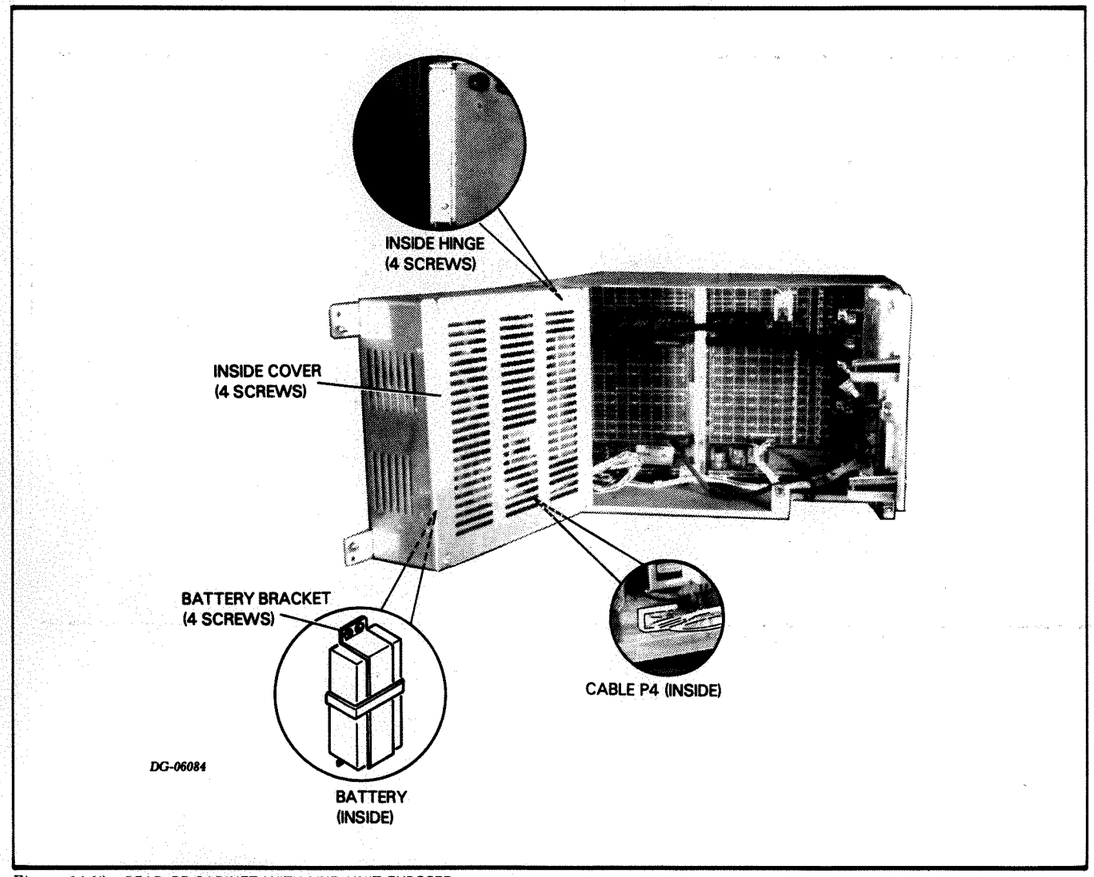

Figure 14.18. REAR OF CABINET WITH VNR UNIT EXPOSED

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PADDLEBOARD AND TERMINATOR REPLACEMENT

1. Power down the system.
2. Open the rear cabinet door. If it is a 16-slot chassis, you must swing the VNR unit out of the way (see p.129).
3. The terminators simply pull off and push on the backpanel. (Be careful not to bend backpanel pins.) They must be located on the pins of the highest slot containing a memory board. They must be positioned so that their connection starts at the center bar of the backpanel.
4. The paddleboards are mounted on a bracket on the right (fan) side of the chassis. They are supported by a pair of stand-offs between each board and a pair between the first board and the bracket. You can remove the stand-offs by hand.

   Their connections to the backpanel pull off and push off. (Be careful not to bend backpanel pins.) They must be positioned so that their connection starts at the center bar of the backpanel.

   The I/O cables are supported by strain relief brackets. There are two brackets per chassis. The brackets each contain one screw on the top to tighten them. The brackets are adjustable to accommodate different size cables.
5. Reposition the VNR unit if this is a 16-slot chassis. Close the rear cabinet door and power up the system.

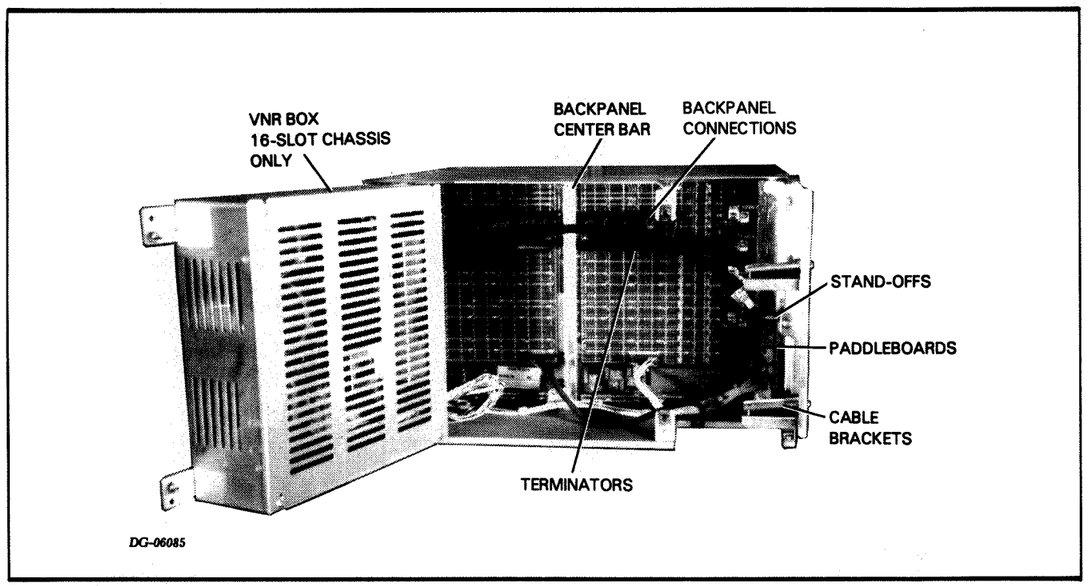

Figure 14.19. PADDLEBOARDS AND TERMINATORS

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BACKPANEL REPLACEMENT FOR 5-SLOT CHASSIS

1. Power down the system, open the rear cabinet door, and unplug the AC source.
2. Remove the front panel (see p. 118).
3. Open the rear cabinet door and remove the power cord connector and the wiring harness cable P1.
4. Remove all PC boards in the chassis (see replacement procedures for power supply board, memory, CPU, and other PC boards, pp. 127, 126, and 124).
5. Remove all connectors, terminators, and paddleboard connections from the backpanel. Note their location so you can reconnect them on the new backpanel.
6. Remove the 8 screws which secure the chassis to the cabinet rails. There are 2 screws per rail.
7. Slide the chassis out from the front of the cabinet. The slides will support it until it is about half way out of the cabinet.

CAUTION *The chassis weighs about 50 lbs (about 23 kgs) fully loaded. You may need help.*

8. Place the chassis on a secure table.
9. Remove the top cover; there are 9 screws on the top and 3 screws on the left (fan) side.
10. Lift the top cover up and over to the left so that it lies on its side.
11. Remove the screw that holds the backpanel to the base of the chassis.
12. Remove the 4 screws that secure the backpanel to the back of the chassis.

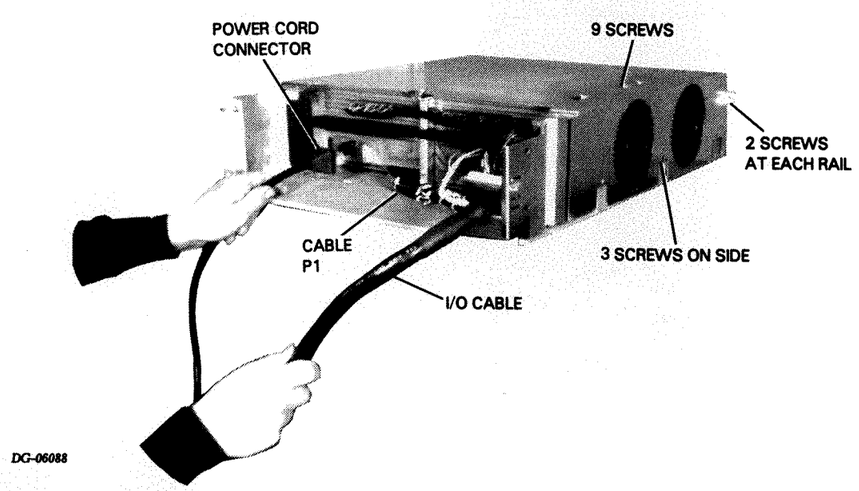

Figure 14.24. REMOVING CABLES FROM BACK OF 5-SLOT CABINET

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5-SLOT WIRING HARNESS REPLACEMENT

1. Go to the procedure for 5-slot fan replacement (p. 120) and perform steps 1-8.
2. Remove cable P3 from the console PCB, the 4 wires from the power switch, and the 4 wires from the fans (2 wires per fan). (Refer to the illustration below and wiring diagram No. 001-001637.) Pull these cables of the harness through the slot in the backpanel.
3. Remove the wiring harness cables connected to the backpanel, P2 and P1.
4. Being very careful to follow the color scheme shown in the illustration below, connect the new wiring harness to the fans (2 wires per fan), the power switch (4 wires), and the console PCB (cable P3).
5. Pull the 2 remaining cables of the harness (P1 and P2) through the slot in the backpanel and plug them in the appropriate locations. (Refer to the illustration below and wiring diagram No. 001-001637.)
6. Go to the procedure for fan replacement and perform steps 13-18.

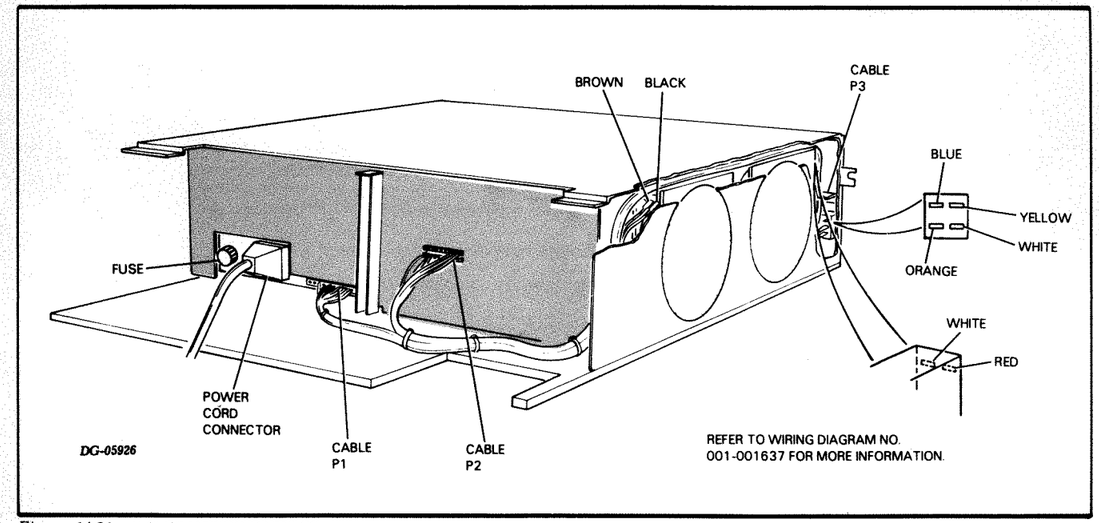

Figure 14.21. 5-SLOT WIRING HARNESS

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BACKPANEL REPLACEMENT FOR 16-SLOT CHASSIS

CAUTION *This procedure requires at least two people. The chassis weighs about 110 lbs. (about 50 Kgs.) fully loaded.*

1. Power down the system and unplug the AC source.
2. Remove the front panel (see p. 118).
3. Remove all PC boards in the chassis (see replacement procedures for power supply board, memory, CPU, and other PC boards, pp. 127, 126, and 124).
4. Remove the fan module (see p. 118).
5. Open the rear cabinet door and remove the power cord from the VNR unit.
6. Swing out the VNR unit (see p. 129).
7. Remove all connectors, terminators, and paddleboard connections from the backpanel. Note their location so you can reconnect them on the new backpanel.
8. Remove the 8 screws which secure the chassis to the cabinet rails. There are 2 screws per rail.
9. With one person on each side of the cabinet, slide the chassis out from the front of the cabinet. The slides will support it until it is about half way out of the cabinet.
10. Place the chassis on a secure table.
11. Remove the top cover; there are 13 screws on the top and 3 screws on the left-hand side (where the fan module is located).

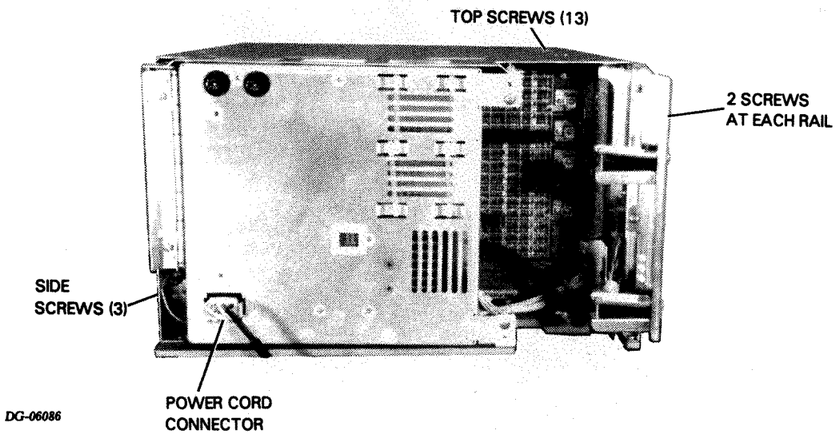

Figure 14.22. BACKPANEL FOR 16-SLOT CHASSIS

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12. Remove the screw which holds the backpanel to the base of the chassis.
13. Remove the bracket which supports the fan module connector (2 screws).
14. Remove the 6 screws which secure the backpanel to the back of the chassis.
15. You should now be able to slide the backpanel out towards the right-hand side, away from the fan module.
16. Slide in the new backpanel and replace the 6 screws which secure it to the back of the chassis.
17. Replace the bracket that supports the fan module connector (2 screws).
18. Replace the screw that holds the backpanel to the base of the chassis.
19. Replace the top cover: 13 screws on the top and 3 screws on the left-hand side (where the fan module is located).
20. Slide the chassis back into the front of the cabinet.
21. Replace the 8 screws that secure the chassis to the cabinet rails.
22. Replace all connectors, terminators, and paddleboard connectors on the backpanel.
23. Return all the PC boards to their proper location in the chassis. (Refer to the Configuration Chart and replacement procedures for power supply board, memory, CPU, and other PC boards, pp. 127, 126, and 124).
24. Replace the fan module (see p. 118).
25. Replace the front panel (see p. 118).
26. Return the VNR unit to its proper position (see p. 129).
27. Reconnect the power cord to the VNR unit.
28. Plug in the AC source, close the rear cabinet door, and power up the system.

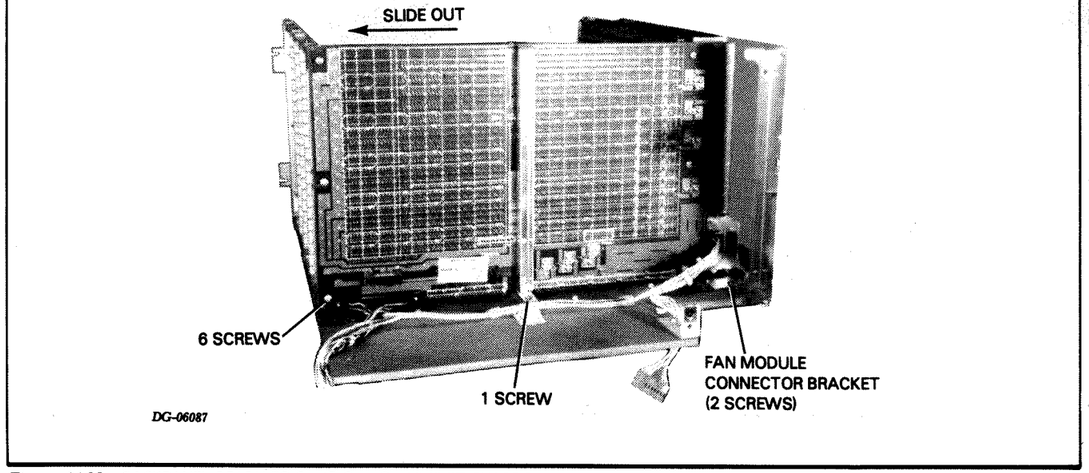

Figure 14.23. BACKPANEL READY TO SLIDE OUT OF 16-SLOT CHASSIS

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13. You should now be able to slide the backpanel out towards the right side, away from the fans.
14. Slide in the new backpanel and replace the 4 screws which secure it to the back of the chassis.
15. Replace the screw in the base of the chassis.
16. Place the cover back in position over the chassis and replace the screws (9 on the top and 3 on the side).
17. Slide the chassis back into the front of the cabinet.
18. Replace the 8 screws which secure the chassis to the cabinet rails. There are 2 screws per rail.
19. Return all the PC boards to their proper location in the chassis. (See the Configuration Chart.)
20. Replace the front panel.
21. Replace the power cord connector and cable P1 at the rear, and replace all I/O cables.
22. Plug in the AC source, close the rear cabinet door, and power up the system.

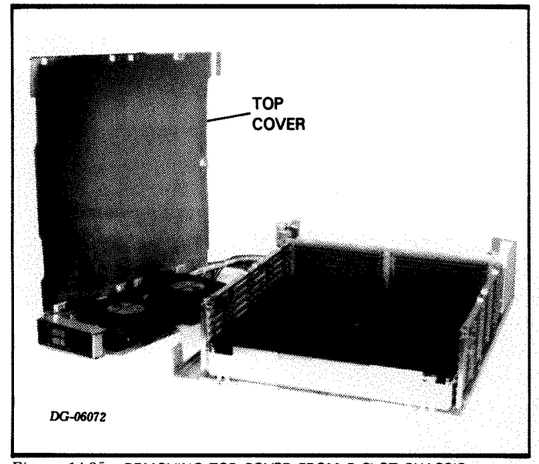

Figure 14.25. REMOVING TOP COVER FROM 5-SLOT CHASSIS

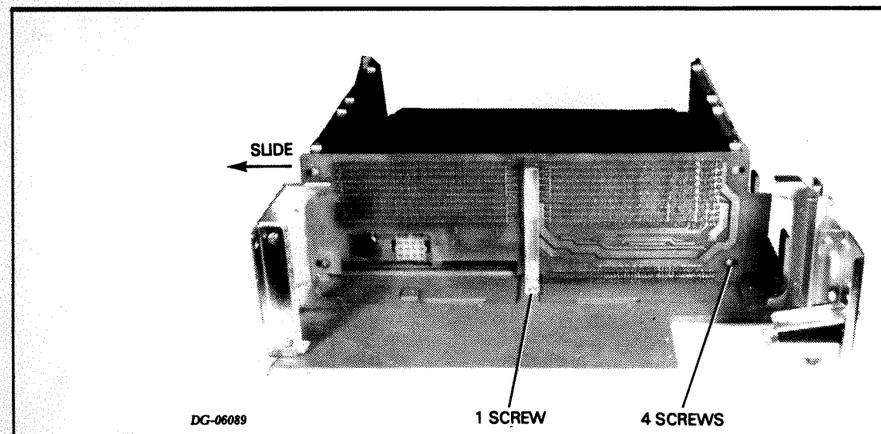

Figure 14.26. SLIDING BACKPANEL OUT OF 5-SLOT CHASSIS

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APPENDIX A
RDOS PANIC CODES

Panic Code No.	Description
1	Not used.
2	This panic is caused by an error in the operating system file SYS.DR. Failure may be caused by memory or disc subsystem prior to the write data operation on the disc media.
3	This panic is caused by a stack overflow inside the RDOS addressing space. Failure may be caused by a CPU/memory related problem or it may be the result of an I/O controller continually interrupting. In the latter case, the stack would overflow from continuous return blocks being pushed on the stack.
4	This panic can be caused by any one of the following: a. RDOS encountered a logical block address outside the boundaries of the disc. b. A device code is encountered in a table for which there is no corresponding device driver. c. A table address was found that pointed to the wrong memory address. Failure may be caused by the disc subsystem, memory, or the CPU.
5	This panic is caused by a fatal error on the disc from which RDOS was booted. Failure is caused by the malfunctioning of the disc subsystem used to boot RDOS.
6	This panic is caused by the lack of an interrupt from the disc that was booted. Failure is caused by the malfunctioning of the disc subsystem used for last boot.
7	This panic can only occur when either the 6060, 6061 or 6067 disc subsystem is present. It indicates that the disc returned an illogical status to the operating system. Accumulator 0 contains the DIA status word; AC1 contains the DIB status word. Failure is caused by the malfunctioning of the disc subsystem.
8	Not used.
9	Not used.
10	This panic occurs when the operating system receives an interrupt from a device that is not recognized by the operating system. The operating system attempts to clear the interrupt 2000 times before it issues panic 10. Accumulator 2 contains the device code of the interrupting device causing the problem. If it is a non-existent device code, check pin B29 (INTR) of each open slot on the backpanel.
11	Not used.
12	Not used.
13	This panic is primarily related to either the operating system or the user software. Failure could be caused by memory.
14	This panic can only occur in a dual processor system containing a 4240 Interprocessor Bus (IPB) Subsystem. It can be caused by an interrupt from the interval timer (indicating a failure in the other processor) or an illegal message from the other CPU. If accumulator 2 contains the octal number 064400, the interrupt was the cause of the failure. In either case, troubleshoot the 4240 IPB subsystem.
15	This panic is caused by a map violation in a user interrupt handler. Accumulator 0 contains the logical address at which the trap occurred. Failure could be caused by malfunctioning of the MMPU on the NOVA 4/X CPU.
16-20	Not used.
21	This panic indicates an unrecoverable I/O error occurred on the RDOS master disc unit.

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Table C.1
DATA FOR CASSETTE BOOTSTRAP LOAD

Location	Input
1000	152440
1001	176440
1002	24402
1003	125401
1004	177624
1005	63600
1006	775
1007	62677
1010	175203
1011	771
1012	055177
1013	151400
1014	14177
1015	764
1016	4200

- Rewind the tape to the beginning.
- Press the READ key on the cassette loader. When a tone sounds, enter the following on the terminal:

  !1000R

- In a few seconds, the tone will stop and the terminal will print the top memory address to be used by the diagnostic programs. For a 64K byte or larger system, the top memory address is 77777_8; for a 32K byte system it is 37777_8. If the tone does not stop before 9 feet of tape have read, the Cassette Executive program probably did not load. In this case, repeat step b.

6. Load a diagnostic program from the cassette using the procedure below. If you do not have a listing of the programs on the cassette and their file numbers, the program in file 1 will print out such a listing. Load this program as described below, and run it starting at address 200 as described in step 7.

   a. Depress the READ switch on the loader, if it is not already depressed.

   b. Enter top memory address used by the diagnostics and press the R key on the terminal.

   c. When the terminal prints out a number sign (#) enter the file number of the program you want to run followed by a Carriage Return.

   d. The terminal will print the file number of each file it comes to. You can keep the terminal from printing these numbers and advance the tape more quickly by holding down the Motion Control Override and the Fast Forward keys on the cassette loader. If the file numbers printed out are higher than the number you entered, rewind the tape by pressing the Motion Control Override and the Rewind keys on the loader.

   e. When the specified file is reached, it will be loaded into memory and the terminal will print the following message:

   !LOADED<file number> <top memory address>
   !

7. Run the program by entering the following on the terminal:

   !<starting address> R

   NOTE: *All programs start at address 200 except for the N4MDM and N4MDU1 programs on the INTERIM UPDATE cassettes #5, #6.1, and #6.3. These programs start at 240 and 205, respectively.*

8. To run another program, press the Break key on the terminal and repeat steps 5 through 7. If you cannot load a program, repeat the entire procedure by starting at step 1.

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APPENDIX B
DTOS LOADING PROCEDURES

FROM MAGNETIC TAPE UNIT

1. Power up processor and tape drive.
2. Set SELECT switch on tape drive to unit 0.
3. Press RESET switch on tape drive.
4. Remove write-enable ring from tape; load and thread tape.
5. Press LOAD and then ON LINE switches on tape drive.
6. Enter 100022L on system terminal keyboard.
7. The system terminal will print or display the following message:

   TYPE IN THE ID NUMBER FOR THIS CPU AND CR
   (0-NOVA 1200, 1-NOVA 800, 2-NOVA II, 3-NOVA III, 4-NOVA IV OR
   5-ECLIPSE)

8. Enter 4 in the keyboard followed by a Carriage Return.
9. The system terminal will print or display the following message:

   TYPE IN CPU SUBTYPE AND CR
   (0-NOVA 4C, 1-NOVA 4S OR X)

10. Enter 1 in the keyboard, followed by a Carriage Return.
11. The system terminal will print or display the following message:

    TOP OF MEMORY XX
    HIDTOS REV XX
    *
    (The "top of memory" number varies with system memory size. The revision number varies with system revision. The asterisk is the DTOS prompt: enter DTOS commands as specified in Part II, Chapters 7 and 8.)

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FROM DISC OR DISKETTE

1. Power up processor and disc or diskette drive.
2. Insert disc cartridge, pack or diskette into drive assigned logical unit 0.
3. Recalibrate the drive as follows:

   a. For 6060/6061 and 6067 disc drives

      Press RESET switch on front console

   b. For diskette

      Open and close drive door
      Make sure the READY and TRACK 0 indicators are lit

   c. For other disc drives, use the virtual console to enter the following data in the locations indicated below. Then enter 00000R in the keyboard.

Table B.1
DATA FOR DTOS LOAD PROCEDURE

Locaton	Input
00000	063033 (for primary device) 063073 (for secondary device)
00001	065333 (for primary device) 065373 (for secondary device)
00002	063077
AC0	000000
AC1	003400

4. When the console prompt (!) appears, enter the following in the keyboard.

   a. For 6060, 6061 and 6067 disc drives:

      100027L (for primary device)
      100067L (for secondary device)

   b. For other disc drives:

      100033L (for primary device)
      100073L (for secondary device)

5. The system terminal will print or display the following message:

   TYPE IN ID NUMBER FOR THIS CPU AND CR
   (0-NOVA 1200, 1-NOVA 800, 2-NOVA II, 3-NOVA III, 4-NOVA IV OR 5-ECLIPSE)

6. Enter 4 in the keyboard followed by a Carriage Return.
7. The system terminal will print or display the following message:

   TYPE IN CPU SUBTYPE AND CR (0-NOVA 4C, 1-NOVA 4S OR X)

8. Enter 1 in the keyboard, followed by a Carriage Return.
9. The system terminal will print or display the following message:

   TOP OF MEMORY XX
   HIDTOS REV XX
   *
   (The "top of memory" number will vary with system memory size. The revision number varies with disc build operator input. The asterisk is the DTOS prompt: enter the DTOS commands as specified in Part II, Chapters 7 and 8.)

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APPENDIX C
FIELD SERVICE CASSETTE PROCEDURES

When you cannot run diagnostic test programs using DTOS, you can run them using the field service cassette. Load the diagnostic programs following the procedure below and run them in the sequence given in the troubleshooting flowchart in Chapter 7.

Throughout the flowchart, action recommendations following each program test are made solely on a pass/fail basis. To determine if a test passed, refer to the Sample Program Run Summary for the particular test at the end of Chapter 7.

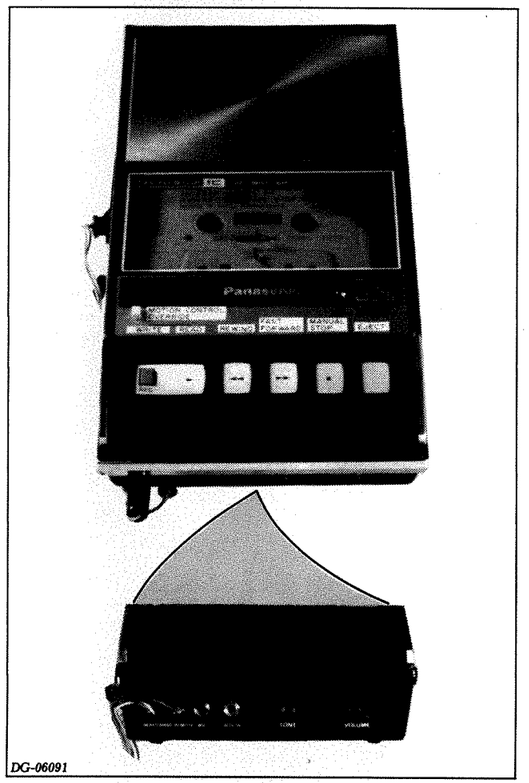

Figure C.1 THE FIELD SERVICE CASSETTE MACHINE

LOADING PROCEDURES

1. Plug the cassette cable into backpanel pins A68 to A100 in any I/O slot.
2. Load the cassette containing the NOVA 4 diagnostics in the cassette loader.
3. Set the VOLUME control on the loader to between 5.5 and 6.
4. Power up the processor.
5. Load the Cassette Executive program into the top of memory following step a or step b below:

   a. Using the Automatic Cassette Load.

- Rewind the tape to the beginning.
- Press the READ key on the cassette loader.
- When a tone sounds, press the F key on the system terminal. In a few seconds, the tone stops and the terminal prints the top memory address to be used by the diagnostic programs. For a 64K byte or larger system, this top memory address is 77777_8; for a 32K byte system it is 37777_8.

  If the tone does not stop before 9 feet of tape have been read, the Cassette Executive program probably did not load. In this case, repeat step a. If the program fails to load after several attempts, use the cassette bootstrap as described in step b. You might also check to see if the cassette bootstrap was loaded correctly. (The automatic cassette load program loads the cassette bootstrap into memory starting at location 2.)

b. Using the Cassette Bootstrap.

- Using the virtual console, enter the data given in Table C.1 in the locations indicated.

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TAPE TAPE

FOLD FOLD

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APPENDIX D
TIMING DIAGRAM FOR SYSTEM CLOCKS

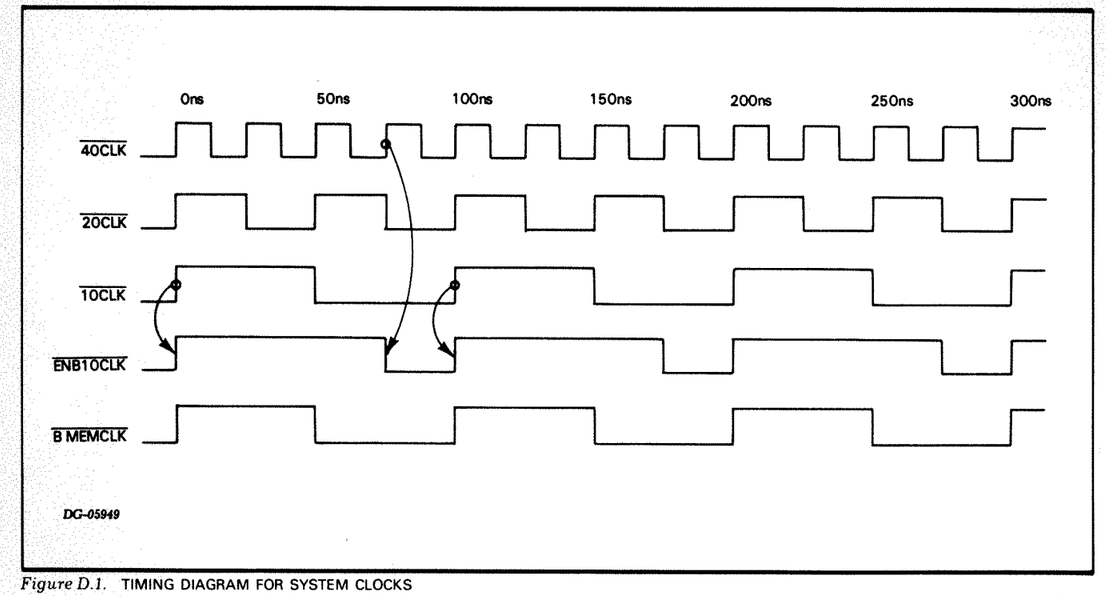

Figure D.1. TIMING DIAGRAM FOR SYSTEM CLOCKS

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