

Griffith

COMPANY CONFIDENTIAL

STRETCH MEMO NO. 45

September 19, 1956

MEMORY WORD LENGTH AND INDEXING

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At a meeting held on September 17, 1956, attended by Messrs. F. P. Brooks, W. Buchholz, S. W. Dunwell, W. A. Hunt, B. L. Sarahan and W. Wolensky, the following conclusions were reached. These decisions are not necessarily final since nothing in STRETCH can be considered frozen at this time.

1. Memory Word Length - (See Stretch Memo No. 40)

The memory word length will now be 64 bits, not counting any error detection and correction bits. Sub-multiples of 32, 16 or 8 bits may also be used if necessary.

2. Input-Output Byte Size

The maximum input-output byte size for serial operation will now be 8 bits, not counting any error detection and correction bits. Thus, the Exchange will operate on an 8-bit byte basis, and any input-output units with less than 8 bits per byte will leave the remaining bits blank. The resultant gaps can be edited out later by programming.

3. Memory Address Blocking

20 bits are needed for a memory addressing capacity of 1 million words, with an additional 6 bits for addressing the bits within a word. A continuous set of address numbers will be needed to permit indexing through all of memory, but it would be unreasonable to have to provide one or more 26-bit addresses for every instruction.

A form of blocking will be needed where the direct addresses in most of the instructions will provide only the lower-order address bits, with the high-order address bits being supplied from the specified index register or, if not indexed, from the instruction counter. This will provide easy direct addressing within the memory block assigned to a particular program, and still permit indexing to any area of memory. Precautions must be taken when the program itself has to cross block boundaries. While this scheme is a compromise, it has the advantage of providing built-in relative addressing which is particularly useful when several independent programs have to be run concurrently.

The most appropriate size of the blocks has yet to be determined.

4. Index Registers

Index registers will be part of addressable storage, either the core memory or the addressable transistor registers. Each register will contain at least,

- (a) i --- the current value of the modifier (or index)
- (b) n --- the number of bits in i (a maximum of 26)
- (c) B or L(B) --- the upper limit of i or its address
- (d) b --- a bit to indicate whether (c) is immediate (the limit B itself) or direct (the address of the limit, L(B)).

n is used for shifting in multiple indexing (see below).

Cyclic operation will be assumed to consist of the following standard functions:

Initially set index to zero.

Advance index by adding any specified positive integer.

Compare current index with limit, and transfer control.

If limit is reached, reset index to zero for restart.

Multiple indexing will be used to obtain non-zero base addresses and multiple loops. The above scheme will also be used for counting. Every effort will be made to achieve desired results directly instead of by trickery.

Counting down, in such applications as reading tape backwards, will be obtained by adding complements.

5. Multiple Indexing

Following the principle that every index quantity should be stored and modified at only one place in a program, it must be possible to combine the contents of more than one index register to modify a data address each time it is used. There should also be no limit, except for a reduction of speed, on the number of times this can be done.

Thus, the 3-dimensional quantity a_{ijk} will be specified in the program by giving,

$$a_{000}, L(i), L(j), L(k),$$

where

a_{000} is the base address if direct addressing is used, or the location of the base address (another index register) if indirect; and $L(i)$, $L(j)$, $L(k)$ are the addresses of the index registers containing i , j , k .

The address is then computed automatically as

$$a_{000} + k + 2^{n_k} j + 2^{(n_k + n_j)} i$$

where n_k is the number of bits in k , etc. In other words, j is shifted to the left of the highest bit of k and i is shifted to the left of that. This means that successive elements in any dimension of any array must be separated by some power of 2. If the length of the row or column in any dimension is less than a power of 2, there will have to be some empty spaces. This would not be a severe penalty, and it results in a simpler and faster mechanism. (The alternative would be multiplying instead of shifting).

Other effects will be obtained by explicit programming.

Trailer instructions will be used to specify as many index registers as desired.